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Design and implementation of a single-phase five-level inverter using a DC Source with voltage balancer on capacitor

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ABSTRACT

The global use of renewable energy resources has led to the design and development of high performance, efficient, controllable, and cheap multilevel inverters, which act as a solution to the numerous power deficiencies. However, in terms of control, these multilevel inverters are often associated with DC sources and complexity. Therefore, this research designed a single-phase five-level inverter using a DC source, with a novel sinusoidal pulse-width-modulated (SPWM) control scheme. The system consists of a flying capacitor DC-DC converter and H-bridge inverter (FCDCDC-HBI). A single absolute reference signal and the phase-shifted triangular carrier were used to generate SPWM to enhance the capacitor voltage balance. The designed inverter is capable of producing five levels of output voltage levels, namely Vi, Vi/2, 0, −Vi/2, and −Vi from a DC supply, thereby reducing the overall cost and complexity of the SPWM system. This research also produced a detailed operation principle of the proposed system, which was verified through simulation and implemented using a prototype. Finally, hardware implementation results are presented to check the performance of the inverter.

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1. INTRODUCTION

Over the years, various studies have been carried out to determine the possibility of a reduction total harmonic distortion in power inverter that used in industrial application. The single-phase multilevel inverters have rise in popularity for low-voltage on/off grid grid-tied inverters [1]-[3]. These inverters are expected to operate with high efficiency, low output voltage/current total harmonic distortion, simple control, and better performance during steady and transient operations. The multilevel inverter has several benefits over the two-level type with better power quality, reduced stress on the load, and others. Nevertheless, the neutral diode clamped of the multilevel inverter [4], [5] faces the inability to produce large numbers of active power switches, DC sources, and inadequate power balancing input. Although the flying capacitor of the multilevel inverter [6]-[8] has a significant DC power source, it is faced with voltage balancing problems and complex control algorithms. One of the many solutions to overcome this problem is to use a shifted carrier signal and combinational logic gate [9]-[11]. This study is also based on designing a single-phase cascaded H-bridge converter for grid-connected PV applications [12], [13], with the cascaded topology in need of isolated DC supplies and several power switches. Therefore, this research analyzes a single-phase symmetrical multilevel inverter topology composed of two parts, namely the level (high-frequency switching) and polarity generators (low- frequency of 50Hz) [14]. Some asymmetrical topologies of the multilevel inverters used to obtain several output steps without increasing the switch count are shown in [15]-[18], with the DC voltage sources asymmetrically represented in geometric progression.

This research developed and implemented a five-level inverter topology that uses five active switches and one passive switch [19], [20]. Previous studies utilized four active switches [21] and needed two DC sources. However, one of the drawbacks of this type of inverter is the number of power switching devices, and isolated DC power sources, increasing the cost and circuit complexity. Therefore, a hybrid multilevel inverter implemented using an H-bridge inverter, and three-level cells were developed [22]. This device needs eight active power switches to create a five-level inverter topology, which was developed from the three-level H-bridge using a single DC source [23]. Furthermore, the developed inverter needs seven active power switches to generate a five-level output voltage. A single active power switch carried out the balancing capacitor with a more complicated control configuration. A five-level inverter is achieved by connecting the H-bridge with a two DC power source, using a multilevel inverter coupled in series [24]. A five-level inverter topology was also designed, which used a single DC source with eighty-six active switches [25]. This inverter used the space vector polygon formed to control the five-level inverter. Therefore, the risk of unbalanced capacitor voltage exists when the inverter is not properly modulated. Furthermore, previous studies developed a multilevel inverter which uses a DC source without split capacitors. This is likely to be the most wanted topology, however, this inverter has not been properly, and the dc component on the inductor current is dangerous for full use of magnetic core [26], [27]. The five-level inverter consisting of five active power switches and two capacitors was developed by [28], however it needed more control for balancing the capacitor. The five-level inverter (seven active switches) used phase-shifted carrier to control and balance the bulk capacitor, it uses six active power switches without any sensors for operated that inverter [29]. Furthermore, the PV-grid application used a multilevel inverter associated with a DC source is suitable for this application [1], [3], [30].

This research proposed a single-phase five-level inverter using a DC source with a simple voltage balancer on a capacitor to make a better level. It also depends on the three levels generator of a Flying Capacitor DC-DC Converter (two diodes, two active power switches, and one capacitor) and H-bridge Inverter (FCDCDC-HBI) into a new single-phase five-level inverter using a single DC source and a novel sinusoidal pulse width modulation (SPWM) strategy. An operation mode is analyzed to obtain a SPWM pattern that is able to balance the capacitor voltage using a phase-shifted carrier signal of 180^0, which automatically enables the equilibrium voltage on the flying capacitor. The FCDCDC used to determine the size of the capacitor is carried out by storing quality valued energy in the capacitor and inductor. This condition occurs when charging and discharging the charge in the capacitor, therefore, it eliminates the need for sensors and a complex control algorithm system to balance the voltage on the capacitor. The proposed five-level inverter and its controller's performance was validated using Power Simulator software and prototyping the laboratory experiments.

2. RESEARCH METHOD

This research was carried out using a hybrid multilevel topology, divided into two parts. The Flying Capacitor DC-DC Converter is the fist part, with high-frequency switches used to generate three levels. Meanwhile, the H-Bridge Inverter is the second part, which operates at a low-frequency of 50Hz, as shown in Figure 1.

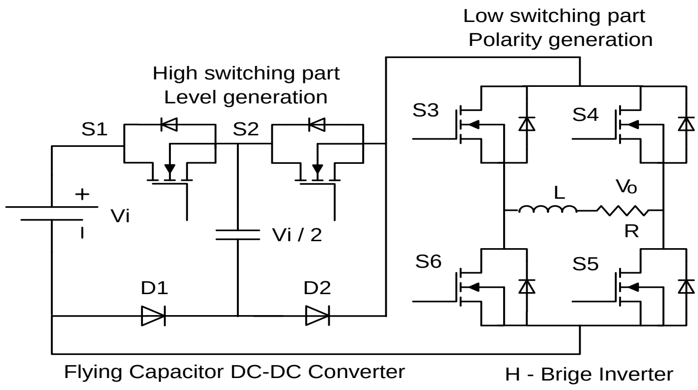


Figure 1. Proposed FCDCDC-HBI topology

The FCDCDC-HBI inverter always has two operating conditions, namely positive and negative values, which comprise a five-level inverter working principle. Figure 2 is a positive operating condition, mode of operation 1 consists of all power switches (*S1* and *S2*) on the FCDCDC and HBI topology with *S3* and *S5* switched "on," as shown in Figure 2 (a). Mode of operation 2 comprises of a power switch (*S1* or *S2*) on the FCDCDC and HBI topology with *S3* and *S5* switched "on," as shown in Figure 2 (b) and Figure 2 (c). The capacitor charges and discharges directly, as shown in Figure 2 (b) and Figure 2 (c), respectively. This operation mode balances the voltage on the capacitor. Mode of operation 3 comprises of no power switches (*S1* and *S2*) on the FCDCDC and HBI with *S3* and *S5* switched "on," as shown in Figure 2 (d).

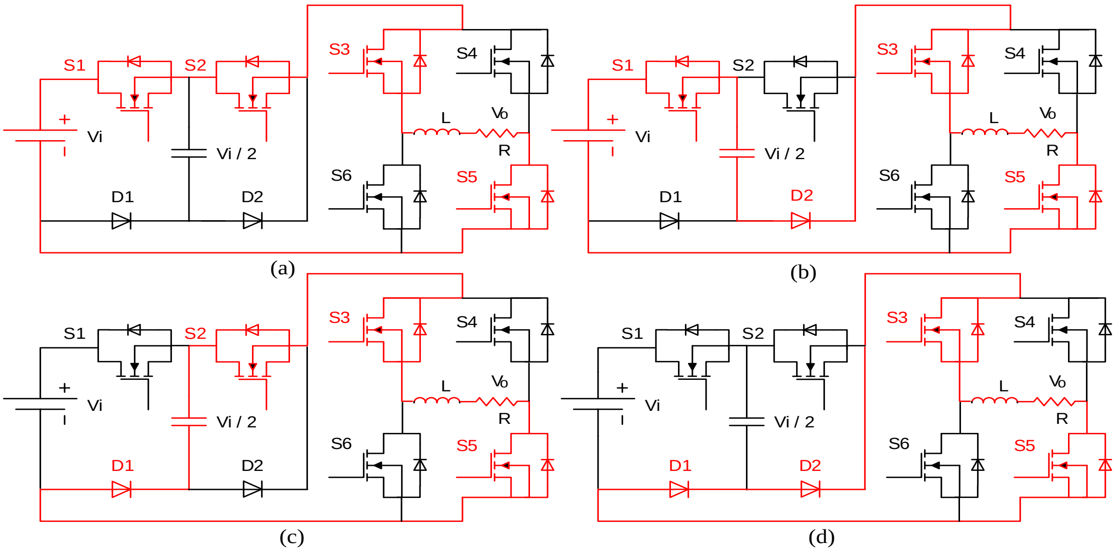


Figure 2. Mode of operation on positive value, (a) 1, (b) 2a, (c) 2b, (c), (d) 3

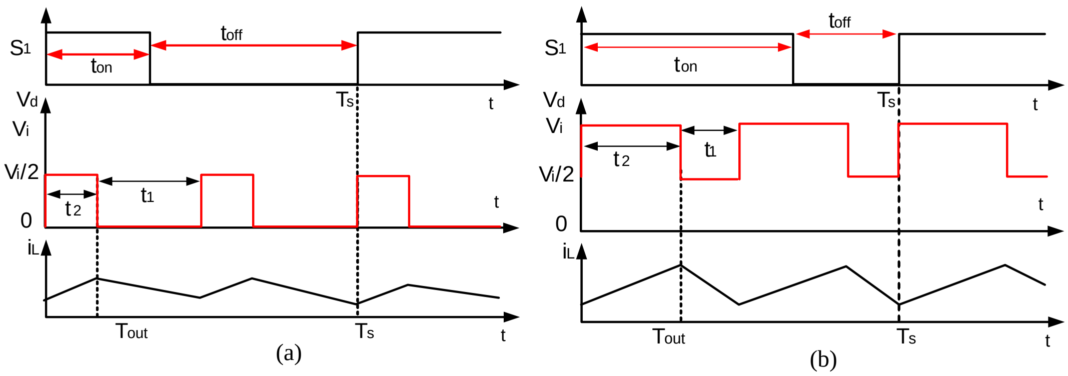


Figure 3. Switching operation, (a) on interval $0 \le m \le 1/2$, (b) on interval $1/2 \le m \le 1$

Figure 3 (a) shows the operation mode analysis on 3 and 2 using an interval $0 \le m \le 1/2$ in which the two-leg H-bridge inverter V_d fluctuates the voltage $V_i/2$ and 0 and causes the inductor current to rise. The equations derived under these conditions are as (1).

$$v_d = v_L + V_o$$
$$\frac{V_i}{2} = L\frac{di_L}{dt} + V_o$$
$$L\frac{di_L}{dt} = \frac{V_i}{2} - V_o$$

$$L\Delta i_L = \left(\frac{V_i}{2} - V_o\right)\Delta t = \left(\frac{V_i}{2} - V_o\right)t_1 \qquad (1)$$

When the voltages on the two-leg H-bridge, the inverters have zero values, thereby leading to a decrease in inductor current. The equations that can be derived under these conditions are as (2).

$$\begin{aligned} v_L &= V_o - v_d \\ L\frac{di_L}{dt} &= V_o - 0 \\ L\Delta i_L &= V_o\Delta t = V_o t_2 \end{aligned} \qquad (2)$$

Substituting (1) into (2) formulates (3).

$$V_o = \frac{V_i}{2}\frac{t_1}{T_{out}} = \frac{V_i}{2}\frac{2t_{on}}{T_s} = mV_i \qquad (3)$$

Figure 3 (b) shows the analysis of operation mode on 1 and 2 using an interval $1/2 \le m \le 1$, thereby causing the two-leg H-bridge inverter V_d to fluctuate the V_i and $V_i/2$ voltages. This increases the inductor current and the equations derived are as (4).

$$\begin{aligned} v_d &= v_L + V_o \\ V_i &= L\frac{di_L}{dt} + V_o \\ L\frac{di_L}{dt} &= V_i - V_o \\ L\Delta i_L &= (V_i - V_o)\Delta t = (V_i - V_o)t_1 \end{aligned} \qquad (4)$$

The voltages on two-leg H-bridge inverters are $V_i/2$ and leads to a decrease in the inductor current. The derived under these conditions are as (5).

$$\begin{aligned} L\frac{di_L}{dt} &= V_o - \frac{V_i}{2} \\ L\Delta i_L &= \left(V_o - \frac{V_i}{2}\right)\Delta t = \left(V_o - \frac{V_i}{2}\right)t_2 \end{aligned} \qquad (5)$$

Substituting (4) into (5) formulates (6).

$$V_o = \frac{V_i}{2}\frac{2t_{on}}{T_s} = mV_i \qquad (6)$$

Operation mode 2 need to be applied to keep the voltage capacitor constant, as shown in Figure 2 (b) and Figure 2 (c). The decrease in voltage across the DC capacitor indicates the power given to the load, as shown in Figure 2 (c). The increase in capacitor voltage at DC indicates power absorption from the power source (E), as shown in Figure 2 (b). Therefore, to ensure the increase and decrease in power, the capacitor voltage needs to be kept constant, as shown in Figure 4.

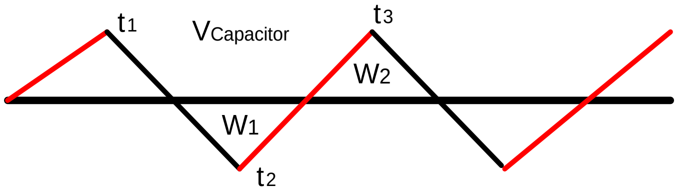


Figure 4. The charging and discharging voltage across capacitor

The capacitor transmitted power to load at an interval of $t_1 - t_2$, thereby decreasing the capacitor voltage. The amount of energy is expressed (7).

$$W_1 = \int_{t_1}^{t_2} P(t)dt \tag{7}$$

This interval produces a voltage across the capacitor known as V_{cap1}. The capacitor absorbed power from the source (E) at an interval of $t_2 - t_3$, thereby increasing the capacitor voltage. The amount of energy is expressed by (8).

$$W_2 = \int_{t_2}^{t_3} P(t)dt \tag{8}$$

This interval would produce a voltage across the capacitor known as $V_{cap\,2}$. The balancing power used the mode of operation 2, therefore the capacitor's energy is derived as (9).

$$W = W_1 = W_2 \tag{9}$$

The capacitor voltage is obtained using the (10).

$$\begin{aligned} &V_{cap1} > V_{cap\,2}\,, \\ &V_{cap\,3} > V_{cap\,2}\,, \\ &V_{cap1} = V_{cap3}\,. \end{aligned} \tag{10}$$

The delivery energy process causes voltage fluctuations in the capacitor as (11).

$$\Delta V = V_{cap2} - V_{cap1} \tag{11}$$

The capacitor was capable of storing energy with an increase and decrease in voltage as obtained using (12).

$$\begin{aligned} &W = \frac{1}{2}C(\Delta V)^2 \\ &W = \frac{1}{2}C(V_{cap2} - V_{cap1})^2 \end{aligned} \tag{12}$$

A capacitor voltage in a balanced condition is needed for a FCDCDC-HBI inverter, with the equilibrium energy determined by the charging and discharging of the power active switches based on the mode of operation 2. This has the ability to store energy in the capacitor that equals those in the inductor. The value of the capacitor can be determined as (13).

$$\begin{aligned} &W_C = W_L\,, \\ &C = \frac{L\,\Delta I^2}{\Delta V^2} \end{aligned} \tag{13}$$

The (3) and (6) show the relationship between the output and input voltage of the conventional and multilevel inverter (FCDCDC-HBI). The five-level waveform is based on the FCDCDC-HBI and the proposed scheme of the SPWM control, as shown in Figure 5 and Figure 6.

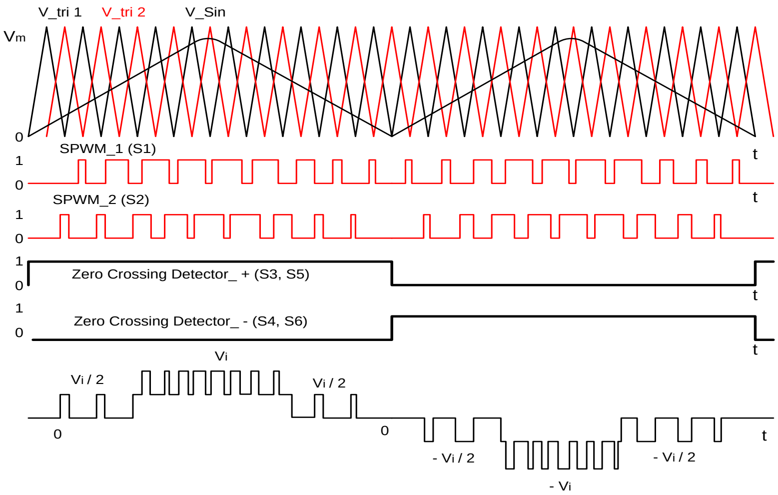


Figure 5. The waveform of the five-level based on FCDCDC-HBI

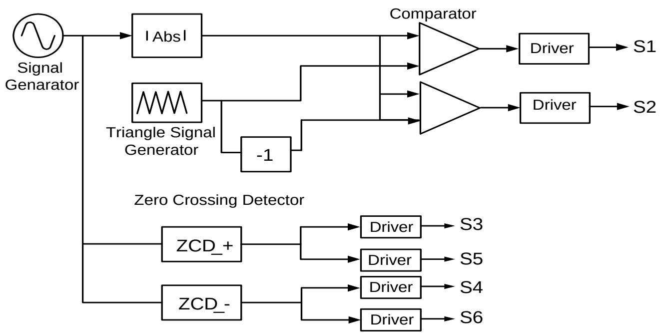


Figure 6. The proposed scheme of a SPWM control

3. RESULTS AND DISCUSSION

The proposed FCDCDC-HBI was verified using the Power Simulator Software and implemented on a prototype scale. Table 1 shows the parameters used as well as the proposed control scheme implemented using an Arduino Mega 2560 microcontroller. Furthermore, MOSFET IRFP 460 and MUR 1560 were used as the active and passive power switches of the FCDCDC-HBI. Meanwhile, B1212S-1Ws and TLP 350s were used as an isolated DC-DC converter and active power switch drivers. The prototype for experimental works is shown in Figure 7.

Table 1. Parameters for the validation works

Parameters	Value
Input Voltage	100 Volt DC
Resistive Load	25 Ohm
Capacitor	470 uF/450V
Inductor Filter	2.5 mH
Operated frequency	5 KHz

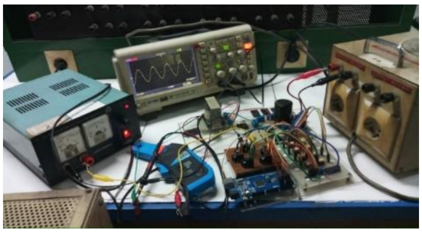
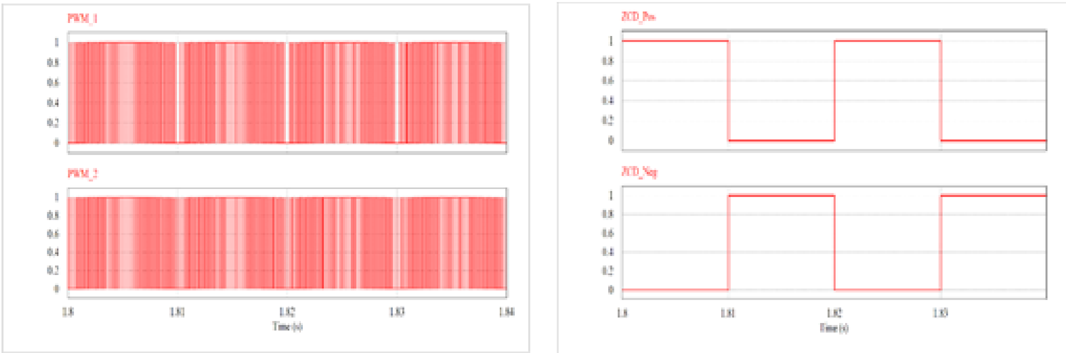


Figure 7. The prototype for experimental works

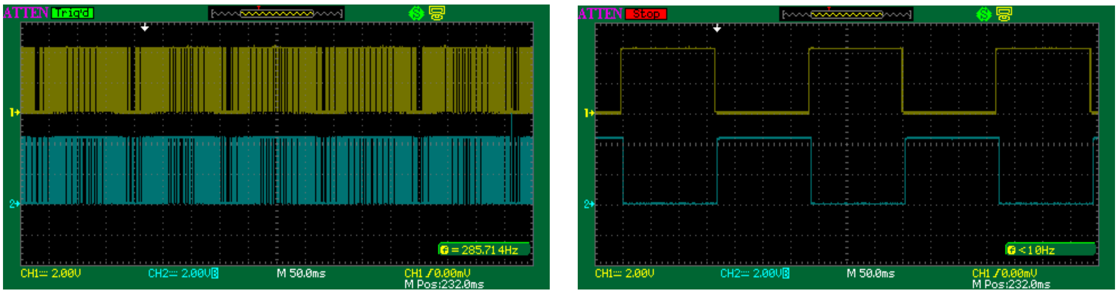
The initial stage of verification is carried out by computational simulation. Figure 8 (a) shows the simulation result of an absolute SPWM gating signal used to power switch *S1* and *S2*. An absolute SPWM gating signal shifts 180^0 between SPWM on *S1* and *S2*. Figure 8 (b) shows a pulse shaper polarity inverted (zero-crossing detector) at 50Hz, which is used to switch *S3-S5* (positive cycle) and *S4-S6* (negative cycle). Furthermore, the power switch *S1* and *S2* used a high frequency of 5KHz, while those on *S3-S5* and *S4-S6* were low. These conditions (SPWM and zero-crossing detector waveform) are similar to the diagram shown in Figure 4.



(a) (b)

Figure 8. Simulated waveforms, (a) SPWM signal: *S1* and *S2*, (b) zero-crossing detector signal: S5 - S8 and S6 – S7

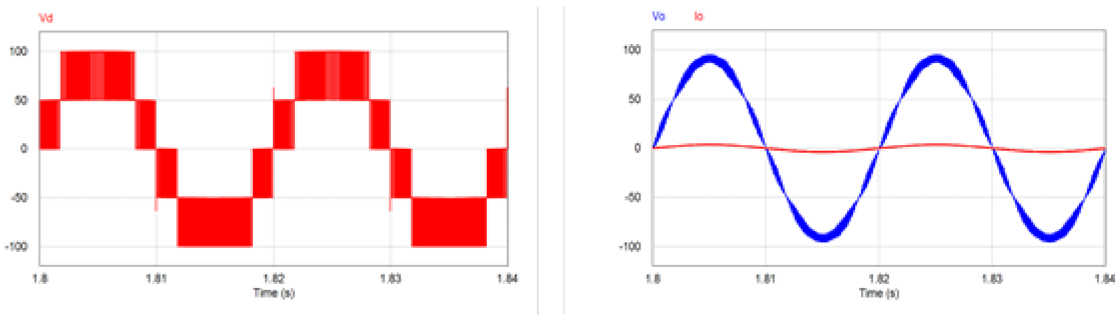
After ensuring that the *S1 - S6* switching pattern is properly running, the next step is to verify the proposed scheme of a SPWM control, which is implemented through the Arduino Mega 2560 microcontroller. Figure 9 (a) shows the implementation result of an absolute SPWM used to power switch *S1 and S2* with a high switching frequency of 5KHz. Figure 9 (b) shows the polarity inverter with zero-crossing detectors of 50Hz used to switch *S3-S5* and *S4-S6.* Therefore, SPWM (Figure 8 (a) and Figure 9 (a)) and zero-crossing detectors (Figure 8 (b) and Figure 9 (b)) resemble each other.



(a) (b)

Figure 9. Implemented waveforms, (a) SPWM signal: *S1* (yellow) and *S2* (blue), (b) zero-crossing detector signal on *S5 - S8* (yellow) and *S6 – S7* (blue)

The proposed FCDCDC-HBI topology shown in Figure 1 is used to simulate a SPWM control scheme, as indicated in Figure 5. Furthermore, Figure 10 (a) shows the simulation result of the five-level inverter voltage output waveform (switching operation on the interval $0 \leq m \leq 1$). The magnitude voltage levels were at +100V, +50V, 0V, −50V, and −100V. Meanwhile, the magnitude of the five-level inverter was related to the switching operation in (3) and (6), thereby minimizing the voltage harmonics by enlarging the filter inductor or switching frequency as shown in Figure 10 (b). Figure 11 shows the simulation result of the three-level inverter voltage output waveform (switching operation on the interval $0 \le m \le 1/2$). The magnitude voltage levels were at +50V, 0V, and −50V, respectively, which were also used to obtain the induced filter's fundamental value. The magnitude of the three-level inverter was related to the switching operation in (3).



(a) (b)

Figure 10. Simulated waveform, (a) inverter output voltage on the interval $0 \le m \le 1$, (b) the fundamental voltage and current output of the inverter

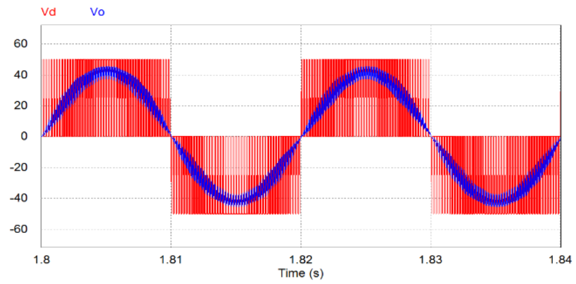
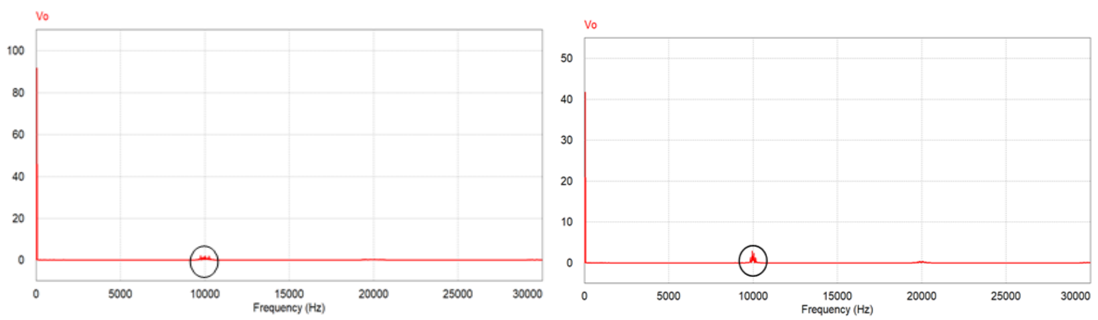


Figure 11. Simulated waveforms: inverter output voltage on the interval $0 \le m \le 1/2$

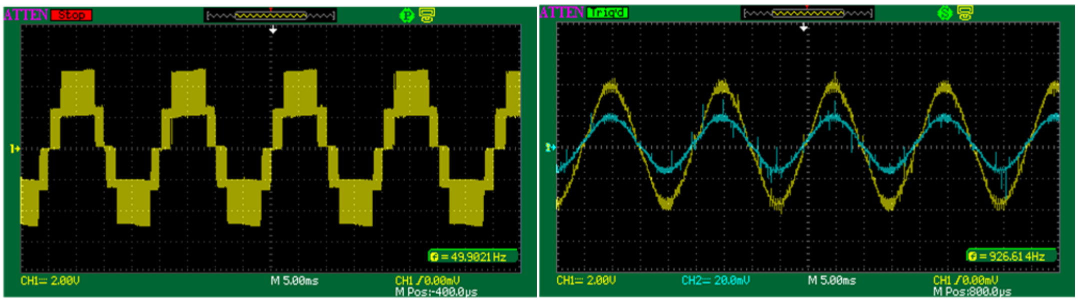
Figure 3 shows the analyses of the switching frequency operation on interval $0 \le m \le 1/2$ and $1/2 \le m \le 1$. It indicates that in one switching period there are two patterns, namely *S1* and *S2*. This method makes double switching frequency (5KHz become 10KHZ), with the output voltage waveforms in Figure 10 (b) and Figure 11 extracted using a Fast Fourier Transform (FFT) as shown in Figure 12. The frequency spectrum becomes 10KHZ at a switching frequency of 5KHZ. The advantage associated with this method is in terms of the size of the inductor filter used.



(a) (b)

Figure 12. The frequency spectrum, (a) voltage output waveform on the interval $0 \le m \le 1$, (b) voltage output waveform on the interval $0 \le m \le 1/2$

The final stage of this verification is to conduct prototype tests of the proposed single-phase five-level inverter. In these tests, the switching operation on the interval $0 \le m \le 1$ is performed to get five levels. Figure 13 (a) shows that the FCDCDC-HBI inverter is capable of producing five levels of output voltage levels, namely 100V, 50V, 0V, −50V, and −100V in a waveform. It also shows that the inverter output voltage of Figures 10 (a) and Figure 13 (a) resemble each other. The five-level inverter voltage output waveform has a good balancer using a phase-shifted carrier signal 180^0 as recommended in the proposed scheme of a SPWM control (Figure 5). Finally, Figure 13 (b) shows the implementation result of five-level inverter voltage and current output waveform after filtering using a 2.5mH inductor.



(a) (b)

Figure 13. Implemented waveform, (a) inverter output voltage on the interval $0 \le m \le 1$, (b) output current (blue) and voltage (yellow)

The performance of the FCDCDC-HBI inverter using simulation and implementation resemble each other, as shown in Figure 13. Furthermore, it is important to balance the voltage of a flying capacitor DC-DC converter in controlling the multilevel inverter due to its ability to control switches *S1* and *S2* easily using a phase-shifted triangular carrier (180^0) without any combinational logic gate. The zero-crossing detector of the H-bridge inverter has the ability to control switches *S3-S5* (positive cycle) and *S4-S6* (negative cycle) at 50Hz.

4. CONCLUSION

The multilevel inverter topology presented in this research depends on the three levels DC-DC converter (FCDCDC) and polarity generators (HBI). The research showed that a proposed five-level inverter based on FCDCDC-HBI topology has more advantages in terms of equilibrium voltage on the capacitor, simple control, and cost-effectiveness. Furthermore, the new system is ideal for sustainable power based on a single-stage delivery technique. An absolute SPWM for the FCDCDC requires no voltage balancer in the capacitor and combinational logic gate. The proposed topology effectively operates as a five-level inverter with a novel modulation strategy.

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