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A single-stage full bridgeless boost half-bridge AC/DC converter with bidirectional switch

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ABSTRACT

This paper proposed an isolated full bridgeless single stage alternating current-direct current (AC-DC) converter. The proposed converter integrates the operation of a pure bridgeless power factor correction with input boost inductor cascaded with center-tap transformer and half bridge circuit. In addition, the bidirectional switch can be driven with single control signal which further simplifies the controller circuit. It was proven that this converter reduced the total number of components compared to some conventional circuit and semi-bridgeless circuit topologies. The circuit operation of the proposed circuit was then confirmed with the small signal model, large signal model, circuit simulation and then verified experimentally. It was designed and tested at 115 Vac, 50 Hz of input supply, and 20 Vdc output voltage with maximum output power of 100 W. In addition, the crossover distortion at the input current was minimized at high input line frequency.

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1. INTRODUCTION

In the past, power factor correction schemes have been implemented mainly for heavy industrial load. However, nowadays, the usage of electronic equipment has increased drastically. The energy efficiency rating and symbol like "Energy Star" has gain consumer attention which demand less harmonic, high power factor and higher efficiency system. This trend has made the power factor correction (PFC) becomesa significantly important aspect even for low power electronic equipment. Conventionally, a switch mode power supplies (SMPS) consist of rectifier followed by a DC-DC converter [1]-[5]. For example, the conventional AC-DC half bridge converter can be depicted in Figure 1 (a). The prefrontal cortex (PFC) function is interposed between the input rectifier bridge and the DC-DC converter. The rectifier bridge circuit converts the AC source to unregulated DC which is normally an absolute value of the sinusoidal voltage. In the typical two stage structure, the front-end PFC is used to shape the input current. The downstream DC-DC converter provides control and isolation (for DC-DC converter with isolation) which then regulates the DC output. It is found that the two stages schemes demonstrate excellent performances in power factor, total harmonic distortion (THD) and output voltage responses [6]. However, it requires high component counts and complex control circuit [6]. Another major drawback is bulky DC link capacitor that filter power fluctuations. The high current flowing to the DC link capacitor also leads to significant power loss, consequently reduce its lifetime leading to capacitor failure [7], [8]. The single stage scheme which integrates the PFC and the DC-DC converter on the other hand leads to a low complexity and reduce cost [6]-[13] but,

the single stage schemes with DC link capacitor suffers adrawback when high input current flow to the DC link capacitor [14]-[17]. There is no big issue on the number of current flows to DC link capacitor for the low power applications. However, the input bridge diodes in single stage converter cause significant conduction losses and requires additional heat management. To overcome this drawback, a single stage bridgeless converter has been introduced. This bridgeless technique integrates the rectifier stage with the high frequency converter, eliminating the full bridge rectifier, allowing considerable reduction in conduction losses [18]. Furthermore, it reduces the number of components thusimprove the power conversion efficiency.

Due to the safety of end users, the products with galvanic isolation are in demand, especially for consumer products. This feature is also one of the considerations in the international electrotechnical commission (IEC) standard that requires electrical isolation in the products [19]. Thus, bridgeless converter with transformer is one of the choices to produce power supply, which provides safety through isolation. One of the drawbacks of having transformer are lowering down the power factor and efficiency. However, this can be minimized by carefully considering the factors that affect transformer efficiency. In addition, other factors that contribute to better performances must be considered. This includes component counts, component material, switching techniques, circuit topologies, and control techniques at significant cost.

The flyback bridgeless AC-DC isolated converter topology is the most reported for low output power application due to its simplicity. The back-to-back flyback allow the full operation of the power conversion at both positive and negative half cycle input [20]-[21]. The back-to-back flyback topology [20] is equipped with two slow rectifier diodes which suppressed the common mode (CM) electromagnetic interference (EMI) noise. However, the components count will be high and hence, the cost increases. With the back-to-back active switch's connection, only one unit of flyback converter is required for the full supply input cycle operation [21] which has low component count. Consequently, switching losses will also decrease. These initiatives improve the converter efficiency compared to the ac-dc converter with back-to-back flyback topologies. The power switches however suffer inrush current and circulating energy between transformer leakage inductance and primary switch parasitic capacitance [22]. Thus, it requires higher rating power switches. Therefore, the flyback topology is suitable for low power range. The integration of input or boost inductor [23], [24] slows down the inrush current and also contributed in shaping the input current. Furthermore, the usage of inductor with common core reduces the size and consequently reduce the cost. Either low power or high-power output, combination with boost inductor [24]-[28] at the input side will contribute to high power factor and improve efficiencies. The input current which continuously flow in each mode of circuit operation [24]-[28] will minimize the deterioration of the input current and in return, high input power factor can be achieved. Further improvement with resonance circuit [29] contributes to converter efficiency. There is no excess current or voltages because it diverted to resonance circuit.

The combination of boost half bridge bridgeless converter [25], [26], [28], [31] is suitable for medium power output. The proposed circuit in [25], [26], [28] are the combination of bridgeless boost and asymmetrical half bridge converter. The proposed boost-half bridge topology in [26] uses two unit of transformers. These transformers allow the mode of circuit operation for completed full cycle of input voltage. However, the proposed topologies in [28] only use one unit of transformer. Thus, reduce parts count and weight. In addition, the zero-voltage switching is achieving with the resonant tank circuit [28]. There are two slow diodes at the input side. Slow diodes will have reverse recovery issue which significantly reduce the energy conversion efficiency. However, the losses due to slow diodes in [28] is smaller as compare to the conventional bridge rectifier. Therefore, an improvement of the conversion efficiency is expected because of a smaller number of slow diodes, power switches operating at zero voltage switching (ZVS) and a smaller number of components conducted at each mode of circuit operation.

The proposed circuit in [31] is the ac-dc bridgeless based on half bridge topology without resonance circuit. It achieves high power factor over the load range. Thus, it also meets the qualifying round of electric power supply which require to have a true power factor 0.9 or more in any measured condition where the input power is equal or greater than 100 Watts at full load [32].

In this paper, an isolated pure bridgeless half bridge AC-DC is proposed. The converter performs direct conversion and at the same time provides isolation without full bridge diode. The idea of the proposed converter is based on the primary side [32] but without bridge diodes which further eliminate the line frequency rectifier losses. Figure 1 shows the comparison of the conventional in Figure 1 (a) and proposed in Figure 1 (b) circuit topologies. In addition, it improves the crossover distortion of input current at voltage supply with high frequency. Therefore, the proposed circuit topology can be applied on power system with higher frequency. The bidirectional switch concept is derived from the topologies in [22], [23]. It allows the circuit operation at positive and negative half cycle of input voltage with reduced number of components. In addition, simple control circuit is expected sinceonly one control circuit is required. The circuit diagram of the proposed converter is shown in Figure 1 (b) while the circuit operation at positive half line cycle input voltages shown in Figure 2. The center-tapped features allow the operation at both positive and negative

input cycle with single transformer. The combination of boost inductors and half bridge contribute to shaping the input current. The boost inductor working in continuous conduction mode (CCM), reshapes the input current waveform to near sinusoidal and in phase with the input voltage. Hence, it is expected high input power factor can be achieves. The circuit operation at negative half cycle input voltage is symmetrical to positive half cycle input voltage. Thus, the circuit operation becomes simpler. Symmetrical circuit operation needs less control signal in one full cycle. The control signal at negative half cycle is similar with the positive half cycle control signal. The number of components of the proposed converter has been reduced compared to the conventional AC-DC converter. The performance of proposed converter is verified by PLECS/Simulink at 100 W (20 V/5 A) with input voltage of 115 Vrms and verified experimentally.

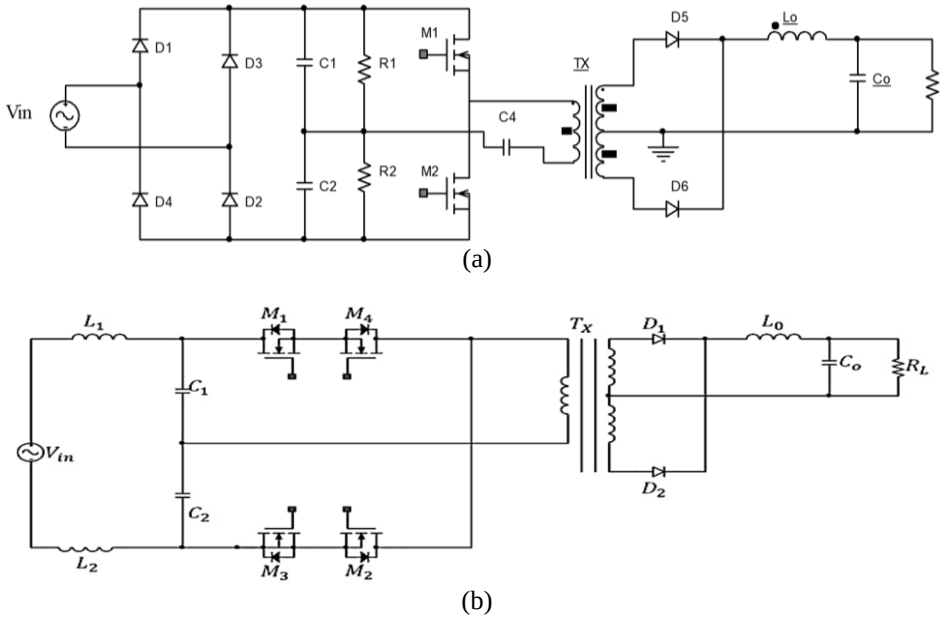


Figure 1. These figures are, (a) conventional AC-DC half-bridge, (b) proposed AC-DC full bridgeless half-bridge with bidirectional switch

2. CIRCUIT OPERATION

Figure 1 (b) shows the proposed bridgeless half bridge converter. Figure 2 shows the active devices during one full cycle of input supply. All passive elements operated at full cycle of input supply except the active switches. Switches $M_1$and M_2active during positive half cycle of input voltage as depicted in Figure 2 (a) while M_3, and M_4 switches operated at negative half cycle of input voltage as shown in Figure 2 (b). Figure 3 shows the circuit operation during positive half cycle of input voltage and the key waveforms as depicted in Figure 4. Analysis is carried out only at positive half line input voltage. This is due to the exact same equivalent circuit during positive and negative half-line cycle. The inductors in the proposed circuit will operate in CCM. Circuit averaging method will be implemented to obtain the small signal model and steady state model for the proposed converter. No input current sensor is used. This is to observe the input power factor of the propose circuit itself without current shaping control. Therefore, only output voltage control is required.

The high frequency model is developed based on the operation of the proposed circuit at each switching period. The magnitude of the sinusoidal input voltage varies from zero to peak and zero again for 180^0half-line input cycle. However, the magnitude of input voltage V_{in} is assume to be constant within the switching period. The switching frequency is much higher compared to line frequency. Therefore, the magnitude looks constant at each switching period.

Through the circuit simulation in Simulink, it is found that four (4) modes of operation have been identified as shown in Figure 3. The first subinterval namely mode 1, followed by mode 2, mode 3, and mode 4. The duty cycles of each sub interval are known as d_1, d_2, d_3, and d_4. The equivalent circuit for each mode is shown in Figure 3. Figures 3 (a)-(d) show the circuit operation during positive half cycle of input voltage.

The two input inductors L_1 and L_2 will slow down the rise of input current (inrush current) and as a boost inductor. Consequently, it reduces the peak current when the switches ON and hence, reduce losses and

the current rating for the power switches. As shown in Figure 3 (a) and 3 (c), switch M_1 is the main power switch for positive half cycle of input voltage while switch M_3 is the main switch at negative half cycle of input voltage. In mode 2 and mode 4, all switches are in off state as depicted in Figure 3 (b) and 3 (d). However, the input current continuously flows through a circuit loop of boost inductor and half bridge capacitor. Switch M_2 and M_4 will operate at mode 3 which allow the input current to flow continuously (boost mode) and charge/discharge the half bridge capacitor C_1 and C_2. Therefore, it can be seen that the input current flow continuously through the circuit in all modes of operation. Transformer T_X with secondary center-tapped transfer the energy to the load. Diode D_1 and D_2 will rectified the energy flows from the secondary center-tapped transformer. Inductor L_o and capacitor C_o work as low pass filter by assuming that big value of output capacitor C_o is used in this analysis. Only the operation at positive half cycle will be discussed due to symmetrical operation at negative half cycle of input voltage. In the proposed circuit analysis, it is assumed that all components and switches are ideal.

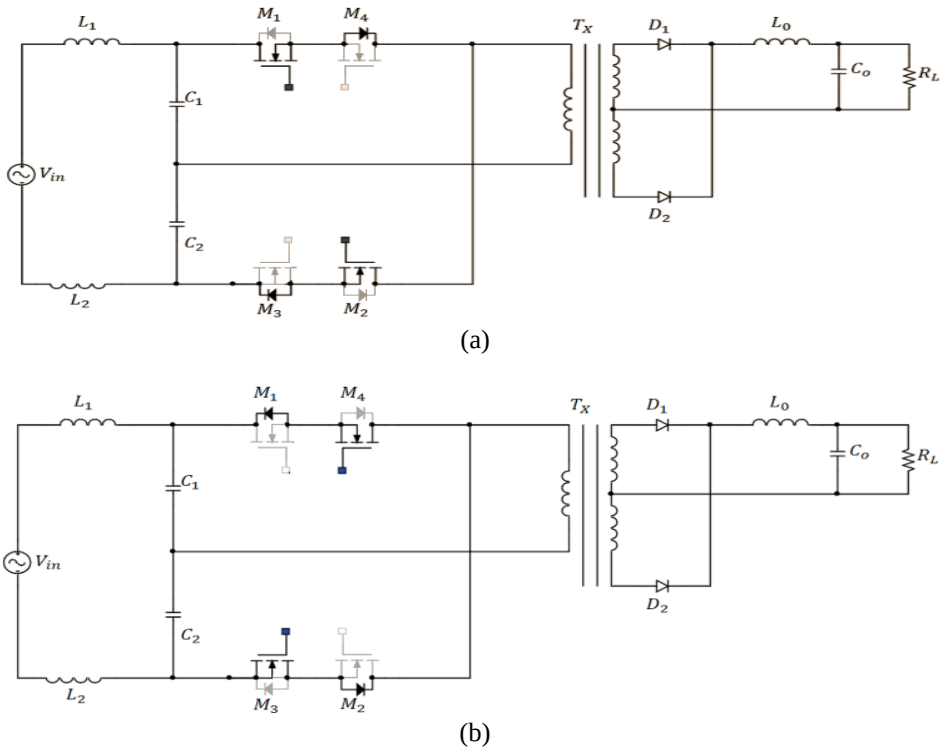


Figure 2. Active devices at input voltage, (a) positive half cycle, (b) negative half cycle

At mode 1 $(t_0 \sim t_1)$ or $d_1 T_S$, switch $M_1$is turn ON. At initial condition, assume that the current at input inductor L_1 and L_2 is at maximum and capacitor C_1 is fully charged. The input current i_{in} and boost inductor current flow to the primary winding of transformer. The half bridge capacitor C_1 is discharging while capacitor C_2 is in charging mode. The sum of i_{in}, i_{L1} and i_{C1} current flows through switch M_1 and body diode of switch M_4 to the primary winding of the transformer as shown in Figure 3 (a). The transformer primary current I_p flows to the half bridge capacitor $C_2$and charge capacitor C_2. Next, current flow from capacitor C_2 will flow to boost inductor L_2 and flow back to the source to complete a closed loop path of the circuit. On the other hand, the flux flow through the transformer core and e.m.f induced in the secondary winding of the transformer, T_X. Diode $D_1$is in forward bias. Secondary current will flow out to the output filter L_o and to the load R_L. At initial, inductor current i_{Lo} is assume to be minimum and output capacitor C_o is fully charge.

At mode 2 $(t_1 \sim t_2)$ or $d_2 T_s$, the power switches at primary side is in OFF state. Therefore, the input current flows to boost inductor L_1 and L_2 and half bridge capacitor C_1 and C_2 as depicted in Figure 3 (b). At t_1, the boost inductor current is at minimum. Thus, the boost inductor charge linearly by the input voltage V_{in}. The C_1 is in discharging mode and C_2 was in charging mode at end of the mode 1. Therefore, the half bridge capacitor C_1 charge linearly by the input voltage. The half bridge capacitor C_2 also in charging mode. However, the voltage magnitude of capacitor C_2 is close to V_{in}. Thus, capacitor C_2 is fully charged at the end

of mode 2 interval. At secondary side of transformer, output inductor L_o and capacitor C_o discharge to the load R_L.

At mode 3 $(t_2 - t_3)$ or d_3T_s; switch M_2 is turned ON as depicted in Figure 3 (c). The boost inductor L_1 and L_2 is in discharging mode and flow to half bridge capacitor C_1. Thus, capacitor continues to charge from mode 2 until end of mode 3. At the end of mode 2, half bridge capacitor C_2 is fully charged. Therefore, in this mode, the half bridge capacitor C_2 is in discharging mode. The primary current i_p, flows to switch M_2 and body diode M_3. The sum of half bridge capacitor current i_{c2} and primary current i_p flow to the boost inductor L_2 and back to the source.

At mode 4 $(t_3 - t_4)$ or d_4T_s; the power switches at primary side is in OFF state. The equivalent circuit is as depicted in Figure 3 (d). The input current flows to boost inductor L_1 and L_2 and half bridge capacitor C_1 and C_2. At t_3, the boost inductor current is at minimum. Thus, the boost inductor charged linearly by the input voltage V_{in}. This is the same as the operation in mode 3. However in mode 4, the half bridge capacitor C_1 is in charging mode and C_2 is in discharging mode at end of the mode 3. Therefore, the half bridge capacitor C_1 charged linearly by the input voltage. The half bridge capacitor C_2 also in charging mode. However, the voltage magnitude of capacitor C_1 is close to V_{in}. Thus, only capacitor C_1 is fully charged at the end of mode 2 interval. At secondary side of transformer, output inductor and capacitor L_o and C_o discharged to the load R_L. However diode D_2 is in forward bias and diode D_1 is in OFF state.

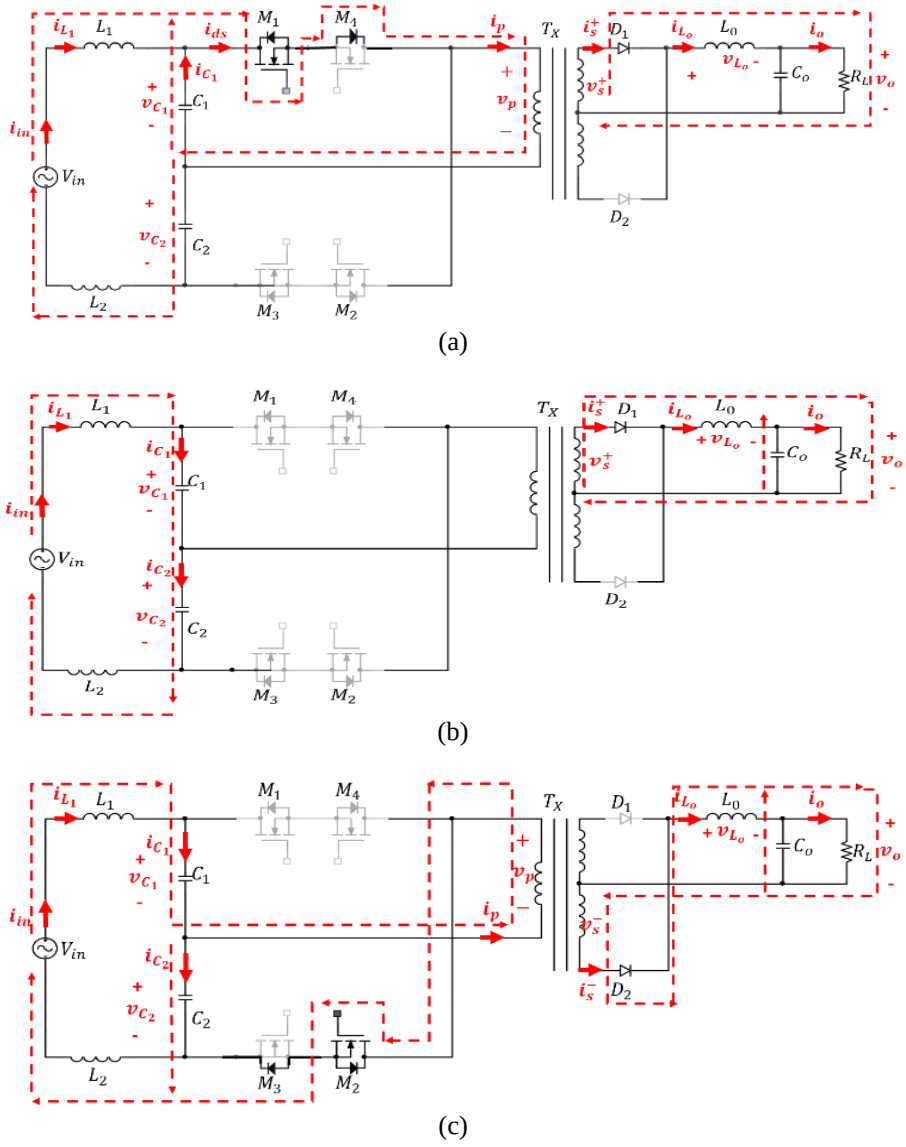
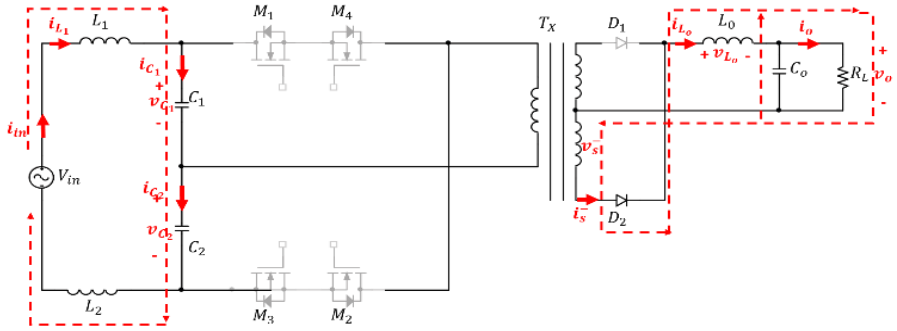


Figure 3. Circuit operation at positive half-cycle of input voltage, (a) mode 1, (b) mode 2, (c) mode 3



(d)

Figure 3. Circuit operation at positive half-cycle of input voltage, (d) mode 4 (*continue*)

It is observed that the input current and boost inductor current continuously flows at each mode of operation. Thus, the boost inductor current working in continuous conduction mode (CCM) which consequently minimize the distortion of input current. This will achieved high input power factor.

3. DESIGN CONSIDERATION AND EXPERIMENTAL SETUP

The specification of the proposed converter is shown in Table 1. The calculated duty cycle at full load condition is 0.39. However, the calculated duty cycle is free from the load variation. Thus, the duty cycle determined from calculation is an average duty cycle that shows input and output voltage conversion ratio. Obviously, higher duty cycle is required for higher load vice versa. Thus, Figure 4 shows the variation of duty cycle at 20% load to full load.

The design of the transformer is derived based on the geometric constant k_{gfe} method [33]. The ferrites 3C90 grade is used as preferred material applied for power transformer [34]. The pre-determined core shape is based on the provided typical power handling chart [35]. However, the boost inductor is designed based on the k_g method [33].

The control circuit parameters are determined based on the obtained steady state equation. The voltage follower control method is used to verify the operation of the proposed converter in circuit simulator and experimentally. This control method is used to regulate the output voltage to the desired value. Thus, the controller is expected to provide the appropriate duty cycle for changes in any load.

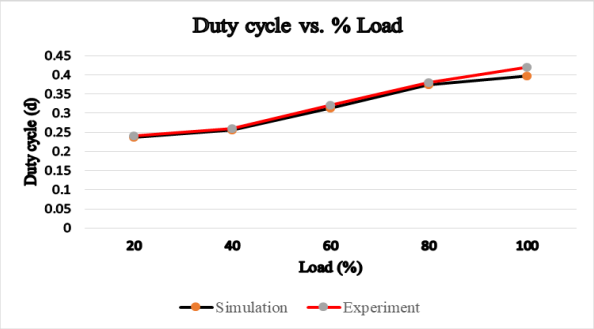


Figure 4. Duty cycle versus load

Table 1. Proposed circuit parameters

Parameters	Values
Input voltage, V_{in}	115 Vrms
Input line frequency,	50 Hz
Switching frequency, f_S	50 kHz
Output voltage, V_O	20 V DC
Nominal output power, P_O	100 W
Output voltage ripple, ΔV_{CO}	≤ 2 V
Boost inductor L_1, L_2	500 µH
Inductor L_o	100 µH
Capacitor C_1, C_2	0.1 µF
Capacitor C_o	10 mF
Mosfet	IPP60R080P7XKSA1
Diode	STPS20H100CT

4. RESULTS

The proposed circuit mode of operation was verified by observing the switching waveforms and compared it with the simulation results. Figure 5 shows the switching waveform from the circuit simulation. The switching waveform obtained from the experiment is depicted in Figure 6. The simulation and experimental gate to source voltage V_{gs} for MOSFET M_1 and M_2 are shown in Figure 5 (a) and Figure 6 (a). It also shows a very good agreement of voltage across the switch M_1 and current flows trough switch M_1 both simulation and experimental as depicted in Figures 5 (b)-(c) and Figures 6 (b) (i), (ii). In addition, the

transformer primary side current and voltage are shown in Figures 5 (d)-(e) for simulation and Figures 6 (c) (i), (ii) experimentally. Thus, the circuit mode of operation wasvalidated.

The simulation and experimental input current slope at line frequency 50 Hz are illustrated in Figure 7 (a) and Figure 7 (b). It can be seen that the waveform enveloped of the input current is sinusoidal and in phase with the input voltage. It was observed that, the highest power factor was obtained at full load condition. Additionally, the input current was also in phase with the voltage supply at line frequency of 500 Hz as depicted from simulation result in Figure 8 (a) and Figure 8 (b) experimentally. It iwasfound that no zero crossing of input current at input voltage with efficiency higher than line frequency value. Thus, the proposed topology is also suitable to be used in a system which operates at frequency higher than the line frequency. The input current obtained from the experiment has good agreement to input current obtained from simulation.

The input current distortion (THD) analyzed governed by IEC 6100-4-7 which requires data acquisition in blocks of 200 ms with no gapped or overlap between the acquired data block [37]. Thus, total 10 cycles of input current were considered in measurement of input current harmonic. The harmonic current was compared with the IEC 6100-3-2 standard up to thirty ninth harmonic level as depicted in Figure 9. It was observed that the harmonic current of the proposed circuit topology meets the IEC 6100 -3-2 standard. The proposed circuit obtain THD of 11.35% experimentally and 9.27% in circuit simulation. This shows a good agreement between the simulation and experiment results where the small difference is acceptable. Additionally, the THD's is lower than conventional AC-DC half-bridge converter and AC-DC bridgeless topology [38]. Furthermore, the THD's comparison with [24], [31] is intangible.

The efficiency of the proposed converter is shown in Figure 10. It was observed that at full load condition, the maximum efficiency is 88.4% obtained in simulation and 82.64% experimentally. This fulfill level IV average efficiency requirement of IEC as AS/NZS 4665. Lower efficiency measured experimentally was mainly due to power loss at secondary side rectifier diodes. Generally, the power losses are proportional to the diode forward current. Thus, better efficiency is expected at smaller load current with the same output power. However, in overall, the proposed circuit topology showed an improvement of 2.54% efficiency at full load as compared to the conventional topology and better efficiency than conventional bridgeless AC-DC topologies as depicted in Figure 11. This improvement of efficiency was obtained by eliminating the bridge diodes.

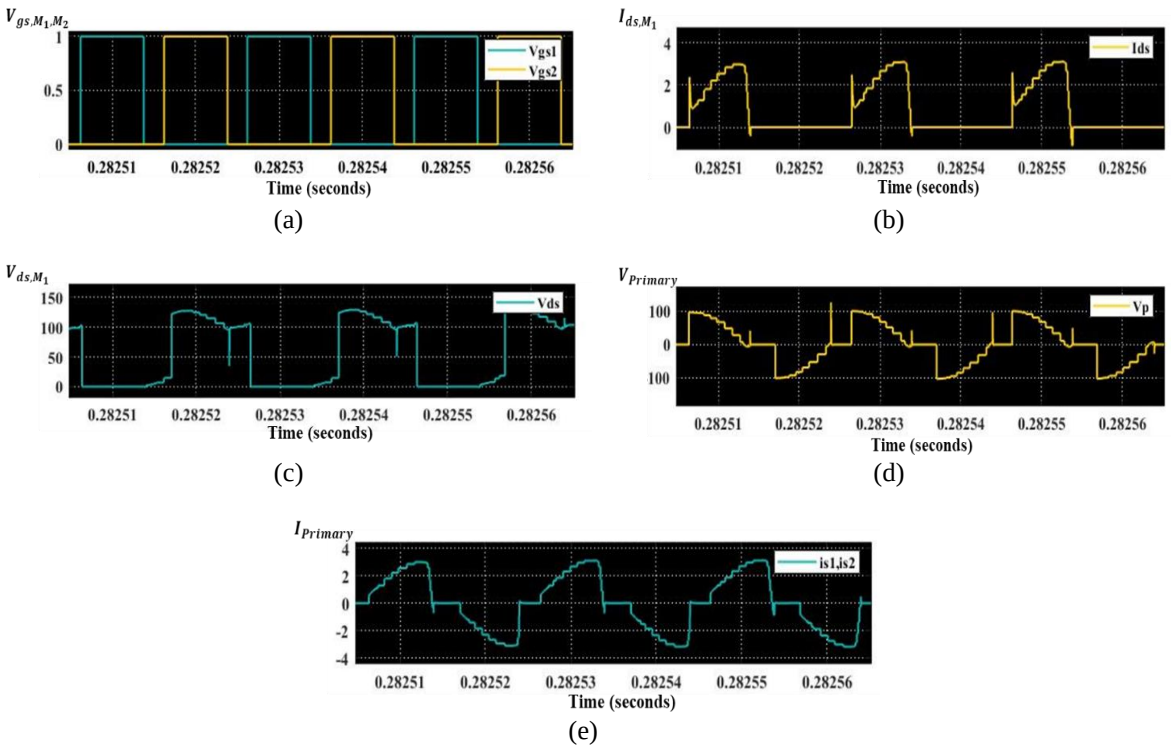


Figure 5. Simulation waveforms for, (a) V_{gs,M_1,M_2}, (b) I_{ds,M_1}, (c) V_{ds,M_1}, (d) transformer primary voltage, (e) transformer primary current

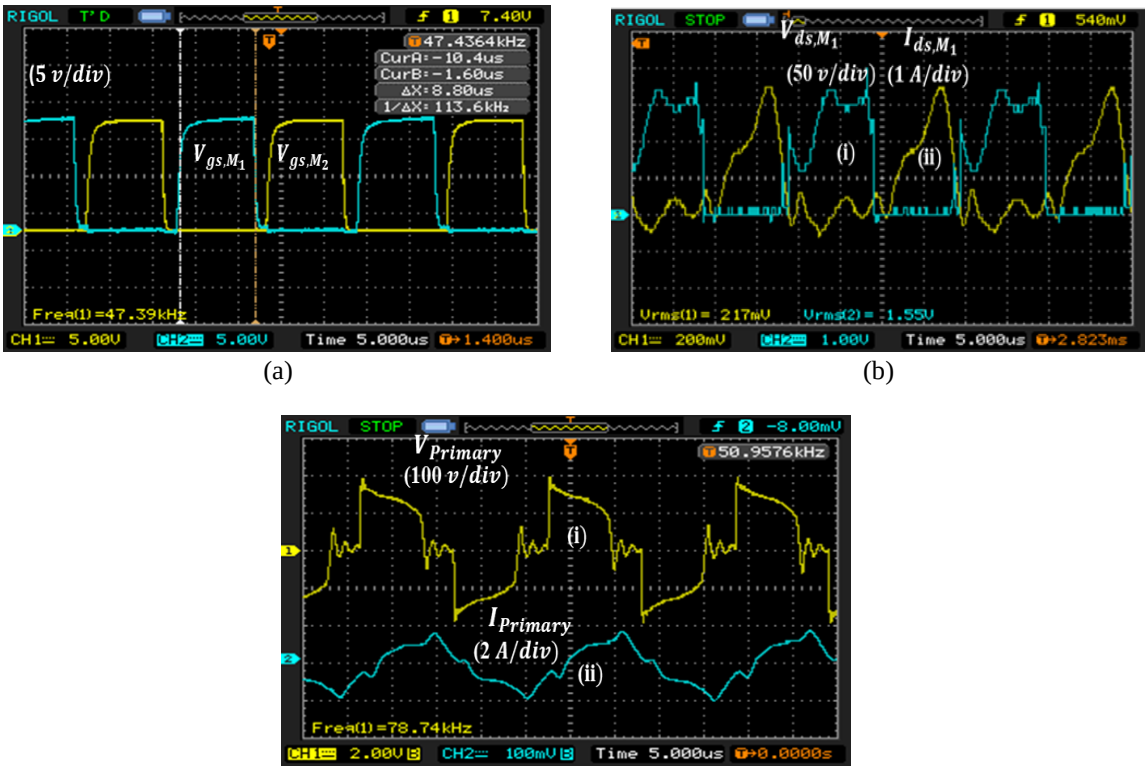


Figure 6. Experimental waveform for, (a) V_{gs,M_1,M_2}, (b) (i) V_{ds,M_1}, (ii) I_{ds,M_1}, (c) (i) transformer primary voltage, (ii) transformer primary current

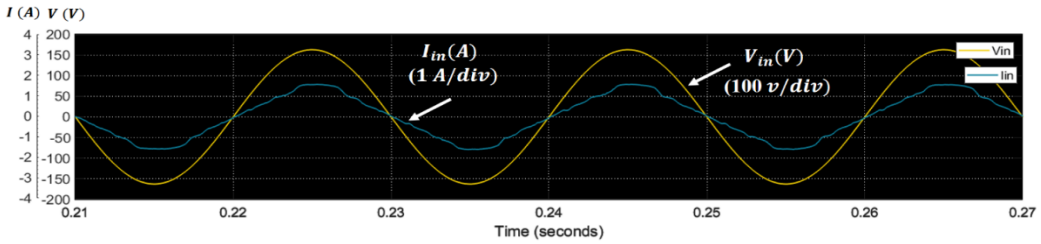
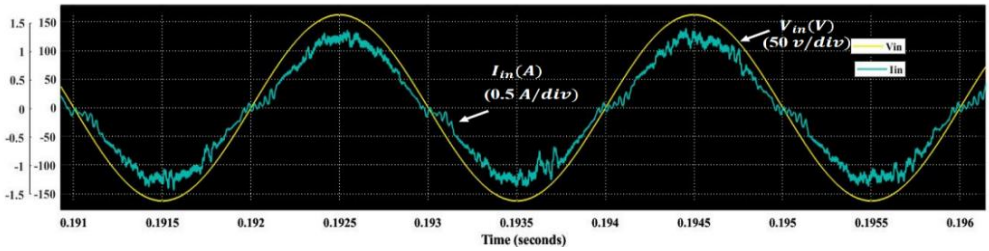
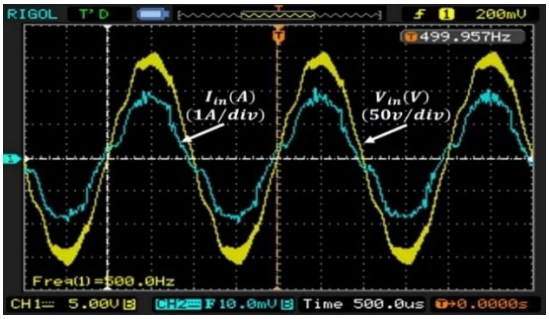


Figure 7. Input voltage V_{in} and current I_{in} at 50 Hz, (a) simulation, (b) experimental



(a)



(b)

Figure 8. Input voltage V_{in} and current I_{in} at 500 Hz, (a) simulation, (b) experimental

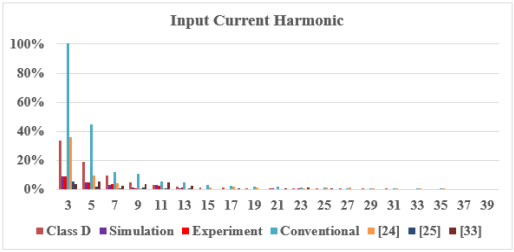


Figure 9. Input current harmonic spectrum compared with IEC 6000-3-2 standard

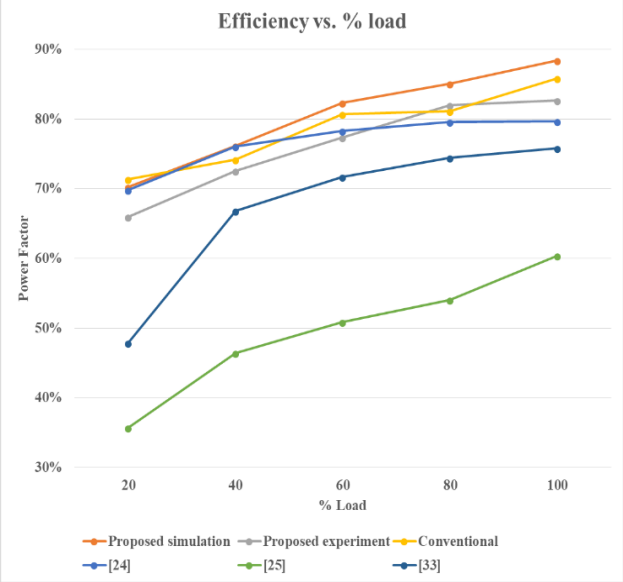


Figure 10. Power conversion efficiency

A breakdown of the power loss incurred at 100 W with 115 Vrms input voltage is shown in Figure 11. The calculated power losses were based on the waveform obtained from the experiment and equation [38]-[41]. Additionally, the theoretical data such as MOSFET $R_{ds(on)}$, Q_{rr} and diode forward voltage V_F was obtained from the product datasheet. The subscripts "sw" and "cond" represent the switching loss and conduction loss respectively. The MOSFET conduction loss is the smallest compares to the body diodes and secondary side rectifier. This is due to the device's characteristics which offer small $R_{ds(on)}$. It can be seen that the MOSFET body diode conduction loss dominated the primary circuit power losses. However, higher conduction loss occurred at secondary rectifier diode mainly due to the on-state current. The diode conduction loss proportional to the load current. Thus, it is expected to have better efficiency with higher output voltage at the same output power. Small switching losses of MOSFET is due to the MOSFET characteristic super junction principle with small Q_C which benefit to fast switching. Additionally, the sufficient dead time reduce the MOSFET turn-on losses. However, the secondary side rectifier diode dominated the overall power losses mainly due to the turn off switching losses. There are no turn-on losses because ZVS wasachieved.

The full load power factor is 0.99 and similar as compared to others AC-DC bridgeless topology. However, the proposed circuit topology achieves better input power factor compared to conventional AC-DC half-bridge converter. Figure 12 shows the comparison of power factor from light load to the full load. Table 2 shows that a smaller number of components in the proposed circuit topology as compared to the conventional AC-DC half bridge and some conventional bridgeless half bridge converter. If two MOSFET considered as one bidirectional switch, the total number of components in the proposed circuit topology becomes 11 components.

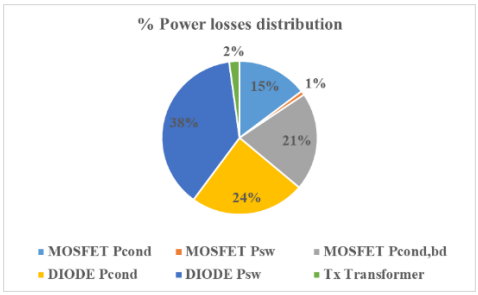


Figure 11. Breakdown of the power losses

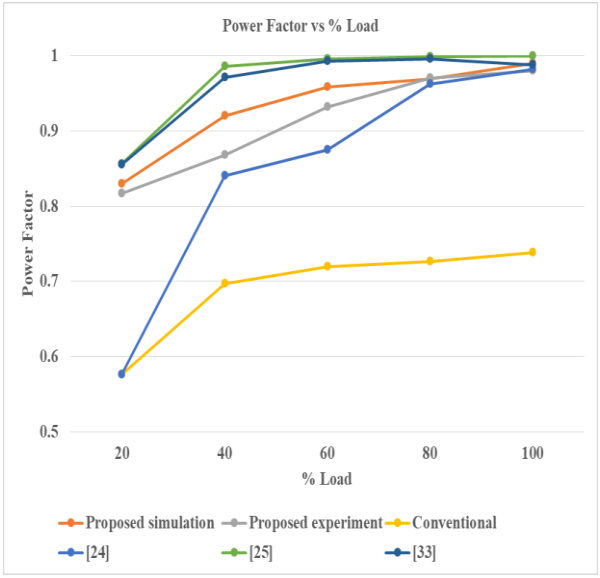


Figure 12. Input power factor

Table 2. Component counts

Reference number	Diode	Inductor	Capacitor	Transformer	Active power switch	Total
[33]	6	3	4	1	2	16
[34]	4	2	3	1	4	14
Conventional	6	1	4	1	2	14
Proposed	2	3	3	1	4	13

5. CONCLUSION

A pure bridgeless boost half bridge with bidirectional switch was proposed. The proposed converter employs lowest number of components with bidirectional semiconductor switches. The bidirectional switches allow the circuit operation at positive and negative cycle of input voltage. The bridge diode in conventional AC-DC half bridge circuit and conventional semi-bridgeless was eliminated. Therefore, it reduces the power losses especially the diodes conduction loss. Hence, better conversion efficiency is achieved. Furthermore, the crossover of input current was minimized with higher frequency of input supply voltage. It was verified that at full load, the input current is in phase to voltage supply which lead to 0.99 power factor both at 50 Hz and 500 Hz of input supply voltage. Furthermore, it was observed that the input current THD meets the standard of IEC 6000-3-2. Moreover, only single control signal was required to drive the power switches which lead to simple control circuit. A proof of concept experimental prototype of a 100 W, 20 Vdc, and 115 Vrms input was built to verify the theoretical working principal.

REFERENCES

[1] B. Singh, B. N. Singh, A. Chandra, K. Al-Haddad, A. Pandey, and D. P. Kothari, "A review of single-phase improved power quality AC-DC converters," in *IEEE Transactions on Industrial Electronics*, vol. 50, no. 5, pp. 962-981, October 2003, doi: 10.1109/TIE.2003.817609.

[2] O. Garcia, J. A. Cobos, R. Prieto, P. Alou, and J. Uceda, "Single phase power factor correction: a survey," *in IEEE Transactions on Power Electronics*, vol. 18, no. 3, pp. 749-755, May 2003, doi: 10.1109/TPEL.2003.810856.

[3] J. C. Salmon, "Techniques for minimizing the input current distortion of current-controlled single-phase boost rectifiers," in *IEEE Transactions on Power Electronics*, vol. 8, no. 4, pp. 509-520, October 1993, doi: 10.1109/63.261022.

[4] R. Erickson, M. Madigan, and S. Singer, "Design of a simple high-power-factor rectifier based on the flyback converter," *Fifth Annual Proceedings on Applied Power Electronics Conference and Exposition*, 1990, pp. 792-801, doi: 10.1109/APEC.1990.66382.

[5] M. R. T. Hossain, A. H. Abedin, M. H. Rahaman, M. S. Arifin, M. A. Choudhury, and M. N. Uddin, "Input switched single phase high performance bridgeless AC-DC Zeta converter," *2012 IEEE International Conference on Power Electronics, Drives and Energy Systems (PEDES)*, 2012, pp. 1-5, doi: 10.1109/PEDES.2012.6484335.

[6] X. Chen, T. Jiang, X. Huang, and J. Zhang, "A high efficiency bridgeless flyback PFC converter for adapter application," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 1013-1017, doi: 10.1109/APEC.2013.6520423.

[7] M. Kwon, and S. Choi, "An Electrolytic Capacitorless Bidirectional EV Charger for V2G and V2H Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6792-6799, September 2017, doi: 10.1109/TPEL.2016.2630711.

[8] K. Yoo, K. Kim, and J. Lee, "Single- and Three-Phase PHEV Onboard Battery Charger Using Small Link Capacitor," in *IEEE Transactions on Industrial Electronics*, vol. 60, no. 8, pp. 3136-3144, August 2013, doi: 10.1109/TIE.2012.2202361.

[9] S. Jeong, J. Kwon, and B. Kwon, "High-Efficiency Bridgeless Single-Power-Conversion Battery Charger for Light Electric Vehicles," in *IEEE Transactions on Industrial Electronics*, vol. 66, no. 1, pp. 215-222, January 2019, doi: 10.1109/TIE.2018.2826458.

[10] C. Qiao, and K. M. Smedley, "A topology survey of single-stage power factor corrector with a boost type input-current-shaper," in *IEEE Transactions on Power Electronics*, vol. 16, no. 3, pp. 360-368, May 2001, doi: 10.1109/63.923768.

[11] Y. Hu, L. Huber, and M. M. Jovanovic, "Single-Stage Flyback Power-Factor-Correction Front-End for HB LED Application," *2009 IEEE Industry Applications Society Annual Meeting*, 2009, pp. 1-8, doi: 10.1109/IAS.2009.5324874.

[12] J. Lee, J. Kwon, E. Kim, W. Choi, and B. Kwon, "Single-Stage Single-Switch PFC Flyback Converter Using a Synchronous Rectifier," in *IEEE Transactions on Industrial Electronics*, vol. 55, no. 3, pp. 1352-1365, March 2008, doi: 10.1109/TIE.2007.911908.

[13] H. S. Athab and D. Dah-Chuan Lu, "A High-Efficiency AC/DC Converter with Quasi-Active Power Factor Correction," in *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1103-1109, May 2010, doi: 10.1109/TPEL.2009.2037000.

[14] S. Li, J. Deng, and C. C. Mi, "Single-Stage Resonant Battery Charger with Inherent Power Factor Correction for Electric Vehicles," in *IEEE Transactions on Vehicular Technology*, vol. 62, no. 9, pp. 4336-4344, November 2013, doi: 10.1109/TVT.2013.2265704.

[15] J. Lee, Y. Yoon, and J. Kang, "A Single-Phase Battery Charger Design for LEV Based on DC-SRC With Resonant Valley-Fill Circuit," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2195-2205, April 2015, doi: 10.1109/TIE.2014.2351371.
[16] N. Q. Trong, H. Chiu, Y. Lo, C. Lin, and M. M. Alam, "Modified current-fed full-bridge isolated power factor correction converter with low-voltage stress," *IET Power Electronics*, vol. 7, no. 4, pp. 861-867, April 2014, doi: 10.1049/iet-pel.2013.0183.
[17] C. Li, Y. Zhang, Z. Cao, and D. XU, "Single-Phase Single-Stage Isolated ZCS Current-Fed Full-Bridge Converter for High-Power AC/DC Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 9, pp. 6800-6812, September 2017, doi: 10.1109/TPEL.2016.2623771.
[18] L. S. C. e Silva, F. J. M. de Seixas, and M. A. G. de Brito, "Bridgeless interleaved boost PFC converter with variable duty cycle control," *XI Brazilian Power Electronics Conference*, 2011, pp. 397-402, doi: 10.1109/COBEP.2011.6085238.
[19] D. Lohbeck, "Safety Isolation Protects Users and Electronics Instruments," www.edn.com, 2003. [Online]. Available: https://www.edn.com/safety-isolation-protects-users-and-electronic-instruments/.
[20] S. H. Hosseini and S. Nazemi, "Unity power factor isolated bridgeless rectifier based on coupled inductors," 2011 *7th International Conference on Electrical and Electronics Engineering (ELECO)*, 2011, pp. I-293-I-297. [Online]. Available: https://ieeexplore.ieee.org/document/6140163.
[21] J. Baek, J. Shin, P. Jang, and B. Cho, "A critical conduction mode bridgeless flyback converter," *8th International Conference on Power Electronics-ECCE Asia*, 2011, pp. 487-492, doi: 10.1109/ICPE.2011.5944586.
[22] M. R. Sahid and A. H. M. Yatim, "An isolated bridgeless AC-DC converter with high power factor," *2010 IEEE International Conference on Power and Energy*, 2010, pp. 791-796, doi: 10.1109/PECON.2010.5697687.
[23] J. Shin, S. Choi, and B. Cho, "High-Efficiency Bridgeless Flyback Rectifier with Bidirectional Switch and Dual Output Windings," in *IEEE Transactions on Power Electronics*, vol. 29, no. 9, pp. 4752-4762, September 2014, doi: 10.1109/TPEL.2013.2283073.
[24] W. Y. Choi, J. M. Kwon, and B. H. Kwon, "Efficient LED back-light power supply for liquid-crystal-display," *IET Electric Power Applications*, vol. 1, no. 2, pp. 133-142, March 2007, doi: 10.1049/iet-epa:20060222.
[25] W. Choi, W. Yu, and J. Lai, "A novel bridgeless single-stage half-bridge AC/DC converter," *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2010, pp. 42-46, doi: 10.1109/APEC.2010.5433695.
[26] H. Cho, J. Yoo, J. Choi, M. Yang, and W. Choi, "Bridgeless half-bridge AC-DC converter with series-connected two transformers," *2013 Twenty-Eighth Annual IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2013, pp. 3241-3245, doi: 10.1109/APEC.2013.6520764.
[27] H. Ribeiro, B. Borges, S. Pinto, and F. Silva, "Bridgeless Single-Stage Full-Bridge Converter with One Cycle Control in the output voltage," *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 2899-2906, doi: 10.1109/ECCE.2010.5618202.
[28] Y. Chen and S. Mo, "A bridgeless active-clamp power factor correction isolated SEPIC converter with mixed DCM/CCM operation," *2013 1st International Future Energy Electronics Conference (IFEEC)*, 2013, pp. 1-6, doi: 10.1109/IFEEC.2013.6687469.
[29] S. Nigsch, S. Cuk, and K. Schenk, "Analysis, modeling and design of a True Bridgeless Single Stage PFC with galvanic isolation," *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2015, pp. 469-476, doi: 10.1109/APEC.2015.7104392.
[30] V. A. G. Cunha, A. O. Costa Neto, G. B. Lima, and L. C. G. Freitas, "A Bridgeless Boost Half Bridge DC-DC Converter for Electrical and Hybrid Vehicle Applications," *2019 IEEE PES Innovative Smart Grid Technologies Conference - Latin America (ISGT Latin America)*, 2019, pp. 1-6, doi: 10.1109/ISGT-LA.2019.8895388.
[31] A. M. Naradhipa, S. Kang, B. Kim, and S. Choi, "A New Single-Stage Bridgeless Boost Half-Bridge AC/DC Converter with Semi-Active-Rectifier," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 2019, pp. 757-762, doi: 10.1109/APEC.2019.8722217.
[32] United States Department of Energy (DOE), "ENERGY STAR Program Requirements for Single Voltage External AC-DC and AC-AC Power Supplies Eligibility Criteria (Version 2.0) Final Draft," pp. 2-8. [Online]. Available: https://www.energystar.gov/ia/partners/product_specs/program_reqs/eps_prog_req.pdf.
[33] R. W. Erickson and D. Macsimovic, "*Fundamentals of Power Electronics"2nd Ed*., Kluwer Academic Publishers, 2000, doi: 10.1007/978-0-306-48048-5.
[34] Ferroxcube, "Soft Ferrites and Data Handbook," *Ferroxcube A Global Company*, p. 30, July 2013. [Online]. Available: https://www.ferroxcube.com/en-global/download/download/11.
[35] Ferroxcube, "Soft Ferrites: Application," *Feeroxcube inc*., pp. 17-53, September 2008. [Online]. Available: http://ferroxcube.home.pl/prod/assets/sfappl.pdf.
[36] M. N. Z. Abidin, "IEC 61000-3-2 Harmonics Standard Overview," *Schaffner EMC Inc., Edsion*, NJ, USA, pp. 1-5, May 2006. [Online]. Available: https://www.emcfastpass.com/wp-content/uploads/2017/04/Class_definitions.pdf.
[37] K. S. Muhammad and D. Dah-Chuan Lu, "Two-switch ZCS totem-pole bridgeless PFC boost rectifier," *2012 IEEE International Conference on Power and Energy (PECon)*, 2012, pp. 1-6, doi: 10.1109/PECon.2012.6450206.
[38] R. Burkel and T. Schneider, "Fasr Recovery Epitaxial Diodes (FRED) Characteristics-Application-Examples," *IXAN0044*, 1999. [Online]. Available: https://www.ixys.com/Documents/AppNotes/IXAN0044.pdf.
[39] W. Shepherd, L. N. Hulley, and D. T. W. Liang, "Power electronics and motor control 2nd Edition," *Cambirge University Press*, January 1996, doi: 10.1017/cbo9781139172820.

[40] Y. Khersonsky, M. Robinson, and D. Gutierrez, "The HEXFRED Ultrafast Diode in Power Switching Circuit," *International Rectifier*, 1992. [Online]. Available: https://www.infineon.com/dgdl/an-989.pdf?fileId=5546d462533600a40153559fa625124d.
[41] F. Musavi, D. S. Gautam, W. Eberle and W. G. Dunford, "A simplified power loss calculation method for PFC boost topologies," 2013 IEEE Transportation Electrification Conference and Expo (ITEC), 2013, pp. 1-5, doi: 10.1109/ITEC.2013.6573469.

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