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Small-signal analysis of a single-stage bridgeless boost half-bridge AC/DC converter with bidirectional switch

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ABSTRACT

A small-signal analysis of a single-stage bridgeless boost half-bridge alternating current/direct current (AC/DC) converter with bidirectional switches is performed using circuit averaging method. The comprehensive approach to develop the small signal model from the steady state analysis is discussed. The small-signal model is then simulated with MATLAB/Simulink. The small-signal model is verified through the comparison of the bode-plot obtained from MATLAB/Simulink and the simulated large signal model in piecewise linear electrical circuit simulation (PLECS). The mathematical model obtain from the small-signal analysis is then used to determine the proportional gain K_p and integral gain K_i. In addition, the switch large-signal model is developed by considering the current and voltage waveforms during load transients and steady-state conditions.

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1. INTRODUCTION

Nowadays, the usage of electronic equipment's has increased drastically. The requirement set up by a regulatory body such as *80Plus* [1] and *"Energy Star"* [2], [3] has gain consumer attention which demand less harmonic, high power factor and higher efficiency system. Significantly, these trend makes the power factor correction (PFC) becoming important aspect even for low power electronic equipment's. Thus, researchers have proposed a new PFC technique which comply the setup standard such as IEC555-2 and IEC6100-4-7. In addition, the galvanic isolation is also one of the state requirements in international electrotechnical commission (IEC) standard [4] for the safety of the end user. However, the total cost is also one of the key factors to meet the setup requirements. Thus, as the comparison to two-stage scheme, single stage scheme is cost effective [5]. Single stage power converter integrates the PFC and direct current-direct current (DC-DC) converter circuit which significantly reduce the number of components [6]. However, the slow input bridge diodes and bulky DC link capacitor significantly leads to power losses. The proposed single stage semi-bridgeless converter without bulky DC link capacitor [7], [8] significantly reduce the converter power losses. Thus, improved the conversion efficiency with less components count.

Any new proposed circuit topologies should consider the main analysis of both large-signal model and small-signal model [9]. The large-signal analysis is for components design such as transformer, inductance and capacitance. The small-signal model is to investigate the behavior of a power convertor.

Several methods have been presented to derive the small signal model of a switched mode converter namely circuit averaging [10]-[17], state-space averaging [18]-[23] and current injected equivalent circuit approach [21], [22]. In circuit averaging technique, the averaging and linearization operations are performed

directly from the converter circuit. The small-signal equation is derived from the steady state operation of the converter circuit. The steady-state equation is derived from the circuit operation and waveform analysis in one switching period. It is assumed that the components are lossless and ideal. This is to simplify the equation which derive from steady-state and small-signal analysis.

In this paper, the small-signal of a bridgeless AC/DC converter with bidirectional switches as depicted in Figure 1 is presented. The full bridgeless of the proposed circuit topology eliminated the bridge rectifier of a conventional circuit topology and the semi-bridgeless diodes [7], [8] in a conventional bridgeless circuit. The idea of the proposed converter is based on the primary side [18] but without diodes presented which further eliminate the line frequency rectifier losses. In addition, the bidirectional switch concept is derived from the topologies in [24]-[31]. The bidirectional switches simplify the mode of circuit operation and control signal. The small-signal model is develop using the similar procedure in [19], [23]. The small-signal model is then used to find the control-to-output transfer function of the converter. Then, the derived transfer function of the proposed circuit is simulated in MATLAB/Simulink. The bode plot obtain from the MATLAB/Simulink is then verified with the bode-plot obtained from the large circuit model which simulated with PLECS. In addition, a switch large-signal model is proposed which is derive from the steady-state equation. The model is designed with the circuit parameters as stated in Table 1.

The circuit level simulation and experimental verification results will be presented in another report. This report will only be discussed on the verification of the derived small signal equation with MATLAB and PLECS software. In a nutshell, this works.

– Eliminates the drawbacks of a bridge rectifier in conventional AC/DC converter circuit and a semi-bridgeless AC/DC conventional circuit
– Eliminates the crossover distortion of input current at high frequency of input supply
– Input current harmonic which comply to the IEC 6000-3-2 standard
– Improve input power factor
– Reduce the components count
– Simplify the modes of circuit operation and control signal

In section 2, the details steady state analysis of the proposed circuit topology will be discussed. The modes of circuit operation with switching waveforms are illustrated to support the derivation of releated equations. Section 3 presented the small signal analysis and derivation steps to obtained the transfer function; control-to-ouput, output-to-input, and impedance. Next, the converter small signal block diagram in Simulink and in PECS is proposed. Section 4 presented the results from both MATLAB/Simulink and PLECS for verification. In addition, the large signal switch model is obtained. Finally, section 5 gives the conclusion.

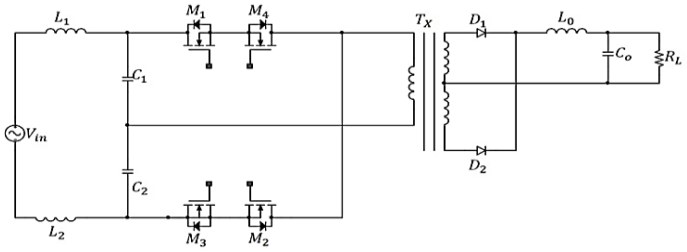

Figure 1. Proposed AC-DC full bridgeless half-bridge with bidirectional switch

Table 1. Proposed circuit parameters

Parameters	Values
Input voltage, V_{in}	115 Vrms
Input line frequency,	50 Hz
Switching frequency, f_S	50 kHz
Output voltage, V_O	20 V DC
Boost inductor L_1, L_2	500 µH
Inductor L_o	100 µH
Capacitor C_1, C_2	0.1 µF
Capacitor C_o	10 mF

2. STEADY STATE ANALYSIS

In this analysis, all switches and components are assumed to be ideal and the analysis only carried out at the positive half line cycle. Figure 2 shows the four mode of circuit operation at positive half cycle of input voltage v_{in}. At Mode 1, the Kirchhoff voltage law (KVL) equation at primary side is:

$$v_{in} = v_{L_1} + v_{C_1} + v_{C_2} + v_{L_2} \quad (1)$$

As depicted in Figure 2 (a), capacitor C_1 is connected in parallel with the transformer primary winding. Capacitor C_1 discharged to primary winding. The value of capacitor C_1 and C_2 are also equal, and capacitor C_2 is in charging mode. As depicted from the key waveform, the capacitor voltage C_1 and C_2 is equal to the difference between the input voltage and the boost inductor voltage. The capacitor voltage is at minimum or maximum at starting of each switching mode. This is due to the capacitor which is almost fully charged or fully discharged at the end of switching mode. Thus, assume the capacitor C_2 voltage; $v_{C_2} \approx 0\ V$ and the capacitor C_1 voltage; v_{C_1} equal to transformer primary voltage v_p. The value of the inductor L_1 and L_2 are equal.
Therefore, (1) can be simplified as.

$$v_{in} = 2v_L + v_p + v_{C_2} \quad (2)$$

The transformer turn ratio n is given by:

$$n = \frac{v_s}{v_p} = \frac{N_s}{N_p} = \frac{i_p}{i_s} \quad (3)$$

where transformer winding number of turns at primary side N_p and secondary side N_s.
Thus, the voltage equation at secondary side v_s^+ in Mode 1 is.

$$v_{s^+} = v_{L_o} + v_o \quad (4)$$

At Mode 2 in Figure 2 (b), the KVL equation at primary side is.

$$v_{in} = v_{L_1} + v_{c_1} + v_{c_2} + v_{L_2} \quad (5)$$

Thus, the inductor voltage can be written as:

$$v_L = \frac{1}{2}\left(v_{in} - v_{c_1} - v_{c_2}\right) \quad (6)$$

Mode 3 in Figure 2 (c) is similar to Mode 1. Thus, the voltage equation at secondary side v_s^-;

$$v_{s^-} = v_{L_o} + v_o \quad (7)$$

where v_{L_o} is voltage drop at ouput inductor and v_o is the load voltage.
The boost mode operation at primary side in Mode 4 is the same as Mode 2. Thus, the KVL equation for mode 4 in Figure 2 (d) is the same as (5).
The voltage drop equation at output inductor is.

$$v_{L_o} = L_o \frac{di_{L_o}}{dt} \quad (8)$$

Substitute (2)-(5) to (1), thus the boost inductor voltage is;

$$v_L = \frac{1}{2}\left(v_{in} - \frac{L_o\left(\frac{di_{L_o}}{dt}\right) + v_o}{n} - v_{C_2}\right) \quad (9)$$

The average voltage across inductor L_o within each switching period is zero. Thus, it can be concluded in (8) that for each half line period.

$$L_o\left(\frac{di_{L_o}}{dt}\right) = v_{L_{o.avg}} = 0 \quad (10)$$

Hence, (7) can be simplified as.

$$v_L = \frac{1}{2}\left(v_{in} - \frac{v_o}{n} - v_{c_2}\right) \quad (11)$$

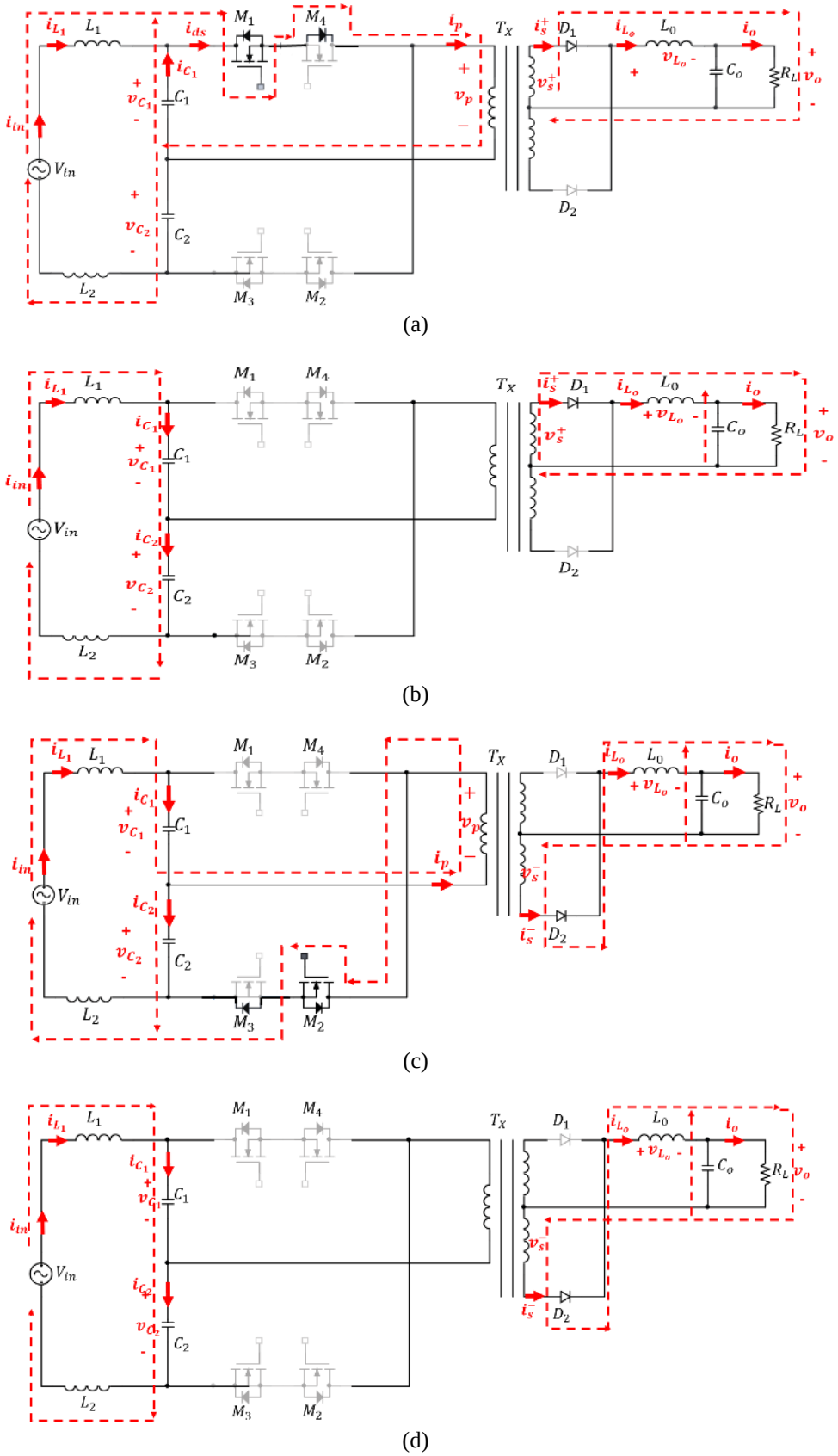

Figure 2. Circuit operation at positive half-cycle of input voltage, (a) Mode 1, (b) Mode 2, (c) Mode 3, (d) Mode 4

The boost inductor is in charging in Mode 1 and 3 and discharge at Mode 2 and 4 of the switching periods. It is assumed that the magnitude of input voltage is constant. Consequently, the input current also assumes to be constant. The boost inductor current works in continuous current mode. Therefore, based on the balanced volt-second;

$$\Delta i_{L-d_1T_s} = \Delta i_{L-d_2T_s} \tag{12}$$

Hence, by (12), the relationship of duty cycle at Mode 1 $d_1$and Mode 2 d_2,

$$d_1 = \frac{v_{in}-v_{c_1}-v_{c_2}}{v_{in}-\frac{v_o}{n}-v_{c_2}} d_2 \tag{13}$$

The capacitor voltage in one switching period is zero volt. Therefore, (13) can be simplified as.

$$d_1 = \frac{v_{in}}{v_{in}-\frac{v_o}{n}} d_2 \tag{14}$$

The total period of Mode 1 and Mode 2 is half of the switching period. Therefore;

$$d_2 = (0.5 - d_1)T_s \tag{15}$$

Substitute (15) in (14), thus;

$$d_1 = \frac{v_{in}}{2\left(2v_{in}-\frac{v_o}{n}\right)} \tag{16}$$

The input current directly flows to the boost inductor L_1 and L_2. Thus, the boost inductor current i_L is equal to input current i_{in}. Assume that all input power transferred to output. Thus, the input current is.

$$i_L = \frac{v_o^2}{v_{in}R\cos\theta} \tag{17}$$

where θ is power factor angle and $R$is load resistance.
Hence, the boost inductor is choose such that.

$$L \geq \frac{\left(v_{in}-\frac{v_o}{n}\right)d_1 v_{in}R\cos\theta}{2v_o^2 f_s} \tag{18}$$

where f_s is the switching frequency
As depicted from switching waveform, the input current flow to the half bridge capacitor $C_1$and C_2 at a period of $(1 - d_1)T_S$. Thus; the current flow trough capacitor C_1; $i_{c_1}$and C_2; i_{c_2}.

$$i_{c_1} = i_{c_2} = i_{in} \tag{19}$$

Therefore, the expression of half bridge capacitor is.

$$C_1 = C_2 = \frac{v_o^2}{\Delta v_c v_{in}R\cos\theta}(1 - d_1)T_s \tag{20}$$

where Δv_C is the minimum to maximum charging voltage of half bridge capacitor. As depicted from Figure 3, each half bridge capacitor is charged approximately from zero to peak supply voltage.

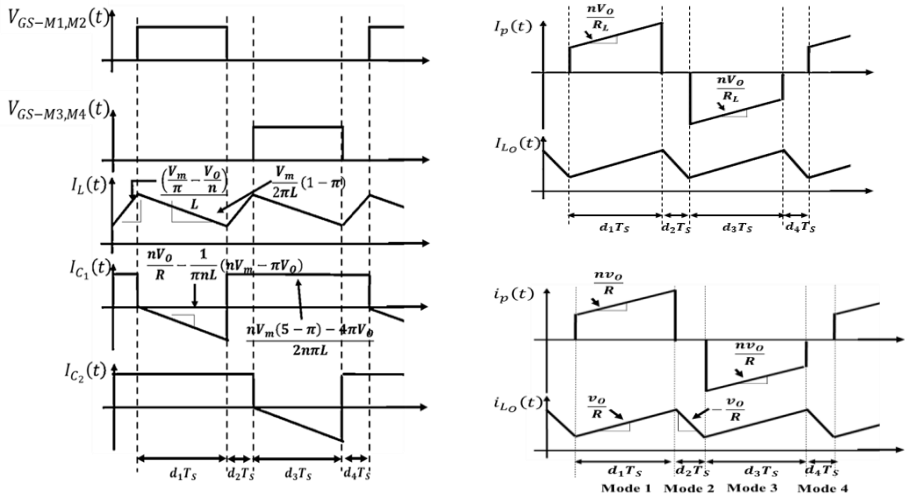

Figure 3. Proposed key waveform

There is no connection between the input boost circuit to output circuit at Mode 2 and Mode 4. Therefore, no energy transferred from primary side to secondary side of the transformer in this mode. Thus, the output inductor L_o and output capacitor C_O are discharged to the load R. Therefore;

$$\frac{di_{L_O}}{dt} = -\frac{v_o}{L_o} \tag{21}$$

By assuming the output capacitor C_O is fully charge, the output inductor current is.

$$i_{L_o} = i_o = \frac{v_o}{R_L} \tag{22}$$

Thus, the maximum and minimum output inductor current $i_{L_{O,max}}$ and $i_{L_{O,min}}$ are.

$$i_{L_{o,\max}} = i_{L,average} + \frac{\Delta i_{L_o - d_2T_s}}{2} \tag{23}$$

$$i_{L_{o,\max}} = \frac{v_o}{R_L} + \frac{v_o}{L_o} d_2T_s \tag{24}$$

$$i_{L_{o,\min}} = \frac{v_o}{R_L} - \frac{v_o}{L_o} d_2T_s \tag{25}$$

Thus, the output inductor ripple Δi_O;

$$\Delta i_{L_o} = i_{L_{o,\max}} - i_{L_{o.\min}} \tag{26}$$

In order to ensure output inductor working in continuous conduction mode;

$$L_{o_{\min}} \geq R_L d_2T_s \tag{27}$$

Since the output capacitor current wave-shape same as output inductor current, the charge in output capacitor is equal to the area under the wave-shape. Thus, the Δv_{C_O} is;

$$\Delta v_{c_o} = \Delta_{v_o} = \frac{d_2 v_o}{8 C_o L_o f_s^2} \tag{28}$$

Hence, the output voltage ripple, r is;

$$r = \frac{\Delta v_o}{v_o} = \frac{d_2}{8C_o L_o f_s^2} \tag{29}$$

By examining the above waveform, the peak inductor current can be represented as.

$$\Delta i_{L-peak} = \frac{1}{2L}\left(v_{in} - \frac{v_o}{n} - v_{c_1}\right) d_1 T_s \tag{30}$$

Based on the Kirchhoff current law, the current at capacitor C_1 is.

$$i_{c_1} = i_p - i_L \tag{31}$$

By substituting (2) and (30) in (31). Thus;

$$\Delta i_{c_{1-peak}} = \left(\frac{nv_o}{R} - \frac{v_{in}}{2L} - \frac{v_o}{2Ln} - \frac{v_{c_1}}{2L}\right) d_1 T_s \tag{32}$$

At d_1, the output inductor is connected to the transformer secondary winding through the rectifier diode. Therefore, output inductor current same as secondary current of the transformer. Thus,

$$\Delta i_{L_{o-peak}} = \left(\frac{i_p}{n}\right) d_1 T_s \tag{33}$$

In addition, the output capacitor current ripple is.

$$\Delta i_{c_{o-peak}} = \left(\frac{i_p}{n} - \frac{v_o}{R}\right) d_1 T_s \tag{34}$$

And at d_2

$$\Delta i_{L-peak} = \frac{1}{2L}\left(v_{in} - v_{c_1} - v_{c_2}\right) d_2 T_s \tag{35}$$

At d_2, since all switches are in OFF state, the boost circuit has no connection to the secondary circuit loop. Therefore, the half bridge capacitor current same as boost inductor current. Thus,

$$\Delta i_{c_1} = \Delta i_L \tag{36}$$

As depicted from the capacitor current waveform, capacitor current is constant across the period of $(1 - d_1)$. Thus.

$$\Delta i_{c_{1-peak}} = \left(\frac{3(v_{in} - v_{c_1})}{2L} - \frac{v_{c_2}}{L} - \frac{v_o}{2Ln}\right)(1 - d_1) T_s \tag{37}$$

At d_2, because has no energy transfer from primary circuit, hence.

$$\Delta i_{L_{o-d_2}} = -\left(\frac{v_o}{L_o}\right) d_2 T_s \tag{38}$$

$$\Delta i_{c_{o-d_2}} = -\left(\frac{v_o}{R}\right) d_1 T_s \tag{39}$$

This derived equation will further apply in development of small signal and steady state modelling.

3. SMALL-SIGNAL ANALYSIS

For the proposed circuit topology, the circuit averaging and average switch model are used to develop the small signal model. The similar procedure [10] applied to develop the small signal model. The small-signal model is then used to find the control-to-output transfer function of the converter. In the case of the proposed bridgeless converter, the input current is the same current flow to the inductor and also to the half bridge capacitors. Thus, only inductor loop and output capacitor loop are presented.

In the steady state, the average inductor voltage is zero but there is no net change in inductor current over one switching period. During transients or ac variations, the average inductor voltage is not zero and this leads to net variations in inductor current. The net change in inductor current over one switching period is

exactly equal to inductor voltage. It can be computed by linear ripple approximation. Thus, the waveforms now will be replaced with their low frequency average value. As depicted from the waveform, the inductor current period is twice of switching period which Mode 1 to Mode 2 and Mode 3 to Mode 4. Therefore, the small ripple approximation equation at Mode 1 interval is.

$$v_L(t)_{T_s} = \frac{\langle v_{in}(t)\rangle_{T_s}}{2} - \frac{\langle v_o(t)\rangle_{T_s}}{2n} - \frac{\langle v_{c_2}(t)\rangle_{T_s}}{2} \tag{40}$$

$$i_{c_o}(t)_{T_s} = \frac{\langle i_p(t)\rangle_{T_s}}{n} - \frac{\langle v_o(t)\rangle_{T_s}}{R} \tag{41}$$

The small ripple approximation equation at Mode 2 interval is

$$v_L(t)_{T_s} = \frac{\langle v_{in}(t)\rangle_{T_s}}{2} - \frac{\langle v_{c_1}(t)\rangle_{T_s}}{2} - \frac{\langle v_{c_2}(t)\rangle_{T_s}}{2} \tag{42}$$

$$i_{c_o}(t)_{T_s} = \frac{\langle i_p(t)\rangle_{T_s}}{n} - \frac{\langle v_o(t)\rangle_{T_s}}{R} \tag{43}$$

In the previous steady state analysis, the input voltage V_{in} is considered to be constant. However, in the next derivation of small signal model, the sinusoidal input voltage will be used. Thus, the small signal equation describes on how the low frequency circuit components waveform evolve in time. The input sinusoidal can be represented as.

$$v_{in}(t) = V_m \sin \omega t \tag{44}$$

Substitute (41) to small ripple approximation equation and integrate it within half cycle of input voltage. Thus, the average inductor voltage can be represented as.

$$L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = \left(\frac{\langle v_m(t)\rangle_{T_s}}{\pi} - \frac{\langle v_o(t)\rangle_{T_s}}{2n} - \frac{v_{c_2}(t)}{2}\right)d_1(t) + \left(\frac{v_m(\omega t)}{\pi} - \frac{v_{c_1}(\omega t)}{2} - \frac{v_{c_2}(\omega t)}{2}\right)d_2(t) \tag{45}$$

The average capacitor loop equation can be represented as.

$$C_o\frac{d\langle v_{c_o}(t)\rangle_{T_s}}{dt} = \left(\frac{\langle i_p(t)\rangle_{T_s}}{n} - \frac{\langle v_o(t)\rangle_{T_s}}{R}\right)d_1(t) + \left(-\frac{\langle v_o(t)\rangle_{T_s}}{R}\right)d_2(t) \tag{46}$$

Both (42) and (43) is non-linear differential equation. Next, assume that the input voltage, duty cycle, dependent voltages and currents are equal to some quiescent values together with superimposed small ac variations. The non-linear equations can be linearized if the magnitude of ac variations are much smaller than the respective quiescent values. Hence, insert the perturbed expression to the average inductor voltage equation and capacitor average equation. Therefore, there are DC term, first order term and second order term present in the inductor and capacitor average loop equations. Hence, the simplified first order equations are.

$$\begin{aligned} L\frac{d\langle i_L(t)+\hat{\imath}_L(t)\rangle_{T_s}}{dt} = {} & \left(\frac{\langle v_m(t)+\hat{v}_m(t)\rangle_{T_s}}{\pi} - \frac{\langle v_o(t)+\hat{v}_o(t)\rangle_{T_s}}{2n} - \frac{\langle v_{c_2}(t)+\hat{v}_{c_2}(t)\rangle_{T_s}}{2}\right)\left(D+\hat{d}_1(t)\right) + \\ & \left(\frac{\langle v_m(t)+\hat{v}_m(t)\rangle_{T_s}}{\pi} - \frac{\langle v_o(t)+\hat{v}_o(t)\rangle_{T_s}}{2n} - \frac{\langle v_{c_2}(t)+\hat{v}_{c_2}(t)\rangle_{T_s}}{2}\right)\left(D'-\hat{d}_1(t)\right) \end{aligned} \tag{47}$$

$$C_o\frac{d\langle v_{c_o}+\hat{v}_{c_o}(t)\rangle_{T_s}}{dt} = \left(\frac{\langle i_p+\hat{\imath}_p(t)\rangle_{T_s}}{n} - \frac{\langle v_o+\hat{v}_o(t)\rangle_{T_s}}{R}\right)\left(D+\hat{d}_1(t)\right) + \left(-\frac{\langle v_o+\hat{v}_o(t)\rangle_{T_s}}{R}\right)\left(D'-\hat{d}_1(t)\right) \tag{48}$$

DC terms only containing DC quantities. Therefore, DC term will be removed in order to get small signal linearize equation. The second order ac terms are nonlinear because it contains the product of ac quantities. On the other hand, the second order ac terms are much smaller than the first order form. Therefore, the second order terms will be neglected. Thus, only first order equation left. The first order term contains a single ac quantity which mostly multiplied by a constant coefficient such as DC term. These first order equation is the linearize equation which describes small signal ac variations.

The proposed circuit average model is depicted in Figure 4 (a) which derived from the of (47) and (48). The average switch network in Figure 4 (a) also can be represented as a transformer coil as depicted in

Figure 4 (b). Next, Figure 4 (c) is the equivalent circuit average model referred to secondary side of the transformer.

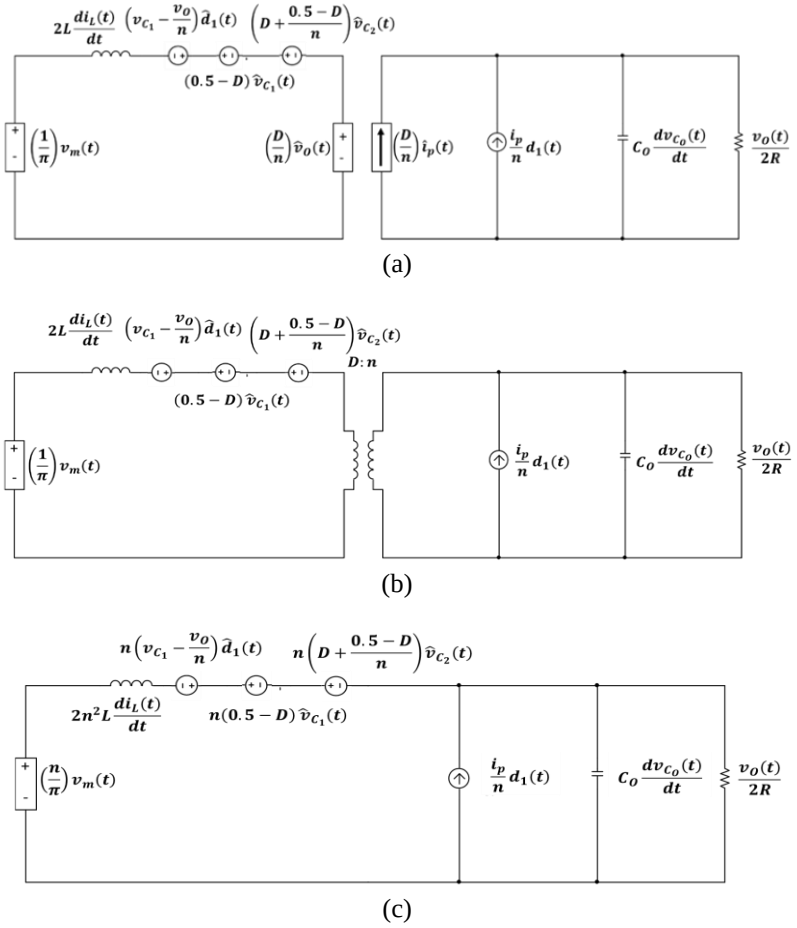

Figure 4. Proposed equivalent circuit of small signal AC, (a) with dependent sources, (b) with ideal DC transformer, (c) referred to secondary side

The circuit elements in the equivalent circuit average model of Figure 4 (c) is then converted from time domain $'t'$ to $'s'$ domain. The voltage sources of $V_m(s), V_{C_1}(s)$ and $V_{C_2}(s)$ are set equal to 0 in order to derive the control-to=output transfer function $\frac{v_O(s)}{d(s)}$. On the other hand, the $D(s), V_{C_1}(s)$ and $V_{C_2}(s)$ is equal to zero to obtain the line to output transfer function $\frac{v_O(s)}{v_m(s)}$. The output impedance $Z(s)$ is obtained as disturbances to test the control to output transfer function. Thus,

$$\frac{v_o(s)}{d(s)} = 2a \frac{\frac{2i_p nL}{a}s+1}{(2n^2LC)s^2+\left(\frac{2n^2L}{R}\right)s+1} \tag{49}$$

Where;

$$a = 2n\left(v_{c_1} - \frac{v_o}{n}\right) \tag{50}$$

$$\frac{v_o(s)}{v_m(s)} = k \times \frac{1}{(2n^2LC)s^2+\left(\frac{2n^2L}{R}\right)s+1} \tag{51}$$

Where;

$$k = \frac{2n}{\pi} \tag{52}$$

$$Z_o(s) = \frac{v_o(s)}{i_o(s)} = \frac{2n^2Ls}{(2n^2LC)s^2+\left(\frac{2n^2L}{R}\right)s+1} \quad (53)$$

The model in Figure 5 is simulated with control design tools in the MATLAB/Simulink. The Simulink control design is used to tune the value of controller proportional and integral coefficient. The control circuit parameters are determined based on the obtained steady state equation. The voltage follower control method is used to verify the operation of the proposed converter in circuit simulator and experimentally. This control method is used to regulate the output voltage to the desired value. Thus, the controller is expected to provide the appropriate duty cycle for any load changes. This closed loop feedback controller is designed using the control-to-output transfer function expressed by (49).

It is then compared with the transfer function that obtained from the switch model in PLECS/Simulink. This is to prove that the derived transfer function (49) is correct. The sinusoidal waveform with frequency of 10-1000 Hz and amplitude range of (0.1-4) V is used to perturb the converter duty cycle in the PLECS model. Thus, the duty cycle that drive the MOSFET's in the PLECS circuit is a summation of d_1 and the perturbed signal. Figure 6 shows the block diagram of the switch Model with perturbation of duty cycle in the PLECS/Simulink.

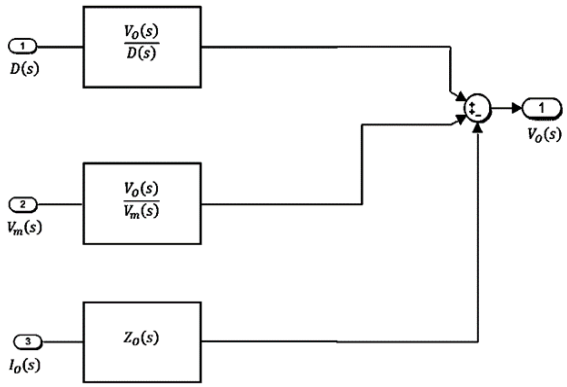

Figure 5. Proposed converter small signal block diagram in Simulink

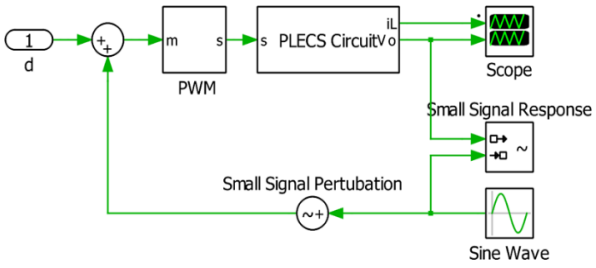

Figure 6. Proposed converter block diagram in PLECS

4. RESULTS

The circuit model in PLECS is used to verify the developed transfer function in Simulink. The bode-plot diagram obtained from the mathematical expression is compared with the bode-plot diagram obtained in the PLECS/Simulink switch model as depicted in Figure 7. The plot shows the same magnitude and Q-factor obtained from the mathematical expression and PLECS/Simulink switch model. However, a small difference of corner frequency f_o around 10 Hz is observed. This due to ideal consideration in developing the mathematical expression. Thus, the results show good agreement between the mathematical expression control to output transfer function and the PLECS/Simulink switch model. Therefore, the mathematical expression (49) which developed using circuit averaging techniques is validated. In this work, PI controller is used such that the output voltage is regulated at $20\ V_{DC}$ regardless the output power condition.

As depicted in Figure 8, the crossover frequency f_c is at 2.92 Hz with overall system phase margin of 90°. Table 2 shows the system performance and robustness which is obtained from the MATLAB/Simulink automated proportional-integrated-derivate (PID) tuning apps. It shows that the system meets the Nyquist stability criterion whereby the system is stable if the phase lag at the crossover frequency is less than 180°. However, an overshoot of 0.474% occurred which have to be accepted.

The small-signal model can be used to determine the stability of the propose system. However, there still have some loop hole even though small signal model can ensure the stability of the system. A small signal model only considered a small variation of circuit signal. Therefore, the large signal model is important to observe the overall time response analysis either during steady-state or transient. The large signal affects the operating point and non-linear components. In this work, the large-signal model as depicted in Figure 9 is developed by considering the current and voltage waveforms during load transients and steady-state conditions.

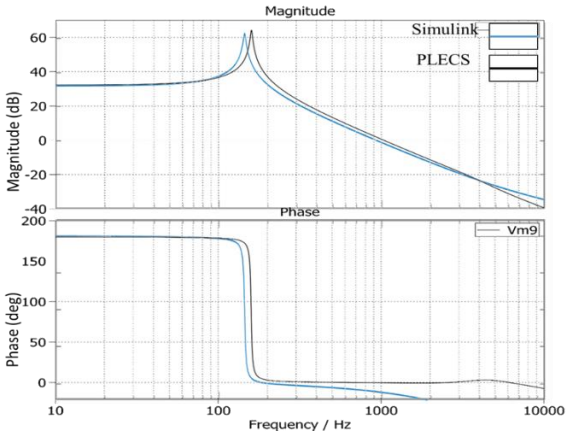

Figure 7. Comparison of an analysis in PLECS and control-to-output bode plot obtained with mathematical expression in Simulink

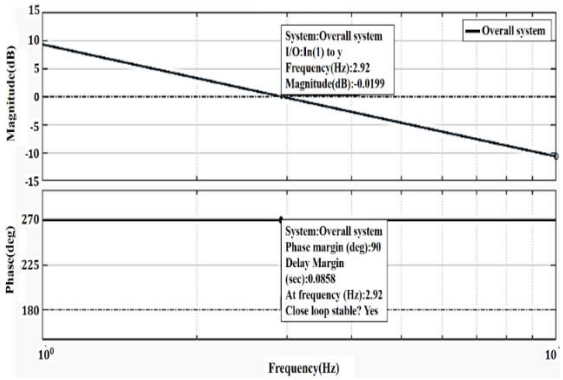

Figure 8. Bode-plot of the overall system with tuned compensator

Table 2. Tuned controller parameters, performance, and robustness

Parameter	Tuned
Rising time	0.118 seconds
Settling time	0.239 seconds
Overshoot	0.47%
Peak	1
Gain margin	2.7 dB @ 902 rad/s
Phase margin	90° @ 18.3 rad/s
Closed-loop stability	Stable

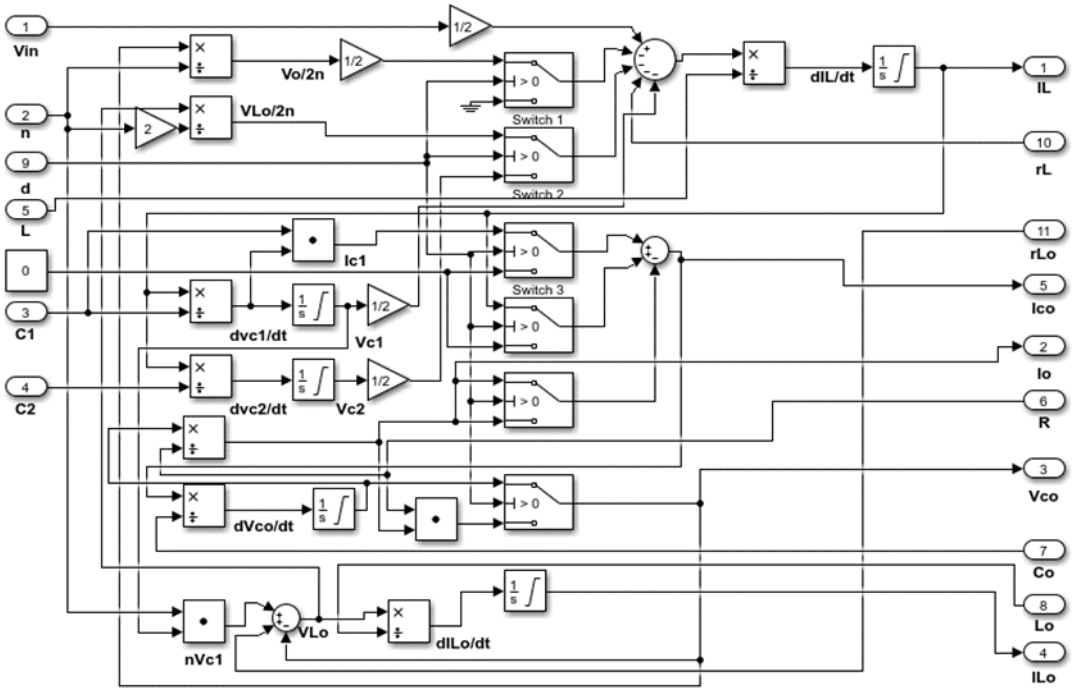

Figure 9. Large signal model developed in Simulink

5. CONCLUSION

The small-signal and steady-state analysis has been derived and discussed in detail. The results show good agreement between the mathematical expression control to output transfer function and the

PLECS/Simulink switch model. The mathematical expression of a small-signal model is used to design the PI controller. It shows that the system is stable and meet the Nyquist stability criterion. In addition, the large signal model based on switch model is developed. The details large signal circuit and experimental results will be discuss in another report.

6. FUTURE WORKS

This study is to verify the mathematical expression of a small signal model with Simulink/PLECS. The details design, circuit simulation, and experimental verification will be reported in another paper. The proposed circuit topology performances tested at input supply 115 Vac 50 Hz with output 20 Vdc 5 A. Hence, for future works, it is suggested to study the circuit performances at another parameters. In addition, the secondary side synchronous rectifier can be applied to furthermore reduce the overall power lossess.

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