Improved 25-level inverter topology with reduced part count for PV grid-tie applications

**Radouane Majdoul[1], Abelwahed Touati[2], Abderrahmane Ouchatti[3], Abderrahim Taouni[4],
Elhassane Abdelmounim[5]**

[1,2]Laboratory of Complex Cyber Physical Systems in ENSAM, Hassan 2 University, Casablanca, Morocco
[3,4]Laboratory of Electrical Systems & Control Engineering at Aïn Chock Science faculty- Hassan 2 University,
Casablanca, Morocco
[5]Laboratory of Mathematics, Informatics in Engineering Science in Science & Technical faculty, Hassan 1 University,
Settat, Morocco

Article Info

ABSTRACT

A new bidirectional multilevel inverter topology with a high number of voltage levels with a very reduced number of power components is proposed in this paper. Only TEN power switches and four asymmetric DC voltage sources are used to generate 25 voltage levels in this new topology. The proposed multilevel converter is more suitable for e-mobility and photovoltaic applications where the overall energy source can be composed of a few units/associations of several basic source modules. Several benefits are provided by this new topology: Highly sinusoidal current and voltage waveforms, low total harmonic distortion, very low switching losses, and minimum cost and size of the device. For optimum control of this 25-level voltage inverter, a special Modified Hybrid Modulation technique is performed. The proposed 25-level inverter is compared to various topologies published recently in terms of cost, the number of active power switches, clamped diodes, flying capacitors, DC floating capacitors, and the number of DC voltage sources. This comparison clearly shows that the proposed topology is cost-effective, compact, and very efficient. The effectiveness and the good performance of the proposed multilevel power converter (with and without PWM control) are verified and checked by computational simulations.

Corresponding Author:

Radouane Majdoul
Laboratory of Complex Cyber Physical Systems
ENSAM, Hassan 2 University
150 Nil Street, Sidi Othmane Casablanca, Morocco
Email: Radouane.majdoul@univh2c.ma

1. INTRODUCTION

The exceptional growth of the photovoltaic systems market is obviously due to major technological innovations and lower costs for photovoltaic panels. It is also due to major research efforts in semiconductor switch design and technological advances in power electronics and digital electronics [1]. Static converters have become much more efficient, reliable, and compact. Their function is also gradually improving, and their field of application is expanding. In this context, many multilevel inverter topologies have been investigated and developed to replace the two-level inverters in various medium and high voltage applications requiring increased performance: energy, grid-tie renewable energy systems, high voltage direct current (HVDC) power transmission, electric vehicles, and a multitude of industrial applications [2].

Furthermore, the continuous and constant development of power electronics and the increasing progress of fully controlled semiconductor technology presents cost-effective opportunities for the design and implementation of several interesting architectures and topologies of multilevel converters. In both academia and industry, these topologies are prevalent as power electronic interfaces due to their outstanding characteristics such as: lower switching power loss as a result of lower switching frequency and reduced device voltage, reduced voltage stress (dv/dt), lower THD, and harmonic contents, and reduced output filter size and cost [3], [4]. Splitting the voltage across the switches also allows for the use of reduced voltage rating semiconductors that have optimized dynamic performance and are economical because they are mass-produced [5]-[7].

The conventional multilevel inverter topologies mostly applied in grid-tie renewable energy and industrial applications include the Neutral Point Clamped (NPC) type shown in Figure 1 (a), the Flying Capacitors (FC) type in Figure 1 (b), the Cascaded H-Bridge converters (CHB) type with separate and isolated DC sources as shown in Figure 1 (c), and Modular Multilevel Converters depicted in Figure 1 (d) [8]-[11]. However, the multilevel converters consist of several drives, a lot of active power switches, and bulky passive power components which lead to considerable cost and increased size of the device; as matter of fact, the number of semiconductor power switches (NS), drivers and passive components required for achieving these topologies increases with the number of desired levels (NL) and the complexity of their structure is thereby increased: NS =2*(NL-1).

The NPC multilevel converters use, in addition to active switches, a large number of clamping diodes for a high number of voltage levels causing more conduction losses and generating reverse recovery currents that affect the switching power loss of the overall system [12]. In the FC multilevel inverters, the increased number of high voltage capacitors leads to bulky equipment, high cost, and complex control methods to balance the voltages of both flying and DC-link capacitors. To overcome these constraints, researchers and authors investigated and proposed many hybrid topologies: Active Neutral Point Clamped type that combines NPC and FC structures. The authors of [12] propose a 7S-5L-ANPC topology with only 7 actives switches by leg: one interrupter and ten clamping diodes less than the NPC structure. In [13], the researchers upgrade the structure of 8S-5L-ANPC to an interesting 10S-9L-MANPC topology by adding a two-level converter leg, but they still use a flying capacitor. In [14], one proposes a new topology of a 9-Level Voltage Inverter using only 9 active power switches. The CHB topology includes the series connection of several H-bridges. It is applied for various applications due to its simplified model that can be categorized into symmetrical and asymmetrical topologies. The use of asymmetric CHB structures allows the further increase of the number of levels therefore the quality of the output signals without increasing the switch number [15]. The series connection of two H-Bridges with asymmetries ratio 1:3 can produce 9 voltage levels using only 8 switches instead of 16. The authors of [16] implement an interesting 27-level inverter using three cascaded H-Bridge (12 switches) with asymmetries ratio 1:3:9.

The main objective of this paper is to propose an improved topology of the Multilevel Inverter, based on two cascaded asymmetrical stages that significantly decrease the number of active power switches and reduce the Switching losses which are directly linked to the frequency PWM operation. Based on this, a novel topology of a 25-Level inverter is developed. Our proposed topology generates a staircase output voltage waveform with 25 levels using only ten switches, much less than forty-eight, the number of active switches used in the equivalent conventional topology, and without an excessive number of clamping diodes or flying capacitors used in NPC, FC, or Hybrid structures. The reduced costs, volume, and control complexity in this novel solution will certainly lead to its adoption in a large range of voltage levels photovoltaic systems. The active elements of this solution can be distributed in such a way that each stage can be connected to a different photovoltaic string. However, the control and the modulation strategy that must be developed will be very elaborate and complicated.

The rest of the paper is organized as: Section 2 presents the operating principle of the ten-switch 25-level proposed topology based on two cascaded asymmetric T-Bridges. A deep comparison between our multilevel inverter and other topologies (NPC, FC, CHB, MMC, ANPC) in terms of the number of required components, system volume, device voltage stress, and efficiency is also developed. In Section 3, we detail the multilevel control strategy which consists of a Modified Hybrid Multilevel Pulse Width Modulation Method (MHMPWM) elaborate for controlling our asymmetrical Cascaded T-Bridges. At the end of this section, we propose the block diagram of the proposed MHMPWM circuit controlling the ten active semiconductor switches. In Section 4, the verification and simulation results are reported in two cases: with and without PWM Control. The different illustrations justify the correct operation and the good performance of our complete multilevel solution. Finally, this paper is concluded in Section 5.
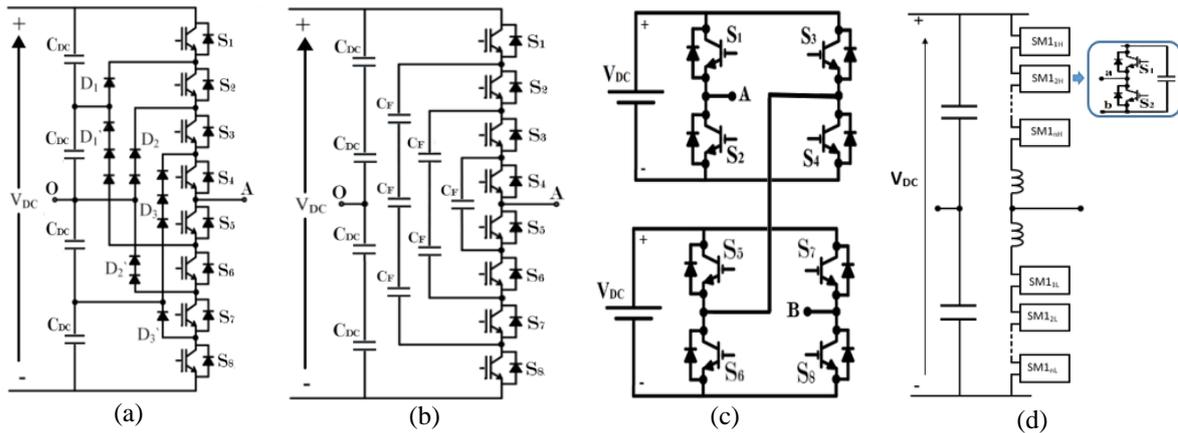
Figure 1. Conventional multilevel topologies, (a) NPC; (b) flying capacitors; (c) cascade H-bridge, (d) modular multilevel converters

2. OPERATING PRINCIPLES OF THE PROPOSED 25-LEVEL CASCADED T-BRIDGE VOLTAGE INVERTER

2.1. New multilevel structure design from basic submodules

During the last few years, in their investigation and search for better solutions, several authors have worked on topologies derived from conventional structures [17]-[19] others on modular structures by assembling several basic units depends on the desired output signal quality and the voltage rating of the semiconductor power switches. Each of these multilevels solutions has benefits and limitations and can be classified into two categories: Topologies with inherent negative voltage levels and topologies with negative voltage levels by H-bridge [20], [21].

In Power Electronics, the basic submodule half-bridge structure (SM1) shown in Figure 2 (a), has two modes and provides two voltage levels (V_{DC} or 0) at output terminals (a, c). In Figure 2 (b), the H-bridge basic module (SM2) is developed by combining two submodules (SM1) in parallel and operates one DC source. SM2 can generate three voltage levels (V_{DC}, 0, - V_{DC}) at the output terminals (a, b). The combination of two submodules (SM1) mounted in antiparallel, allows the creation of the T-type derived submodule (SM3) shown in Figure 2 (c). The T-type structure generates three unipolar voltage levels (0, V_{DC}, 2V_{DC}) at terminals (a, b). The parallel connection of submodules SM1 and SM3 makes these voltages bipolar and leads to the creation of the T-Bridge structure as depicted in Figure 3. The T-Bridge is then considered as a 5-level inverter structure that can generate (2 V_{DC}, V_{DC}, 0, - V_{DC}, 2V_{DC}). In this operation, the T-Bridge uses only five active switches instead of eight and more other components like clamping diodes, flying capacitors, and isolated DC sources in classical topologies. In this structure, we are in a configuration where $N_S = N_L$ more less than 2(N_L-1) [21]. The authors of [22] propose an interesting 31-level structure with only 14 switches and 4 asymmetric DC sources.

In the T-Bridge topology, the five power switches have different voltage stress: S_1, S_2, S_3, and S_4 need to block unipolar voltage 2V_{DC} whereas the switch S_5 needs to block the bipolar voltage V_{DC} and –V_{DC}. Therefore, to significantly increase the number of voltage levels and remarkably reduce the switches and components count, we develop a new topology of a 25-Level inverter based on two cascaded asymmetrical T-Bridges using only ten switches as depicted in Figure 3.
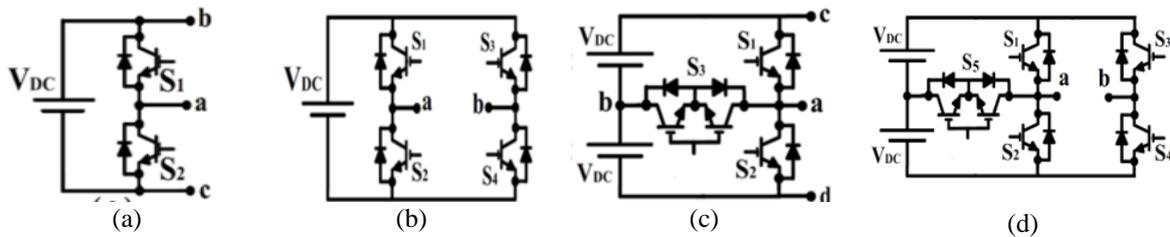

Figure 2. Main submodules (SMs) used as basic units of multilevel converters: (a) SM1, half-bridge; (b) SM2, H-bridge; (c) SM3, T-type derived submodule; (d) T-bridge derived module for generating five voltage levels
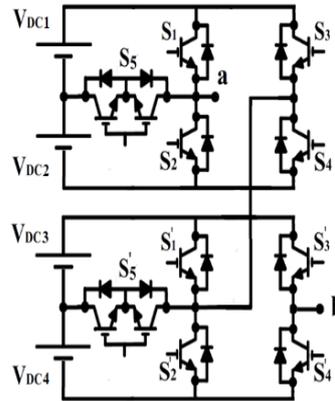
Figure 3. Scheme of the 10-switch 25-level voltage inverter based on two cascaded asymmetric T-bridge modules

2.2. Basic operating principle of 10S-25L voltage inverter

The proposed topology is composed of two cascaded asymmetric sub-circuits using four DC supplies. Each sub-circuit is a T-bridge consisting of two basic units: T-type (SM3) and Half-bridge (SM1) submodules. Each T-bridge stage generates five voltage levels. By combining the possibilities of each stage, our multilevel inverter can provide up to 25 voltage levels. Table 1 and Figure 4 illustrate the switches states for many output voltages levels. The concept of this structure can be simply extended to obtain more voltage levels by adding more cascading T-bridges.
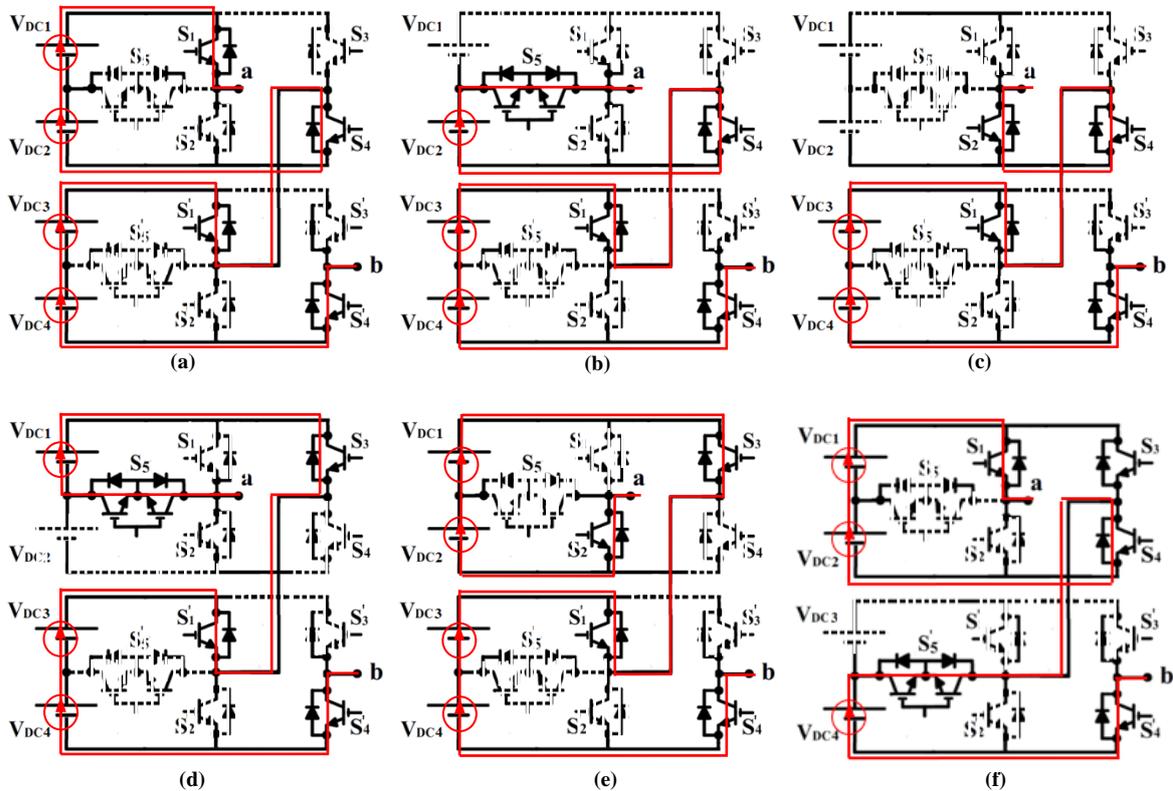

Figure 4. Switching states of our Cascaded two T-Bridge with reduced switches count:
(a) $V_{ab} = V_{DC4}+V_{DC3}+V_{DC2}+V_{DC1}$; (b) $V_{ab} = V_{DC4}+V_{DC3}+V_{DC2}$; (c) $V_{ab} = V_{DC4}+V_{DC3}$; (d) $V_{ab} = V_{DC4}+V_{DC3}-V_{DC1}$; (e) $V_{ab} = V_{DC4}+V_{DC3}-V_{DC2}-V_{DC1}$; (f) $V_{ab} = V_{DC4}+V_{DC2}+V_{DC1}$

Table 1. Switches states for twenty-five output voltage levels

State	V_{ab}	Switches States									
		S_1	S_2	S_3	S_4	S_5	S'_1	S'_2	S'_3	S'_4	S'_5
1	$V_{DC4}+V_{DC3}+V_{DC2}+V_{DC1}$	1	0	0	1	0	1	0	0	1	0
2	$V_{DC4}+V_{DC3}+V_{DC2}$	0	0	0	1	1	1	0	0	1	0
3	$V_{DC4}+V_{DC3}$	0	1	0	1	0	1	0	0	1	0
4	$V_{DC4}+V_{DC3}-V_{DC1}$	0	0	1	0	1	1	0	0	1	0
5	$V_{DC4}+V_{DC3}-V_{DC2}-V_{DC1}$	0	1	1	0	0	1	0	0	1	0
6	$V_{DC4}+V_{DC2}+V_{DC1}$	1	0	0	1	0	0	0	0	1	1
7	$V_{DC4}+V_{DC2}$	0	0	0	1	1	0	0	0	1	1
8	V_{DC4}	0	1	0	1	0	0	0	0	1	1
9	$V_{DC4}-V_{DC1}$	0	0	1	0	1	0	0	0	1	1
10	$V_{DC4}-V_{DC2}-V_{DC1}$	0	1	1	0	0	0	0	0	1	1
11	$V_{DC2}+V_{DC1}$	1	0	0	1	0	0	1	0	1	0
12	V_{DC2}	0	0	0	1	1	0	1	0	1	0
13	0	0	1	0	1	0	0	1	0	1	0
14	$-V_{DC1}$	0	0	1	0	1	1	0	1	0	0
15	$-V_{DC2}-V_{DC1}$	0	1	1	0	0	1	0	1	0	0
16	$-V_{DC3}+V_{DC2}+V_{DC1}$	1	0	0	1	0	0	0	1	0	1
17	$-V_{DC3}+V_{DC2}$	0	0	0	1	1	0	0	1	0	1
18	$-V_{DC3}$	0	1	0	1	0	0	0	1	0	1
19	$-V_{DC3}-V_{DC1}$	0	0	1	0	1	0	0	1	0	1
20	$-V_{DC3}-V_{DC2}-V_{DC1}$	0	1	1	0	0	0	0	1	0	1
21	$-V_{DC4}-V_{DC3}+V_{DC2}+V_{DC1}$	1	0	0	1	0	0	1	1	0	0
22	$-V_{DC4}-V_{DC3}+V_{DC2}$	0	0	0	1	1	0	1	1	0	0
23	$-V_{DC4}-V_{DC3}$	0	1	0	1	0	0	1	1	0	0
24	$-V_{DC4}-V_{DC3}-V_{DC1}$	0	0	1	0	1	0	1	1	0	0
25	$-V_{DC4}-V_{DC3}-V_{DC2}-V_{DC1}$	0	1	1	0	0	0	1	1	0	0

A careful analysis of the Table 1 shows that the choice of the $\mathbf{V_{DCi}}$ values is very important and must allow the following criteria: i) the output voltage must be symmetrical with respect to zero; ii) the values of the zones A, B, C, D, and E must not overlap; iii) the step between the different values must be constant. For this purpose, we deduce the essential relationships between the different V_{DCi} voltages:

$$V_{DC2} = V_{DC1} = V_{DC}$$

$$V_{DC4} = V_{DC3} = 5V_{DC}$$

As depicted in Figure 5, the proposed topology then becomes a cascade of two Asymmetric T-bridge stages: i) a Low Voltage stage generating at its terminals the five levels ($-2V_{DC}$, $-V_{DC}$, 0, V_{DC}, $2V_{DC}$); and ii) a High Voltage stage also generating five levels ($-10V_{DC}$, $-5V_{DC}$, 0, $5V_{DC}$, $10V_{DC}$). Table 2 shows the states of the HV and LV stage switches for output voltage values ranging from $-12V_{DC}$ to $+12V_{DC}$.
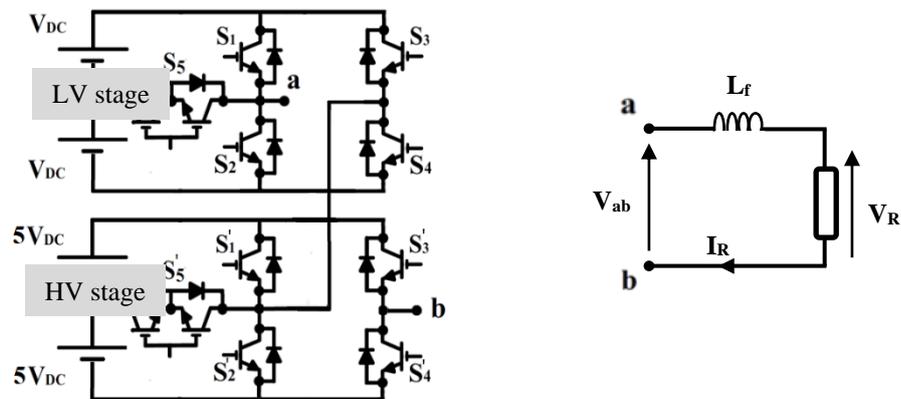

Figure 5. Scheme of two Cascaded T-Bridge stages with asymmetric DC source ratio 1:5. The multilevel output terminals are connected to a "L-filter" and an output load

Table 2. 5n-level zone and common switches states for the HV and LV stages

State	V_{ab}	5n-Level Zone	HV Stage V_{S_HV}	LV Stage V_{S_LV}	S_1	S_2	S_3	S_4	S_5	S'_1	S'_2	S'_3	S'_4	S'_5
1	$12\,V_{DC}$			$2\,V_{DC}$	1	0	0	1	0					
2	$11\,V_{DC}$			V_{DC}	0	0	0	1	1					
3	$10\,V_{DC}$	A	$10\,V_{DC}$	0	0	1	0	1	0	1	0	0	1	0
4	$9\,V_{DC}$			$-V_{DC}$	0	0	1	0	1					
5	$8\,V_{DC}$			$-2\,V_{DC}$	0	1	1	0	0					
6	$7\,V_{DC}$			$2\,V_{DC}$	1	0	0	1	0					
7	$6\,V_{DC}$			V_{DC}	0	0	0	1	1					
8	$5\,V_{DC}$	B	$5\,V_{DC}$	0	0	1	0	1	0	0	0	0	1	1
9	$4\,V_{DC}$			$-V_{DC}$	0	0	1	0	1					
10	$3\,V_{DC}$			$-2\,V_{DC}$	0	1	1	0	0					
11	$2\,V_{DC}$			$2\,V_{DC}$	1	0	0	1	0					
12	V_{DC}			V_{DC}	0	0	0	1	1	0	1	0	1	0
13	0	C	0	0	0	1	0	1	0					
14	$-V_{DC}$			$-V_{DC}$	0	0	1	0	1	1	0	1	0	0
15	$-2\,V_{DC}$			$-2\,V_{DC}$	0	1	1	0	0					
16	$-3\,V_{DC}$			$2\,V_{DC}$	1	0	0	1	0					
17	$-4\,V_{DC}$			V_{DC}	0	0	0	1	1					
18	$-5\,V_{DC}$	D	$-5\,V_{DC}$	0	0	1	0	1	0	0	0	1	0	1
19	$-6\,V_{DC}$			$-V_{DC}$	0	0	1	0	1					
20	$-7\,V_{DC}$			$-2\,V_{DC}$	0	1	1	0	0					
21	$-8\,V_{DC}$			$2\,V_{DC}$	1	0	0	1	0					
22	$-9\,V_{DC}$			V_{DC}	0	0	0	1	1					
23	$-10\,V_{DC}$	E	$-10\,V_{DC}$	0	0	1	0	1	0	0	1	1	0	0
24	$-11\,V_{DC}$			$-V_{DC}$	0	0	1	0	1					
25	$-12\,V_{DC}$			$-2\,V_{DC}$	0	1	1	0	0					

2.3. Comparison between our 10S-25L voltage inverter and conventional multilevel topologies

It is important to compare the proposed 10S-25L Voltage Inverter to other equivalent structures in order to illustrate its advantages and strengths. The proposed multilevel inverter synthesizes 25 voltage levels at the output terminals using only ten active switches. In parallel, up to 48 active switches and more other components are needed in classical topologies. The comparison of this 25-level inverter with other existing nine-level topologies is summarized in Table 3.

Table 3. Comparison between our 10S-25LVI, 25L-NPC VI, 25L-FC VI, 27L-CHB VI and 25L-MMC VI in terms of system volume

	10S-25LVI	14S-31LVI [22]	27L-CHB VI [16]	25L-NPC VI	25L-FC VI	25L-MMC VI
Actives switches	10	14	12	48	48	48
Clamped diodes	0	0	0	552	0	0
Flying capacitors	0	0	0	0	276	24
DC sources or DC floating capacitors	4	4	3 (isolated sources)	24	24	24
THD-V (%)	3.21	3.35	7.07	--	--	--

The comparative analysis clearly shows that our 10-Switch 25-Level inverter topology is more interesting in terms of THD and it is less bulky and uses fewer electronic components and devices than many other recent and conventional topologies. However, it is noticeable that in this topology, the switches need to withstand different voltage stress:

− Switches S_1, S_2, S_3, and S_4 must be able to block a unipolar voltage equal to $2V_{DC}$;
− Switches S'_1, S'_2, S'_3, and S'_4 must be able to block a unipolar voltage equal to $10V_{DC}$;
− S_5 must withstand a bipolar voltage of V_{DC} and $-V_{DC}$;
− S'_5 must withstand a bipolar voltage of $5V_{DC}$ and $-5V_{DC}$.

3. PROPOSED MODIFIED HYBRID MULTILEVEL PWM CONTROL STRATEGY

Many publications and studies are presenting several modulation methods designed to improve harmonic characteristics, control dynamics, filter size, and switching loss. The multi-carrier-based sinusoidal pulse-width modulation (MSPWM) scheme is one of the most used modulation methods for multilevel structures [23], [24]. One distinguishes two conventional categories: Level-shifted PWM (LS-PWM) and

Phase-shifted PWM (PS-PWM). However, it should be noted that each special structure requires a dedicated control and modulation method. Thus, for this singular multilevel topology, special multilevel modulation control is needed and must be developed. As depicted in Figure 5, our 10S-25L Voltage Inverter is composed of two cascaded T-Bridges with asymmetric DC source ratio 1:5. The 25 voltage levels are obtained by merging each of the five combinations of the HV stage with the five combinations of the LV stage. The switching states and their corresponding voltage level are depicted in Table 2 making the operation and level generation process much more comprehensible. We first note 5 zones A, B, C, D, and E associated with the HV stage levels: $10V_{DC}$, $5V_{DC}$, 0, $-5V_{DC}$, and $-10V_{DC}$. It is observed that the states of the LV stage switches are redundant and do not depend on these zones but on the deviation of the output voltage from the voltage levels (V_{ab} - $5nV_{DC}$). The voltages delivered by the LV stage, whatever the zone, are: $2V_{DC}$, V_{DC}, 0, $-V_{DC}$, $-2V_{DC}$. So, the Multistep Modified Reference Voltage allowing the control of the LV stage will have the following recurrent expression:

$$V_{M2REF} = V_{REF} - 5n \qquad (1)$$

with $V_{REF} = M * 12 * \sin 2\pi f.t \ \& \ n \ in \ \{2, 1, 0, -1, -2\} / -2 \leq V_{M2REF} \leq 2$
        M defines the global PWM modulation index.

This structure is designed to operate in PWM and generate all the voltages of zones A, B, C, D, and E. It must also generate the intermediate voltages between the different zones: from (+/-) $2V_{DC}$ to (+/-) $3V_{DC}$ and from (+/-) $7V_{DC}$ to (+/-) $8V_{DC}$. For these intermediate zones, we consider dedicated PWM comparators where the modified modulating reference signal must be reduced to a voltage between 0 and 1V. For these intermediate zones, the comparator operates both stages: (S_1, S_4) of the LV stage and (S'_2, S'_3) of the HV stage. Two decoder circuits are designed to identify each of the 5n level zones and each of the intermediate zones. Inspired by the control realized in a previous work [12], we design a circuit able to generate the gate pulses of the LV stage's semiconductor switches. The modified modulating reference signal V_{M2REF} is transformed into a unipolar signal V_{UM2REF} varying between 0 and 2V.

$$V_{UM2REF}(t) = V_{M2REF}(t) + 2 \left(\frac{1 - sgn(V_{M2REF}(t))}{2} \right) \qquad (2)$$

with

$$sgn(v) = \begin{cases} 1 \ when \ v \geq 0 \\ -1 \ when \ v < 0 \end{cases}$$

The switches S_3 and S_4 are clamping to a high or low state depending on the sign of the modified modulating reference signal V_{M2REF}: the switch S_4 is ON when V_{M2REF} is positive and S_3 is in a high state in the opposite case. The unipolar modified modulating reference signal V_{UM2REF} depicted in Figure 6 is compared to two triangular carrier bands, which are level-shifted incrementally by 1with the same amplitude 1 in order to generate the PWM commands for the three power semiconductors (S_1, S_2, S_5). Figures 7 (a)-(d) shows the block diagram of the electronic circuit implementing MHMPWM control.
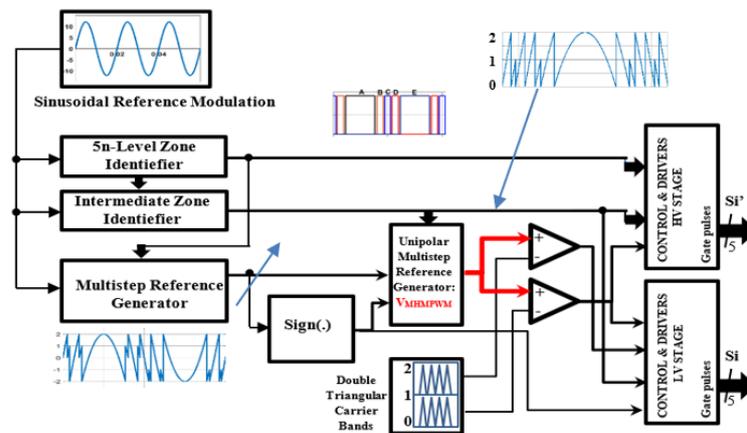

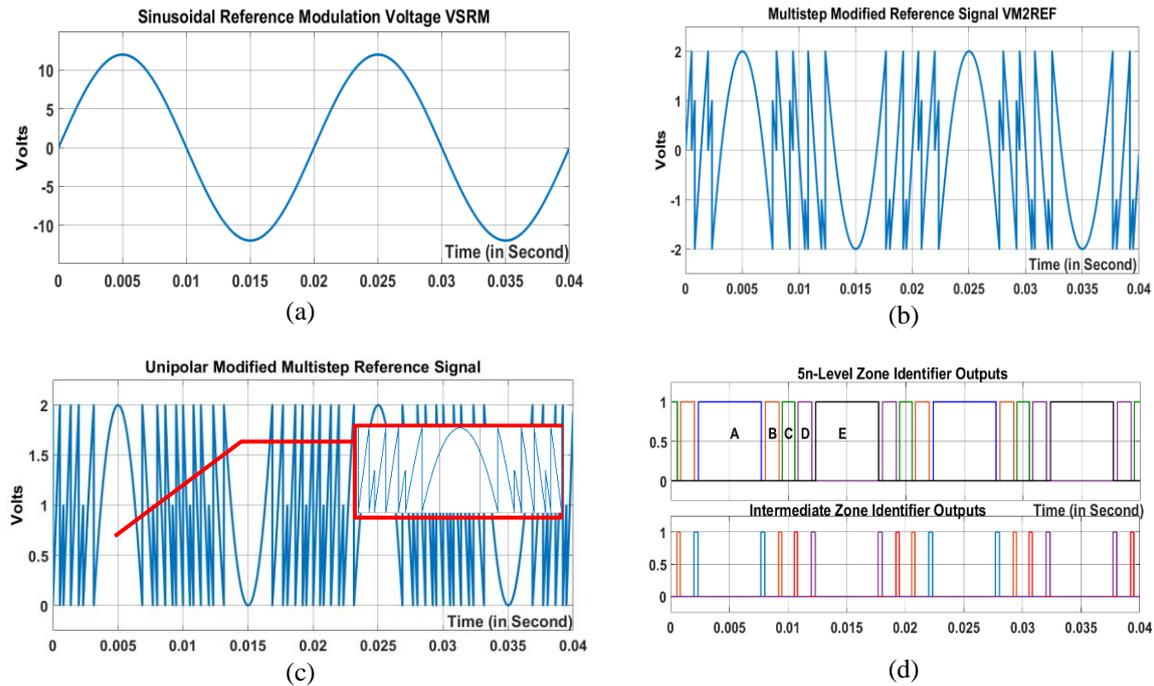Figure 6. Block diagram of the proposed MHMPWM scheme controlling the Ten power switches

Figure 7. Waveforms of the control signals: (a) Sine Reference Voltage of 12V amplitude and frequency 50 Hz; (b) Multistep Modified Reference Signal extracted from **V$_{SRM}$**; (c) Unipolar Multistep Modified Reference to compare with the two triangular carrier bands ; (d) 5n-Level and Intermediate Zone Identifier Outputs

4.   RESULTS AND DISCUSSION

In this section, a single-phase 10-switch 25-level voltage inverter with an output L-filter is modeled using MATLAB/Simulink. To evaluate the performance of our multilevel inverter, we test it with non-high switching frequency further reduce the switching power losses in semiconductors components. Our goal is to generate a sinusoidal voltage with amplitude and frequency fixed by the reference signal with improved harmonics characteristics (THD), minimum switching loss and minimum cost and size of L-filter at the system output. Table 4 summarizes the considered simulation parameters for the multilevel voltage system.

Table 4. Simulation multilevel system parameters

Parameters	Symbol	Numerical values
DC Source Voltage	V_{DC}	100V
Output filter	L_f	5mH
Switching frequency	f_{PWM}	2kHz
Reference signal: Pulsation & Modulation Index	ω	100π
	M	1
Load Active Power	P	20kW
Load Nominal Voltage (RMS) & Frequency	V_N - f_N	1000V - 50Hz

In this section, the obtained simulated results are discussed. It is intended to confirm the good performance of our multilevel inverter with its elaborate control. It is then easy to demonstrate that the objectives of this work are fully achieved. Figure 7 shows the synthesis of the signals allowing the PWM control during all the phases and zones of the sine reference signal evolution in detail. Figure 8 (a) shows that, even without PWM control, the output voltage delivered by the inverter is a perfectly sinusoidal stepped signal of 25 levels. Its harmonic distortion rate is 3.27% as depicted in Figure 8 (b). Figures 8 (c) and (e) illustrate respectively that the voltage V$_R$ and current I$_S$ at the output of the L-filter are quasi sinusoidal with a THD of 0.67% as shown in Figures 8 (d) and (f). These THDs (3.27%, 0.67%) are well within the standards recommended by the Institute of Electrical and Electronics Engineers (IEEE).
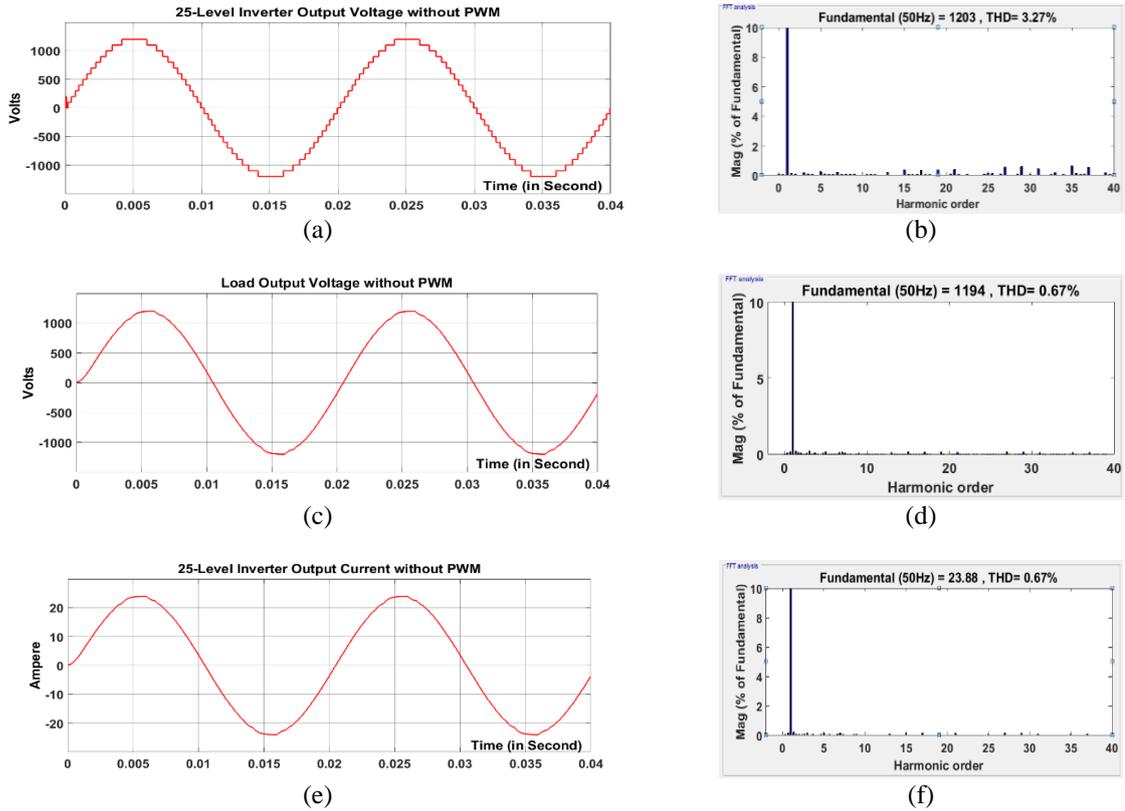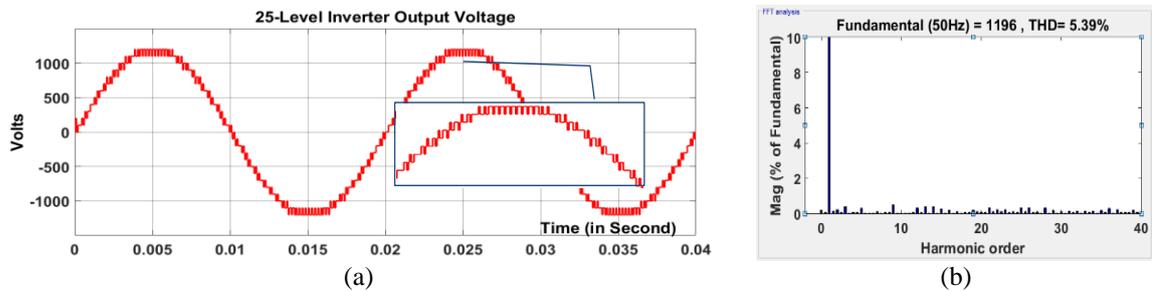
(a)

(b)

(c)

(d)

(e)

(f)

Figure 8. Waveforms of the Output signals and their Harmonic Spectrum without PWM command: a) 25-Level Inverter output Voltage V_{AB} of amplitude 1200V and frequency 50 Hz; b) V_{AB} harmonic spectrum; c) V_R the output voltage across the resistive load ; d) V_R harmonic spectrum THD_V; e) Load output current; f) its harmonic spectrum THD_I

Figure 9 shows the inverter output signals when the MHMPWM control is operated. As depicted in Figure 9 (a), the inverter output voltage waveform shows that our Cascaded asymmetrical structure with Modified Hybrid Multilevel PWM command worked well: we have 25 voltage levels perfectly modulated in time according to the sine reference voltage. PWM switching takes place for the most part in the LV stage, thus minimizing the harmonic distortion rates: $THD\_V_{AB}=5.39\%$ as shown in Figure 9 (b), $THD\_I_S=THD\_V_R=082\%$ in Figures 9 (d) and (f). Subsequently the switching losses are minimizing. Figures 9 (c) and (e) also illustrate respectively that the voltage V_R and current I_S at the output of the L-filter are quasi sinusoidal. After modeling the entire system as shown in Figure 5, this power multilevel converter can be controlled by a linear or nonlinear regulator (PID, backstepping, sliding mode…) to ensure good performance with respect to disturbances [25].
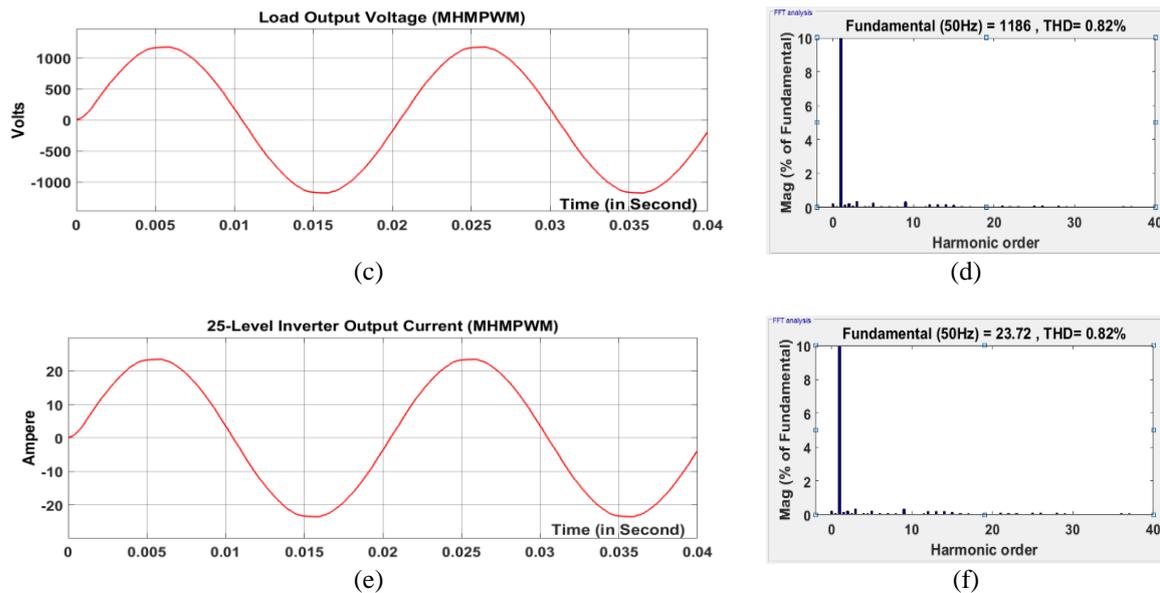

(a)

(b)

Figure 9. Waveforms of the output signals and their harmonic spectrum with MHMPWM command: (a) 25-level inverter output voltage V_{AB} of amplitude 1200V and frequency 50 Hz; (b) V_{AB} harmonic spectrum; (c) V_R the output voltage across the resistive load; (d) V_R harmonic spectrum THD_V; (e) Load output current; (f) its harmonic spectrum.

5. CONCLUSION

In this paper, a novel 25-Level inverter topology has been proposed with many benefits and features: very reduced count part, highly sinusoidal output signals with low harmonic content and reduced commutation losses. As depicted in the comparison with the other inverter's topologies, it requires only TEN active switches for a single-phase converter. The design of this cascaded asymmetric structure from basic submodules has been developed and detailed. The operating principles and switching states are presented. A detailed comparison between the proposed and the conventional topologies in terms of the number of switches, system volume, voltage stress, and switching loss is made. The development of a specific modulation strategy of the 10S-25L VI has been proposed. It consists of a modified hybrid multilevel PWM method essentially based on a unipolar multistep modified reference control signal and with outputs decoding operating areas. According to simulation results, the validity and advantages of the proposed topology and modulation method are demonstrated. Therefore, the proposed 25-Level inverter is a suitable and improved solution that can be used in E-mobility and grid-tie PV systems applications.

REFERENCES

[1] R. Majdoul, A. Abouloifa, E. Abdelmounim, M. Aboulfatah, A. Touati, and A. Moutabir, "Backstepping controller of five-level three-phase inverter," in *MATEC Web of Conferences, EDP Sciences*, vol. 16 no. 06003, May 2014, doi: 10.1051/matecconf/20141606003.

[2] A. Sheir, M. Z. Youssef, and M. Orabi, "A novel bidirectional T-type multilevel inverter for electric vehicle applications," in *IEEE Transactions on Power Electronics,* vol. 34, no. 7, pp. 6648-6658, July 2019, doi: 10.1109/TPEL.2018.2871624.

[3] N. Flourentzou, V. G. Agelidis, and G. D. Demetriades "VSC-based HVDC power transmission systems: an overview," *IEEE Transactions on Power Electronics*, vol. 24, no. 3, pp. 592-602, March 2009, doi: 10.1109/TPEL.2008.2008441.

[4] M. A. Perez, S. Bernet, J. Rodriguez, S. Kouro, and R. Lizana "Circuit topologies, modeling, control schemes, and applications of modular multilevel converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 4-17, Jan. 2015, doi: 10.1109/TPEL.2014.2310127.

[5] J. Venkataramanaiah, Y. Suresh, and A. K. Panda, "A review on symmetric, asymmetric, hybrid and single DC sources based multilevel inverter topologies," *Elsevier J. Renewable and Sustainable Energy Reviews*, vol. 76, pp. 788-812, Sep. 2017.

[6] M. J. Mojibian, and M. T. Bina, "Classification of multilevel converters with a modular reduced structure: implementing a prominent 31-level 5 kVA class B converter," *IET Power Electronics*, vol. 8, no. 1, pp. 20-32, 1 2015, doi: 10.1049/iet-pel.2013.0872.

[7]   J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," in *IEEE Transactions on Industrial Electronics*, vol. 54, no. 6, pp. 2930-2945, Dec. 2007, doi: 10.1109/TIE.2007.907044.

[8]   A. Nabae, I. Takahashi, and H. Akagi, "A neutral-point clamped PWM inverter," *IEEE Transactions on Industrial Applications*, vol. 1A-17, no. 5, pp. 518-523, 1981, 10.1109/TIA.1981.4503992.

[9]   L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives," in *IEEE Transactions on Industrial Applications*, vol. 35, pp. 36-44, 1999, doi: 10.1109/28.740843.

[10] L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel inverters for electric vehicle applications," in *Proceedings of IEEE Workshop on Power Electronics in Tran*, Michigan, USA (1998), doi: 10.1109/PET.1998.731062.

[11] F. Z. Peng, J. W. McKeever, and D. J. Adams "Cascade multilevel inverters for utility applications," in *Proceedings of the IECON'97 23rd International Conference on Industrial Electronics, Control, and Instrumentation (Cat. No.97CH36066,* New Orleans USA 1997, doi: 10.1109/IECON.1997.671773.

[12] H. Wang, L. Kou, Y.-F. Liu, and P. C. Sen, "A seven-switch five-level active-neutral-point-clamped converter and its optimal modulation strategy," in *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5146-5161, July 2017, doi: 10.1109/TPEL.2016.2614265.

[13] N. Sandeep, and U. R. Yaragatti, "Operation and control of a nine-level modified ANPC inverter topology with reduced part count for grid-connected applications," in *IEEE Transactions on Industrial Electronics*, vol. 65, no. 6, pp. 4810-4818, June 2018, doi: 10.1109/TIE.2017.2774723.

[14] R. Majdoul, A. Touati, A. Ouchatti, A. Taouni, and E. Abdelmounim "A nine-switch nine-level converter new topology with optimal modulation control," in *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 12, no. 2, pp. 932-942, June 2021, doi: 10.11591/ijpeds.v12.i2.pp932-942.

[15] F. Briz, M. Lopez, A. Rodriguez, and M. Arias, "Modular power electronic transformers: modular multilevel converter versus cascaded h-bridge solutions," in *IEEE Ind. Electron. Mag.* Vol. 10, no. 4, 2016, doi: 10.1109/MIE.2016.2611648.

[16] P. Gaisse, et al., "Improved predictive control for an asymmetric multilevel converter for photovoltaic energy," *Sustainability* 2020, 12, no. 15: 6204. https://doi.org/10.3390/su12156204

[17] Y. Liu, et al., "A Modular Multilevel Converter with Self Voltage Balancing," 2019 *IEEE Applied Power Electronics Conference and Exposition (APEC),* Anaheim, CA, USA, 2019, pp. 97-111.

[18] P. Barbosa, P. Steimer, L. Meysenc, M. Winkelnkemper, J. Steinke, and N. Celanovic "Active neutral-point-clamped multilevel converters," in *2005 IEEE 36th Power Electronics Specialists Conference*, Recife, 2005, pp. 2296-2301, doi: 10.1109/PESC.2005.1581952.

[19] A. K. Sadigh, V. Dargahi, and K. A. Corzine, "Analytical determination of conduction and switching power losses in flying-capacitor-based active neutral-point-clamped multilevel converter," in *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5473-5494, Aug. 2016, doi: 10.1109/TPEL.2015.2498107.

[20] R. Razani, M. H. Ravanji, and M. Parniani, "Enhanced hybrid modular multilevel converter with improved reliability and performance characteristics," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3139-3149, April 2019, doi: 10.1109/TPEL.2018.2853625.

[21] M. Vijeh, M. Rezanejad, E. Samadaei, and K. Bertilsson "A general review of multilevel inverters based on main submodules: structural point of view," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9479-9502, Oct. 2019, doi: 10.1109/TPEL.2018.2890649.

[22] D. Prasad, C. Dhanamjayulu, S. Padmanaban, J. B. Holm-Nielsen, F. Blaabjerg, and S. R. Khasim, "Design and implementation of 31-level asymmetrical inverter with reduced components," in *IEEE Access*, Special Section on Evolving Technologies in Energy Storage Systems for Energy Systems Applications, vol. 9, January 2021, doi: 10.1109/ACCESS.2021.3055368.

[23] B. Li, R. Yang, D. Xu, G. Wang, W. Wang, and D. Xu, "Analysis of the phase-shifted carrier modulation for modular multilevel converters," in *IEEE Transactions on Power Electronics*, vol. 30, no. 1, pp. 297-310, Jan. 2015, doi: 10.1109/TPEL.2014.2299802.

[24] S. Kouro *et al.*, "Recent advances and industrial applications of multilevel converters," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 8, pp. 2553-2580, Aug. 2010, doi: 10.1109/TIE.2010.2049719.

[25] R. Majdoul, E. Abdelmounim, M. Aboulfatah, and A. Abouloifa, "The performance comparative of backstepping, sliding mode and PID controllers designed for a single-phase inverter UPS," *2014 International Conference on Multimedia Computing and Systems (ICMCS),* Marrakech, 2014, pp. 1584-1589, doi: 10.1109/ICMCS.2014.6911310.

BIOGRAPHIES OF AUTHORS

Radouane Majdoul was born in Meknes, Morocco, in 1969. He received the Engineer degree in electrical Engineering from High Institute of Technical Education (ENSET) of Rabat in 1991. In 1997, he successfully passed the external aggregation contest. In 2012 and 2017 he received respectively the M.Sc and Ph.D in Automatic Signal Processing and Industrial Computing from HASSAN 1st University – FST of Settat Morocco. In 2018, he joined the Hassan 2 University of Casablanca, Morocco. Currently he is Research Professor in Laboratory of Complex Cyber Physical Systems at National High School of Arts and Crafts ENSAM, Department of Electrical Engineering. His research interests include control strategies for Power Electronics Converters, Multilevel inverters, PV systems, AC machine Drives, renewable energy, Smart-Grids, and Power to X.

Abdelwahed Touati was born in Casablanca, Morocco, in 1970. He received the Engineer degree in electrical Engineering from High Institute of Technical Education (ENSET) of Mohammedia in 1993. In 1999, he successfully passed the external aggregation contest. In 2012 he received the MASTER ATSII (Automatic Signal Processing and Industrial Computing) from HASSAN 1 University – FST of SETTAT Morocco. Currently he is Research Professor Laboratory of Structural Engineering, Intelligent Systems & Electrical Energy at National High School of Arts and Crafts ENSAM, Department of Electrical Engineering - Hassan II University Casablanca, Morocco. His research interests include control strategies for AC machine Drives, Wind renewable energy and Power Quality.

Abderrahmane Ouchatti was born Morocco in 1972. He received the Engineer degree in electrical Engineering from High Institute of Technical Education (ENSET) of Rabat in 1994. Received the Aggregation in Electrical Engineering from ENSET, Rabat, in 2000. He received the Master degree in ATSII (Automatic, Signal Processing and Industrial Computing) from Faculty of Science and Technology Hassan 1st university SETTAT, Morocco in 2011. He received in 2018, the Ph.D degree in Industrial electronics and electrical machines from Engeneering Mohammadia high School of Rabat in Morocco. Currently he is Research Professor in Laboratory of Electrical Systems & Control Engineering (ESCE) – Aïn Chock Science faculty- Hassan II University Casablanca, Morocco. His research interests include control strategies for AC machine Drives, renewable energy and Multilevel converters.

Abderrahim Taouni was born in Morocco in 1974. He received the Engineer degree in electrical Engineering from High Institute of Technical Education (ENSET) of Mohammedia in 1997. Received the Aggregation in Electrical Engineering from the Ecole Normal Superior of Technical Education (ENSET), Rabat, in 2008. He received the Master degree in ATSII (Automatic, Signal Processing and Industrial Computing) from Faculty of Science and Technology Hassan I university SETTAT, Morocco in 2011. Currently he is Research Professor Laboratory of Electrical Systems & Control Engineering (ESCE) – Aïn Chock Science faculty- Hassan II University Casablanca, Morocco. His research interests include control strategies for AC machine Drives, Power electronic converters, renewable energy and batteries.

Elhassane Abdelmounim received his PhD in applied Spectral analysis from Limoges University at science and technical Faculty, France in 1994. in 1996, he joined, as Professor, applied physics department of science and technical faculty, Hassan 1st University, Settat, Morocco. His current research interests include digital signal processing and machine learning. He is currently coordinator of a Bachelor of Science in electrical engineering and researcher in "ASTI" System Analysis and Information Technology Laboratory at science and technical faculty, Hassan 1st University, Settat, Morocco.