

Z-source reversing voltage multilevel inverter for photovoltaic applications with inherent voltage balancing

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Article Info

Article history:

Received May 6, 2021

Revised Jan 26, 2022

Accepted Feb 2, 2022

Keywords:

Maximum power point tracking

Multilevel inverters

Power electronic components

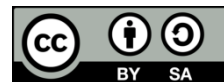
PV panel

Z-source converter

ABSTRACT

Photovoltaic (PV) inverters have been widely used in solar energy to change the direct current (DC) voltage of PV panels to the grid alternating current (AC) voltage. They are comprised of DC-DC section for maximum power point tracking (MPPT) and DC-AC part to provide required output AC voltage. This paper provides a unique configuration that integrates both sections in one part. A Z-source multilevel inverter is proposed based on Z-source networks and reversing voltage (RV) multilevel inverter. The Z-source network can be used to increase the level of the input voltages and MPPT as well. In addition, the prop used topology uses multilevel topology to accommodate more DC inputs and benefit from features of multilevel level inverters in AC output. Moreover, using Z-source network can minimize equated monthly installment (EMI) due to the lower stress on the semiconductor switches. Finally, a seven level topology is designed and simulated to show the performance of proposed topology.

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1. INTRODUCTION

One of the main components of solar energy conversion into electric energy is the inverter [1]. In order to extract maximum power from the panels, a direct current (DC)-DC converter is also incorporated in the inverter to increase the overall efficiency of conversion [2]. It is worth noting that new generation of inverters called multilevel inverters have found great attention in industry. Multilevel inverters have been the subject of many researches in recent years due to their superiority over the conventional three-level inverters in terms of capabilities to support medium voltage-high power applications, lower switching losses and lower voltage stress over switches, higher efficiency and high quality output waveform hence smaller output filter size [3], [4].

Some of the conventional multilevel inverters are diode clamped (DC) inverter, flying capacitor (FC) inverter and cascaded H-bridge (CHB) inverter. Each of these multilevel inverters has its own advantages and drawbacks [5]–[7]. Among the conventional multilevel converters, CHB has attracted great attention due to simplicity and effectiveness [8], [9]. Over the years a great number of topologies were designed to overcome those disadvantages and improve the performance of the multilevel inverters. A well known multilevel inverter that benefits from less number of switches and control circuits is reversing voltage (RV) multilevel inverter that divides the circuit into high frequency level generation part and low frequency polarity generation [10]. This will tremendously reduce the number of switches as well as control circuits. Therefore, this topology has been adopted for the purpose. Although some recent topologies claim higher number of output voltage levels with fewer components, they use some techniques such as asymmetric technique that needs different DC supply [11], [12]. This technique is not suitable for photovoltaic (PV)

inverters as the output voltage of PV modules are almost identical and managing different voltage levels may cause uncertainties and complexities specially during installations in PV plants. In a large scale PV plant, installation procedure shall be straight forward and simple to enable technicians at site avoid mistakes and faults during installation. Therefore, PV panels are selected from the same size and ratings to make the installation and wirings identical and coherent all over the site in contrast to asymmetric topologies that need different PV ratings for operation.

It is worth mentioning that solar panels provide DC voltage that should be scaled up to the required voltage for grid connected inverters. In addition, they shall be manipulated to extract maximum power from the panels (MPPT) [13]. Some research suggest using isolated DC-DC converters, but this approach need transformer and several more switches to make DC/AC/DC conversion [14]. Therefore, almost all photovoltaic (PV) inverters are transformerless due to cost and size concerns. In order to cover these necessities, a DC-DC converter is vital between the inverter and panels. Z- source converters are DC-DC converters that create less equated monthly installment (EMI) due to their switching structure and topology [15]. In this converter, X shaped LC network reduces the EMI generated during switching instances and creates a smoother output voltage [16]. So, this converter is a suitable option for DC-DC part of a PV inverter [17]. In addition, transformer less PV inverters that account for most of the PV inverters, shall consider leakage current due to PV panels capacitance with ground [18]. The Z-source converter can also solve the leakage current problem and this will add to the advantages of application of this converter in PV applications. While using Z-source topology for DC-DC conversion has been put into practice as three level Z-source inverter [19], [20], application Z source on a novel multilevel inverter (RV) is unique with advantages such as simpler control approach with less number of components that will be discussed.

In this paper, Z-source converter is used as an interface between multilevel inverter and PV output. While some research has done in this field, it is pertinent to note that PV applications need symmetric multilevel topologies and asymmetric topologies are not suitable for the applications [21]. In order to provide maximum flexibility during inverter operation and when the PV output of panels are not the same (for example during shading) each input is regulated separately with separate Z-source converters. Since, the multilevel topology in this research provides 7 level outputs with 3 input sources, three Z- source converters are utilized in this work. In order to control the overall system, a switching approach is also used to achieve the required output voltage. One of the main advantages of the proposed topology is the reduction of control signals for the system. It happens due to the integration of the DC-DC Z-source with the multilevel control approach and it eliminates extra control signals. Therefore, the control implementation of the method will be easier and needs less burden on the controller. The overall system as well as building blocks will be explained here after.

2. BASIC BUILDING BLOCKS

2.1. RV multilevel inverter

This topology is widely referred due to its simplicity and effectiveness [10]. The overall diagram of the topology is depicted in Figure 1. The topology is comprised of high frequency level generation part that is responsible for output voltage level generation and low frequency polarity generation that creates the appropriate output voltage polarity. The PV panels are considered as DC sources that should be connected to a Z-source converter before connecting to the inverter. It is pertinent to mention that some multilevel topologies claim less number of components at the expense of more complex control strategies or issues such as capacitor balancing [22].

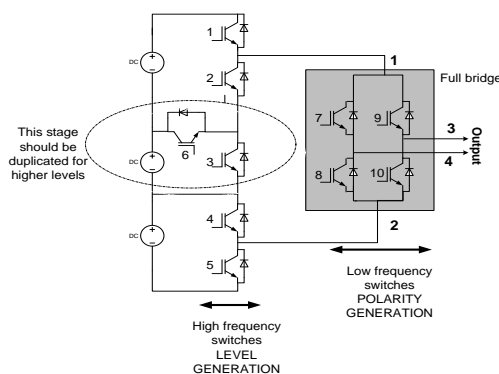


Figure 1. General schematic for RV topology

2.2. Z-source converter

Z-source converter should be integrated with the level generation part. So, it should be compatible with the current route of the inverter during switching instances. In order to avoid unwanted switching path and unusual output levels in the multilevel inverter high performance Z source (HPZ-source) converter is adopted as in Figure 2. This topology benefits from a bidirectional switch (sw_7) that avoids unwanted path during switching instances. Without this switch, uncontrolled unwanted output voltage levels may appear during some switching instances. In order to control converter output voltage, Shoot through happens in each switching period. In this case, output of the converter is short circuited and this time defines how much the output voltage will increase. the relation between shoot through and switching period with the overall voltage gain is as shown in (1).

$$\frac{V_o}{V_i} = \frac{1}{1-2\frac{t_0}{T}} \quad (1)$$

Where as V_o , V_i , T and t_0 are output voltage, input voltage switching period and shoot through time, respectively.

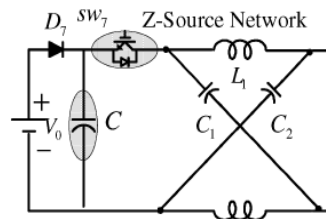


Figure 2. A general schematic for HPZ source network

3. PROPOSED TOPOLOGY

The proposed 7 level topology (RV-HPZSI) in PSIM software is depicted in Figure 3 combining HPZ source converter and RV multilevel. In Figure 3, diodes are named with the letter “D” and insulated gate bipolar transistor (IGBT) switches with “S” while capacitors and inductors are mentioned by “C” and “L”, respectively. Each DC source also represents a PV module in the Figure 3. The frequency of switching for high frequency switches (in level generation and Z-source part) is 6 KHz. The magnitude of inductors is 200 μ H and capacitors are 1000 μ F. In order to manage shoot through time and make sure that it happens correctly in all voltage levels, an innovative pulse width modulation (PWM) approach is adopted. In this case a shoot through level is defined in the diagram and modulator magnitude shall be less than that. When the highest carrier becomes greater than the shoot through level, shoot through happens. The PWM waveform schematic is illustrated in Figure 4 while the upper straight line refers to shoot through. Level (V_{sh}) in the Figure 4 determines the shoot through instances during intersections with the highest carrier (when carrier is greater than the line, shoot through starts and vice versa). This is because at this time, inverter output does not change and the shoot through that makes the output of Z-source converter temporarily zero does not affect output voltage. This is why this topology can omit extra control signals for the HPZ source inverter.

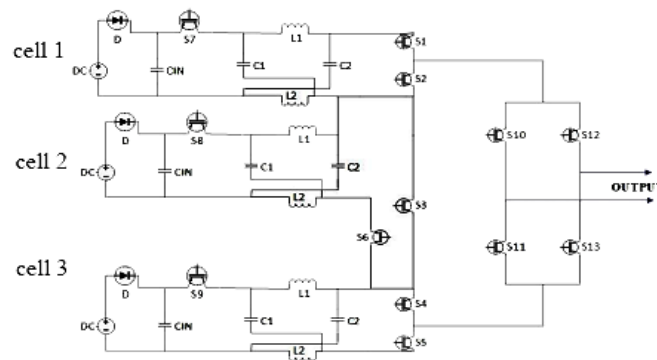


Figure 3. Proposed RV-HPZSI topology

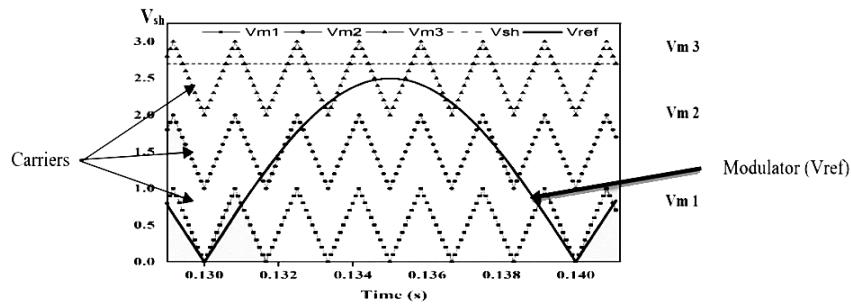


Figure 4. PWM waveforms for the proposed topology including modulator, carriers and shoot through level

DC voltage sources represent PV output voltage levels that are attached to the Z-source converters and finally to multilevel inverter. In order to define the switching pattern of the overall inverter, the following Table 1 is defined that show which switches are turned on in each instance. In this Table 1, a comparison is made between the highest carrier and the shoot through level (V_{sh}) and asterisk (*) shows no output or shoot through. In order to keep the capacitor voltage in balanced conditions, shoot through is done sequentially in the cells. Therefore, during the shoot through instances (that is found based on the comparison of the shoot through level and highest carrier), cells are selected cells are short circuited sequentially as defined in Table 1. The required switched to be switched on at these instances are also mentioned in Table 1.

Table 1. Proposed conducting switches for each output voltage level

Level	comparison	Shoot through cell	Output cell	ON switches
0	+	1	*	1,2,3,4,8,9
		2	*	2,3,4,6,7,9
		3	*	2,3,4,5,7,8
		*	*	2,3,4,7,8,9
1	+	1	3	1,2,3,5,8,9
		2	1	1,3,4,6,7,9
		3	2	2,4,5,6,7,8
		*	3	2,3,5,7,8,9
2	-	*	1	1,3,4,7,8,9
		*	2	2,4,6,7,8,9
		1	2,3	1,2,5,6,8,9
		2	1,3	1,3,5,6,7,9
3	+	3	1,2	1,4,5,6,7,8
		*	2,3	2,5,6,7,8,9
		*	1,3	1,3,5,7,8,9
		*	1,2	1,4,6,7,8,9
3	-	*	1,2,3	1,5,6,7,8,9

This Table 1 is calculated in order to distribute shoot through time, symmetrically between cells to avoid unbalanced DC supplies. Therefore, each cell is short circuited with multilevel inverter switches in a sequential way so that the output voltage is generated correctly while a cell is short circuited. The only level that can not provide shoot through and output voltage generation simultaneously is highest level (level 3). Since the shoot through level is selected higher than modulator, level generation and shoot through will not interfere in each other. In other words, shoot through happens when carrier is greater than shoot through level and 3 level output voltage is generated when modulator is larger than carrier and they do not coincide with each other because the shoot through level is always larger than modulator. It is worth mentioning that the frequency of shoot through in this case is one third of the switching frequency in the level generation section due to sequential nature of shoot through (each cell is short circuited after previous cell and there are three separate cells). This issue is well illustrated in the Figure 5 showing only shoot through level (V_{sh}) and highest carrier.

According to Figure 5, the shoot through level determines the timing for shoot through and is always higher than modulator. In addition as discussed above, shoot through is equally distributed between cells to balance the voltage among them. It is worth mentioning that based on (1) as the modulation level decreases, the shoot through level can also decrease respectively which leads to increase in its output due to greater shoot through time. In order to investigate the relation between the decrease in the maximum value of

modulator and increase in the overall output due to shoot through, the modulator is decreased from 2.9 to 2.3 and the respective output voltage is found and illustrated in the Figure 6. According to Figure 6, as the modulator level decreases, the time for shoot through can be increased that culminate in the overall increase in the output voltage level.

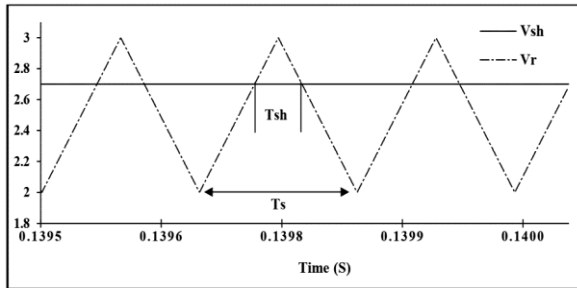


Figure 5. Shoot through timing in cells in a complete switching cycle

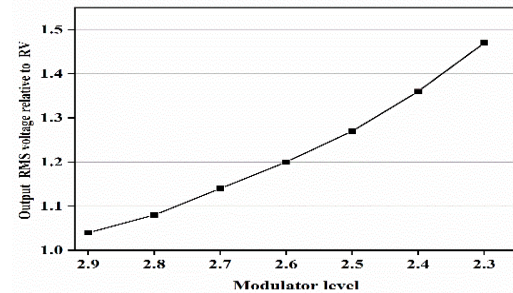


Figure 6. Overall output RMS voltage of proposed topology relative to overall output RMS voltage of RV topology in different modulator levels

4. SIMULATION RESULTS

In order to show the consequent output voltage of the proposed converter, simulation has been performed by PSIM based on the above mentioned approach. In this simulation, the primary DC sources are 50 V, level generation part frequency is 6 KHz with an output RL load (72 ohm and 30 mH). Based on above explanations, the frequency of shoot through in each cell in this case is one third of level generation frequency *i.e.* 2 KHz. The shoot through level (V_{sh}) is also considered 2.7.

Figure 7 depicts the Z-source cells output voltage. According to the figure, the shoot through is symmetrically distributed among cells to avoid any voltage unbalance. Moreover, it is only performed during special times while the cell voltage does not contribute in the output voltage and is governed by the shoot through level.

Finally, these levels are manipulated by RV inverter and the output voltage level is generated. Figure 8 illustrates the output voltage level based on the proposed converter. According to Figure 8, the output voltage is balanced without any disturbance from shoot through in the waveform. In order to illustrate the harmonic performance of the converter, the output voltage harmonic spectrum of the output voltage is also shown in Figure 8. The harmonic spectrum is the shown for the output voltage without any filter and the total harmonic distortion (THD) is 23.7%. Due to the high ripple of the output waveform and to minimize the output voltage THD a simple LC filter (1 mH, 200 μ F) is utilized. The tuning (resonance) frequency of the filter is 2.2 kHz that is well below switching frequency of the system (6 kHz) and can successfully remove the switching frequency harmonics. The results in Figure 9 illustrate that the waveform has been properly filtered and the THD is greatly reduced from 23% to less than 3%.

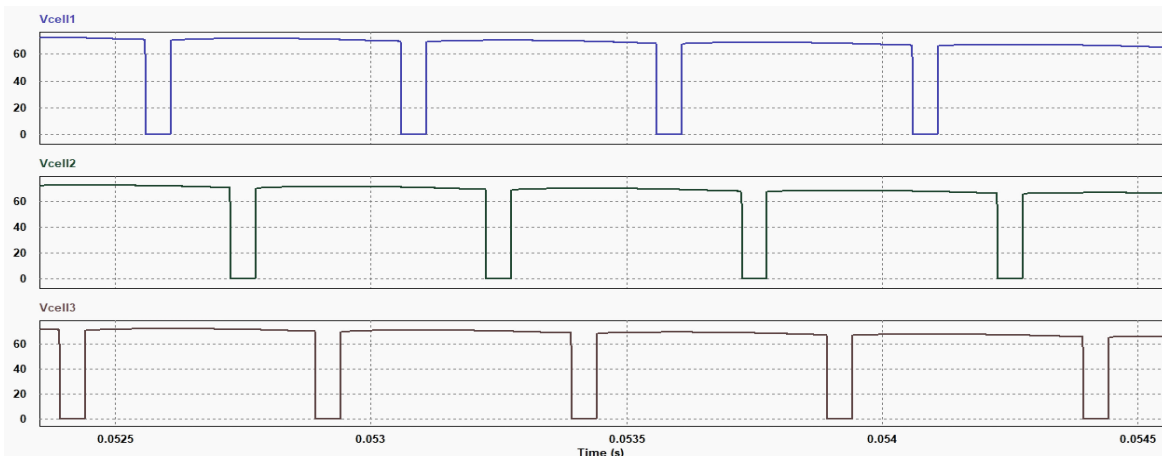


Figure 7. Z-source output voltage for different cells

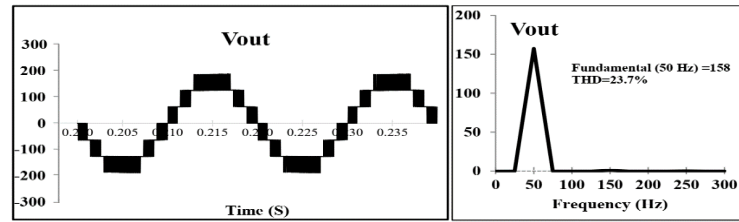


Figure 8. Proposed topology output voltage and harmonic spectrum without filter

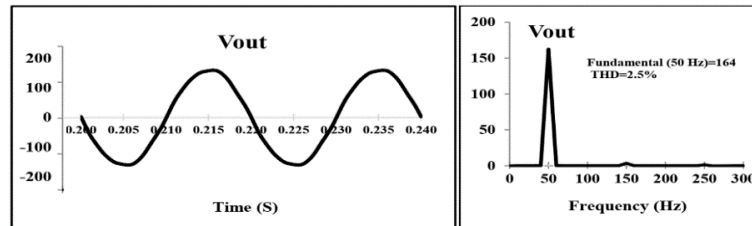


Figure 9. Output voltage and harmonic spectrum of the proposed inverter with LC harmonic filter

In order to compare the proposed topology with available research, the Table 2 is prepared that illustrates the comparison in terms of number of main components. Based on Table 2, the proposed topology has less number of overall semiconductor switches and diodes that lead to cost reduction of the converter. In addition, the topology benefit from less number of main switched that culminates in less complexity of the converter. Babaei and Ahmadzadeh [23] proposed a topology that suffers from unequal blocking voltage for diodes. It is worth mentioning that the compared topologies except [24] have the advantage of separate z source converters for manipulating separate MPPT function for PV applications. Matam *et al.* [24], proposed a topology with several floating capacitors that need extra circuit for balancing, hence increasing the complexities and size of the circuit. Prasad *et al.* [25], has suggested the topology which combines diode clamped topology with Z-source inverter. However, it suffers from too much number of diodes DC link capacitors. In addition, topologies such as [24] and [26] can only be used in cases where all panels encounter similar environment characteristics (shading) and a single MPPT be applied to them. In addition, this topology inherently avoids leakage currents due to PV parasitic capacitors without sophisticated and complex approaches [27].

Table 2. Comparison of components of proposed inverter with similar single phase 7 level topologies

	Proposed RV-HPZSI	Z source diode clamped inverter [25]	ISSCMLI [24]	Z-NPC [23]
DC Power supply	6	1	3	3
Main switch	12	13	12	10
Z source switch	0	1	0	3
Diode	12	2	9	3
Overall semiconductor switches and diodes	24	16	21	16
DC link capacitor	0	2	6	3
Floating capacitor	0	3	0	0

5. CONCLUSION

In this paper, a novel Z-source multilevel inverter topology is proposed. The topology makes it possible to increase output voltage magnitude by controlling shoot through in the Z-source sections. Moreover, the overall number of elements was less than other similar topologies making it a good candidate for multilevel inverter applications. The proposed PWM strategy was also explained for the proper controlling of the converter showing effective and simple approach for it. Finally, simulation waveforms were also presented in the paper showing the performance of the topology.





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