

A new direct current circuit breaker with current regeneration capability

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ABSTRACT

Direct current (DC) power systems are becoming very popular due to better control ability and equipment reliability thanks to the continuous development of power electronics. A DC circuit breaker (DCCB) used for current interruption in a DC network is a major part of the system. It plays the vital role of isolating networks during fault clearing as well as during normal load switching. Breaking the DC current is a major challenge as it does not have any natural zero crossing points like the AC current has. In addition, energy stored in the network inductances during normal operation opposes the instantaneous current breaking. Hence, all the conventional DC circuit breaker topologies use lossy elements to dissipate this stored energy as heat during the current breaking operation. However, it is possible to store this energy and reuse it later by developing an improvised topology. In this paper, the prospects of energy recovery and reuse in DC circuit breakers have been studied, and a new topology with regenerative current breaking capability has been proposed. This new topology can feed the stored energy of the network back into the same network after breaking the current and thus can improve the overall system efficiency.

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NOMENCLATURE

V_{DC}	: DC voltage source	η	: Energy recovery efficiency
V_S, I_S	: Source voltage, current	R_S, L_S	: Source resistor, inductor
P_S	: Source power	R_L	: Load resistor
I_{LOAD}	: Load current	C	: Capacitor
I_R	: Regenerated current	L	: Inductor
E_R	: Regenerated energy	D_1-D_2	: Diodes
I_L	: Inductor current	$S1-S2$: Mechanical switches
V_C, I_C	: Capacitor voltage, current	$T1-T2$: Thyristors
V_{S2}	: Voltage across mechanical switch (S2)	IGBT	: Insulated Gate Bipolar Transistor
V_{gT}	: Thyristor gate pulse	MOV	: Metal Oxide Varistor
V_{gI}	: IGBT gate control voltage	T_{trip}	: Current breaking time

1. INTRODUCTION

In the present era, dealing with direct current (DC) power systems has become significantly easier due to the stunning advancement of semiconductor technology and the continuous development of power electronics. With rapid growth in renewable energy resources (RES) and increasing demand for smart and efficient loads, DC power distribution systems can become the most suitable option for many applications. Meanwhile, there are a number of application areas where DC power systems are already in use, such as DC microgrid, HVDC transmission, electric vehicle, and electric traction load [1]. It is widely agreed that DC micro grids are also superior to AC micro grids in many ways, such as in terms of control simplicity, efficiency, reliability, RES integration, and connection of DC loads. However, despite having many advantages, designing an appropriate protection scheme for a DC power system poses a significant challenge [2]. Basically, the challenge originates from the nature of DC fault current, which during a sudden fault can rapidly rise to several times the normal load current and has no naturally occurring zero crossing point like AC has. Fast and efficient fault detection techniques, fault current limiting methods, proper grounding systems and an appropriate DC circuit breaker (DCCB) are required to address the challenges of DC system protection [3]. The DCCB used for current interruption in a DC network, is an integral part of the system. In this paper, different types of DCCB topologies have been discussed to exploit their limitations, and a new topology with a unique current breaking feature has been presented and evaluated. This paper is structured as shown in: section 2 gives a brief background of the topic along with literature reviews, related works, and problem statement. Section 3 introduces and discusses the new DCCB topology. Section 4 describes the research methodology in detail with a methodology flow chart and later discusses the mathematical modelling and working principle of the proposed topology thoroughly. Section 5 presents the simulation results, compares the performance with that of the conventional topologies and finally validates the proposed concept through experimentation.

2. BACKGROUND STUDY

Circuit breakers are switching devices used to break the current in any electrical network. Circuit breakers either deploy mechanical contacts to make a break in the current path by isolating the contacts or use a solid state turn off mechanism to achieve the current breaking. As the contacts separate in a mechanical turn off process, an arc is initiated in between them, and this arc must be extinguished quickly to break the current efficiently as well as to keep the contacts undamaged. In an alternating current (AC) network, due to the sinusoidal nature of the current, a natural current zero situation arises twice in a full cycle. Using different arc extinguishing techniques, the circuit breaker usually breaks the current at these current zero instances. This process of current breaking is quite straightforward in an AC network, but in a DC network it is not that simple. Natural current zero is not available in the DC current and that makes the breaking of DC current using conventional circuit breakers very challenging [4], [5]. Furthermore, when current flows in a DC network under normal conditions, energy is stored in the inductance of the line as well as in the filter elements of the DC/DC converters. As a result, current in this network cannot be broken instantaneously, otherwise it will create high potential stress on the breaker contacts, create and maintain an arc for a longer period of time, and damage the contacts in the process [6], [7]. Similarly, in the case of a solid state turn off process, a sudden ceasing of current flow in an inductive DC network will develop a high potential stress across the device and may damage it. For safe and efficient breaking of DC current, it must be reduced to zero and the stored energy of the network must be dissipated during the process. Snubber networks or impedance networks or nonlinear resistors or a combination of them are usually used in the conventional DCCB topologies to absorb and dissipate the stored energy as heat and to assist in the current reduction.

2.1. Literature review

As per literature, DC circuit breakers are mainly divided into four categories: (1) Mechanical circuit breakers; (2) Solid-state circuit breakers; (3) Hybrid circuit breakers and (4) Z-source circuit breakers [8]. Some modified versions of these categories are also found in literature. A brief description of the construction and working principles of these topologies is presented in the following sub-sections.

2.1.1. Mechanical circuit breaker

The basic mechanical circuit breaker (MCB) is composed of a mechanical switch, a commutation circuit, and a voltage limiter circuit. The typical schemes of MCB with passive and active commutation circuits are shown in Figure 1 (a). Under normal operating conditions, the mechanical switch (CB) conducts the load current. Once the breaker receives a trip signal, the mechanical switch opens that creates an arc across it. The arc voltage forces the current to shift from the mechanical switch to the commutation circuit. Then the commutation circuit consisting of a capacitor and inductor in series generates a sinusoidal current oscillation at its natural resonant frequency. While the amplitude of the oscillating commutation current (I_c)

becomes sufficiently large, zero-crossing points are created in the mechanical switch current (I_n) and the mechanical switch extinguishes the arc and interrupts the current at the first zero crossing point. A metal oxide varistor (MOV) limits the voltage across the switch. The main advantages of MCBs are low power loss, simple architecture, and relatively low cost. However, slow response time and limited current interruption capability are the main disadvantages [9], [10].

2.1.2. Solid-state circuit breaker

Semiconductor based switches such as thyristor, gate turn-off thyristor (GTO), integrated gate-commutated thyristor (IGCT), and insulated gate bipolar transistor (IGBT), are used as the current interrupting element in solid-state circuit breaker (SSCB) to address the problem of slow time response [11]. A typical SSCB is shown in Figure 1 (b). The operation procedure of SSCB is very simple. Devices like GTO, IGCT and IGBT are fully controllable, and they can be turned on or turned off easily by control signal. But thyristor requires an extra commutation circuit to be turned off, and it takes longer time, and this delay can lead to high fault current. However, the conduction loss in thyristors is the lowest, and such a low on-state loss results in a reduction in the overall size and cost of the SSCB [12]. A MOV connected in parallel to the solid-state switching device limits the voltage surge across it during the current interruption process. Though SSCB has simple construction and provides faster response, higher conduction loss, lack of galvanic isolation, and bulky cooling systems are a few of the limitations [13].

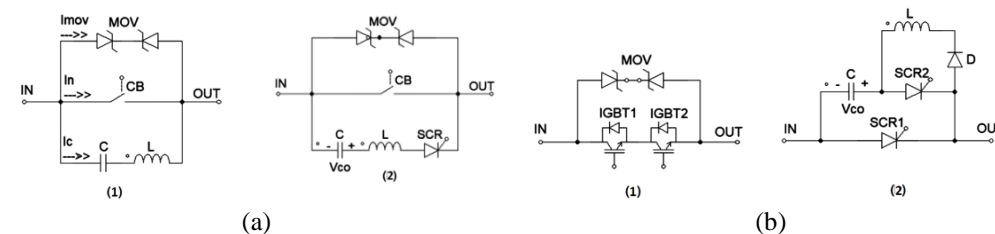


Figure 1. Typical DCCB topology; (a) Mechanical circuit breaker; (b) Solid-state circuit breaker

2.1.3. Hybrid circuit breaker

Hybrid circuit breaker (HCB) is a combined technology that integrates both the MCB and the SSCB. As a result, HCBs possess the advantages of both and offer faster operation, low power loss, and negligible arcing. As shown in Figure 2 (a), a basic HCB scheme has three main parts, including a fast-mechanical switch (FMS), a high-voltage solid state (SS) switch as the main breaker (MB), and a MOV [14]. Under normal operating conditions, the current passes through the FMS. When a trip signal is received, the FMS starts opening and sends a turn-on signal to the MB. Due to the arc voltage developed across the FMS, the current shifts naturally from the FMS to the MB. Once the FMS gains sufficient breakdown strength, the MB is turned off, which creates a voltage spike due to circuit inductances. The MOV turns on to clamp this spike voltage and the current now commutes through MOV and decays to zero. Once the current becomes zero, the residual current breaker (RCB) opens to provide complete galvanic isolation [15]. Despite having many advantages, HCB has few challenges as well. Mismatches in reaction times of the FMS branch and MB branch, mismatches in their current ratings, dependency of the FMS operation on the fault magnitude, and requirement for a higher arc voltage for current commutation, are few of the challenges [16].

2.1.4. Z-source circuit breaker

Z-source circuit breaker (ZSCB) is an upgraded version of the SSCB. A typical ZSCB scheme is shown in Figure 2 (b). While in operation, once a short circuit fault occurs, the fault current is drawn from the capacitors as the current through the inductor can not change instantaneously. At this point, both the capacitor currents increase to reach the prefault inductor current. When the capacitor current equals the inductor current, the SCR current becomes zero, forcing the SCR to turn off. In the next stage, the two series (L - C) branches connected to the fault form resonance and hence current oscillation is created. During this oscillation, the diodes turn on to bypass the current through the resistor, causing the inductor current to circulate in the inductor/resistor/diode loop until it decays to zero [17]. Although ZSCB has some benefits over MCB and SSCB, it only operates reliably in severe fault conditions. Moreover, ZSCB also has drawbacks like undesirable frequency response, not having common ground, and high spike current during turning on [18].

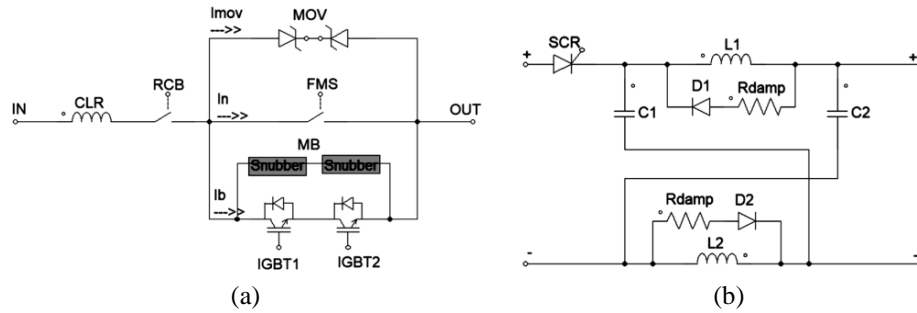


Figure 2. Typical DCCB topology; (a) hybrid circuit breaker; (b) Z-source circuit breaker

2.1.5. Modified topologies

Apart from the conventional topologies, some modified and updated schemes are also proposed in the literature, such as the proactive hybrid circuit breaker [19], Superconductor based hybrid circuit breaker [20], hybrid circuit breaker with commutation booster [21], coupled-inductor solid state circuit breaker [22], ZSCB based on coupled inductors, fast current releasing SSCB topology [23], and gas discharge tube (GDT) based circuit breaker [24]. Table 1 summarizes the advantages and disadvantages of the different topologies.

Table 1. A comparative statement of conventional DC circuit breaker topologies

S.L.	Type	Advantages	Disadvantages	References
Conventional Topology				
1	Mechanical Circuit Breaker	1. Low contact resistance 2. Very low power losses 3. Relatively low cost 4. Provides galvanic isolation	1. Slow operating speed 2. Limited current interruption capability 3. Low lifetime	[9], [10]
2	Solid-State Circuit Breaker	1. Ultra fast operation 2. Very long lifetime	1. High on-state losses 2. Relatively costlier 3. Big size due to heatsink 4. No galvanic isolation	[11]–[13]
3	Conventional Hybrid Circuit Breaker	1. Low power losses 2. Arc free current breaking 3. Reasonable operation speed 4. Provides galvanic isolation	1. Complex technology 2. Current commutation relies on the arc voltage 3. Very expensive	[14]–[16]
4	Z-Source Circuit Breaker	1. Automatic tripping for critical fault 2. Lower cost than SSCBs 3. Reasonable operation speed	1. Requires higher fault for self tripping 2. Cannot provide prolonged protection 3. No common ground 4. No galvanic isolation	[17], [18]
Modified Mechanical Circuit Breaker Topology				
1.1	Gas Discharge Tube (GDT) based Circuit Breaker	1. Fast operation 2. Reasonable efficiency	1. Lifetime not proven yet 2. Continuous power requirement 3. Expensive	[24]
Modified Solid State Topology				
2.1	SSCB Topology with Self-Adapting Fault Current Limiter	1. Automatic tripping for set fault level 2. Bidirectional power flow capability 3. Automatic fault current limiting capability	1. High on-state losses 2. Complex architecture 3. Bigger size 4. Reliability not proven yet	[11]
2.2	Fast Current Releasing SSCB Topology	1. Faster operation 2. Soft turning off operation 3. Free from surge voltage 4. Very long lifetime	1. High on-state losses 2. No bidirectional power flow capability 3. Source inductance degrades current interruption capability	[23]
2.3	Coupled-Inductor Solid State Circuit Breaker	1. Automatic tripping for critical fault 2. Fault current is not reflected to the source	1. No bidirectional power flow capability 2. Requires higher fault for self tripping	[22]
2.4	Self-Powered SSCB Topology	1. Automatic tripping for critical fault 2. Bidirectional power flow capability 3. Self powered hence, no external power supply is required	1. High on-state losses 2. Complex architecture 3. Requires higher fault for self tripping	[25], [26]

Table 1. A comparative statement of conventional DC circuit breaker topologies (*continue*)

Modified Hybrid Topology				
3.1	Proactive Hybrid Circuit Breaker	1. Faster operation 2. Reasonable efficiency	1. Increased on-state losses 2. Very expensive	[19]
3.2	Hybrid Circuit Breaker with Commutation Booster	1. Faster operation with high rate of rise of the fault current	1. Losses in the coupled inductor 2. Very expensive	[21]
3.3	DC Circuit Breaker with Superconductor based Current Limiter	1. Low losses 2. Inherent fault current limiting	1. Self-oscillation circuit needed for the mechanical switch 2. Cryogenic system required 3. Very expensive	[20]
3.4	Superconductor based Hybrid Circuit Breaker	1. Low losses 2. Fast operation	1. Cryogenic system required 2. Very expensive	[20]
Modified Z-source Topology				
4.1	Bi-directional ZSCB based on Cross Connection	1. Fault current is not reflected to the source 2. Bidirectional power flow capability 3. Moderate conduction losses	1. No common ground 2. Complex architecture 3. Bigger size 4. Relatively costly	[18]
4.2	Bi-directional ZSCB based on Series Connection	1. Provides common ground 2. Bidirectional power flow capability 3. Moderate conduction losses	1. Fault current is reflected to the source 2. Complex architecture 3. Bigger size 4. Relatively costly	[24]
4.3	Bi-directional ZSCB based on Coupled Inductors	1. Provides common ground 2. Bidirectional power flow capability 3. Fault current is not reflected to the source 4. Moderate conduction losses	1. Complex architecture 2. Bigger size 3. Relatively costly	[24]

2.2. Problem statement

Each of the DCCB topologies has its own advantages and limitations. But all the topologies have a common drawback in terms of the current breaking technique. Almost all the topologies use either snubber networks or impedance networks, or nonlinear resistors or a combination of them as absorber circuits to dissipate the stored energy of the network as heat during each current breaking operation. This conventional current breaking technique makes the DCCB an inefficient device in the network. Because a significant amount of energy is wasted during every current breaking operation in a high current network. But instead of dissipating, the stored energy can be reused in a similar way like the regenerative braking in an electrical drive system works. As we are striving for more energy efficient technology for every day application for a sustainable future, if there is a slightest scope of energy conservation, it should be grasped whole heartedly. However, from the knowledge of the literature, there is hardly any study that deals with the energy reuse capability of a DCCB. A thorough review of the literature, as well as scholarly and patent-related information from [27], demonstrates that the concept of regenerative current breaking in circuit breakers is novel. Though studies such as [25], [26] have presented topologies which utilize network energy to operate themselves and do not require any external power, those are not dealing with the greater domain of energy regeneration. Hence, this paper will explore the scopes and techniques of current breaking with regeneration in DCCB, will propose a new topology with energy regeneration capability, will build the mathematical modelling and validate the proposed concept through simulation and experimentation.

3. PROPOSED WORK

Regenerative braking is a well-known technique used in electrical drive systems. The rotor of a running motor stores mechanical energy in the form of rotational kinetic energy. When this running motor needs faster deceleration, the drive system manipulates the motor supply voltage in such a way that the motor enters into generating mode. The drive system now absorbs electrical energy from it and feeds this electrical energy back into the source. As the mechanical energy of the rotor is absorbed, a negative torque is generated which decelerates the motor faster. In addition, the energy absorbed by the drive system is reused to recharge the battery if battery was used as a source or simply used to supply other loads connected to the source. This technique increases the overall efficiency of the system on a greater scale. Similarly, energy is stored in the network inductances of a DC network in terms of current, and while breaking this current, the stored energy can be absorbed and fed back to the source afterwards. Figure 3 (a) presents the proposed DCCB topology, which consists of mechanical switches, thyristors, diodes, IGBT, capacitor, and inductor. As per the proposed regenerative current breaking concept, upon receiving a trip signal, the load current is diverted from the main branch to the impedance network (L - C network) inside the circuit breaker to reduce the current to zero

initially; and to store the energy within the capacitor in terms of voltage. Once the current becomes zero, the load is disconnected from the source side and, subsequently, the stored energy of the capacitor is fed back towards the source, commencing regeneration as shown in Figure 3 (b). The detailed working principles and mathematical modelling are presented in section 3.

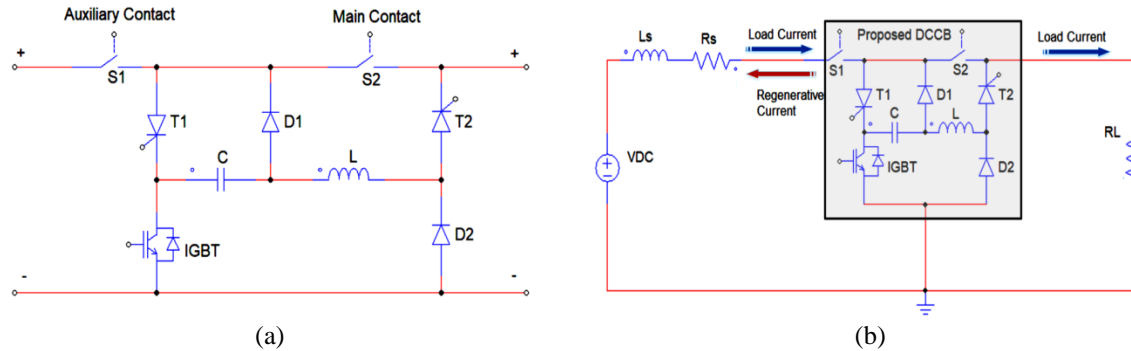


Figure 3. Proposed DCCB topology and its application; (a) proposed DCCB topology, (b) proposed topology used in a radial DC network

4. RESEARCH METHOD

This section describes the research methodology, presents the methodology flow chart, and finally discusses the mathematical modelling and working principle of the proposed topology thoroughly.

4.1. Methodology

A detail graphical representation of the research methodology is stated in Figure 4 that shows the different phases of the research. The research work was conducted through simulation, analysis, and experimentation and was carried out in four phases given by:

- Phase-1: Literature Review and Simulation of the Existing DCCB Models: The first step of this research was to extensively go through the literature on different DCCB topologies, to understand their working principles and to realize their limitations. Special focus was given to their current breaking mechanisms to exploit the drawbacks and to generate new ideas for feasible solution.
- Phase-2: Modeling of the Proposed Regenerative Current Breaking Technique: The mathematical model of both the current breaking and regeneration operations was developed in this phase. Later, a new topology was devised to be best fitted with the mathematical model, followed by developing a control algorithm for generating coordinated switching signals for the topology.
- Phase-3: Simulation and Analysis: In the third phase, the proposed DCCB was simulated in PSIM software. A radial DC network with source resistance and inductance was used for simulation where the proposed model was applied to break the network current and to regenerate current afterwards. In addition to that, properties such as current breaking time, voltage stress, and voltage disturbance in the network. were thoroughly investigated and evaluated.
- Phase-4: Experimental Validation: In the final phase, a prototype model of the proposed DCCB topology was built for experimental validation. The current breaking capability, along with the regeneration effect, was demonstrated and the performance was evaluated accordingly.

4.2. Modeling

Mathematical modelling of the proposed topology is explained in this subsection. Necessary differential equations based on simple circuit analysis are developed and then solved to find the time domain responses which justify the working principle.

4.2.1. Mathematical model for current breaking

The proposed regenerative current breaking technique is formulated based on the concept that an inductor and a capacitor form a resonant circuit that creates current oscillation when connected to a voltage source, and they store energy cyclically in terms of current (I) and voltage (V) respectively. Energy stored in an inductor and a capacitor is calculated as $\frac{1}{2}LI^2$ and $\frac{1}{2}CV^2$ respectively, where L stands for inductance and C

for capacitance. As shown in Figure 5 (a), when current $i(t) = I_o$ flows in the DC network, energy is stored in the source inductance L_s . At time $t = t_o$, the breaker receives a trip signal which initiates the tripping process.

At the initiation of tripping, the fast-operating mechanical switch (S2) opens, and an arc voltage is created. At the same time, gate pulses are sent to the thyristors (T1 & T2). Due to this combined effect, the load current is commutated from the main branch to the secondary branch (impedance network) as shown in Figure 5 (b). This impedance network consisting of L and C generates a current oscillation at its natural resonant frequency. This current oscillation diverts the main branch current completely, and thus the arc voltage cannot go very high, and the arc is extinguished shortly. The current oscillation is governed by (1). It is to be noted that the source current and the load current are synonymous here.

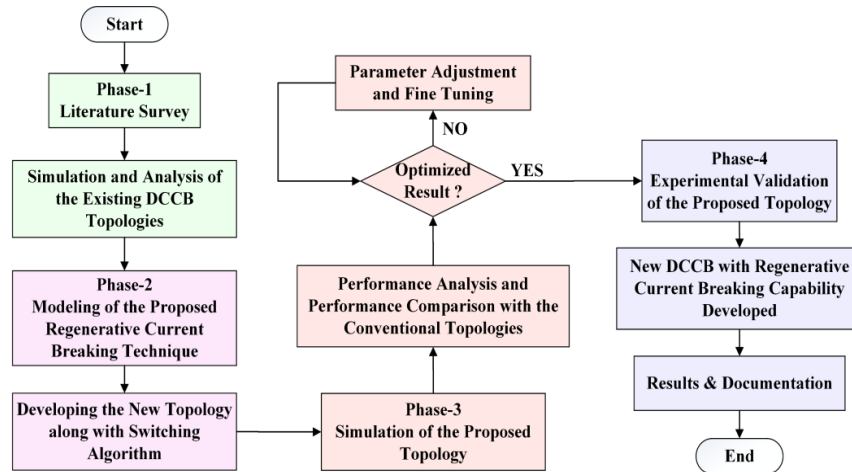


Figure 4. Methodology flow chart

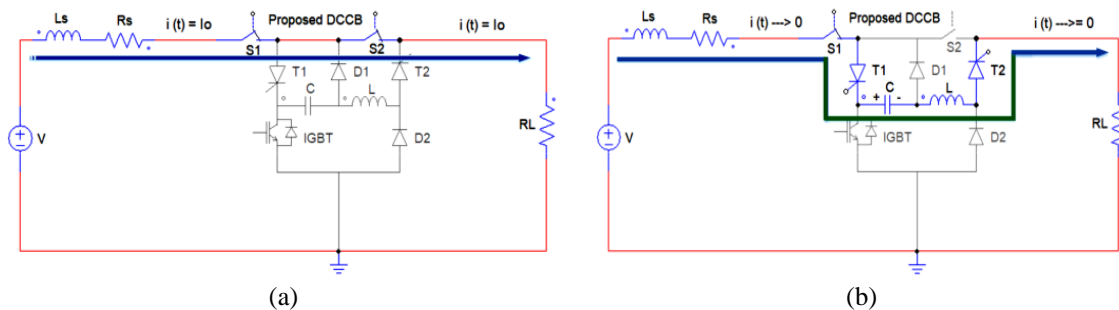


Figure 5. Current breaking operation in the proposed circuit breaker; (a) source current path before tripping initiated, (b) source current path after tripping initiated

$$(L_s + L) \frac{di(t)}{dt} + (R_s + R_L) i(t) + \frac{1}{C} \int i(t) dt = V, i(t = t_0) = I_0 \quad (1)$$

where, V = DC source voltage, R_s = source resistance, L_s = source inductance, R_L = load resistance, $i(t)$ = source current, I_o = initial value of source current, L = breaker inductance, C = breaker capacitance. The solution of (1) is given by (2) where, $\alpha = \frac{(R_s + R_L)}{2(L_s + L)}$ is the damping factor, $\omega_r = \frac{1}{\sqrt{(L_s + L)C}}$ is the resonant frequency, $\beta = \sqrt{\omega_r^2 - \alpha^2}$, $A = I_0$ and $B = \frac{-V + I_0(R_s + R_L)}{\alpha\beta(L_s + L)}$.

$$i(t) = e^{-\alpha t} (A \cos \beta t + B \sin \beta t) \quad (2)$$

As shown in (2) is a damped oscillation which ultimately decays to zero as shown in Figure 6 (a). But, during the first zero-crossing point of this oscillating current, the thyristors (T1 & T2) are turned off by natural commutation and the capacitor C remains charged as shown in Figure 6 (b). As the thyristors are now

turned off, the load becomes totally disconnected from the source, completing a successful current breaking operation. The current breaking time is calculated as $T_{trip} = t_1 - t_0$.

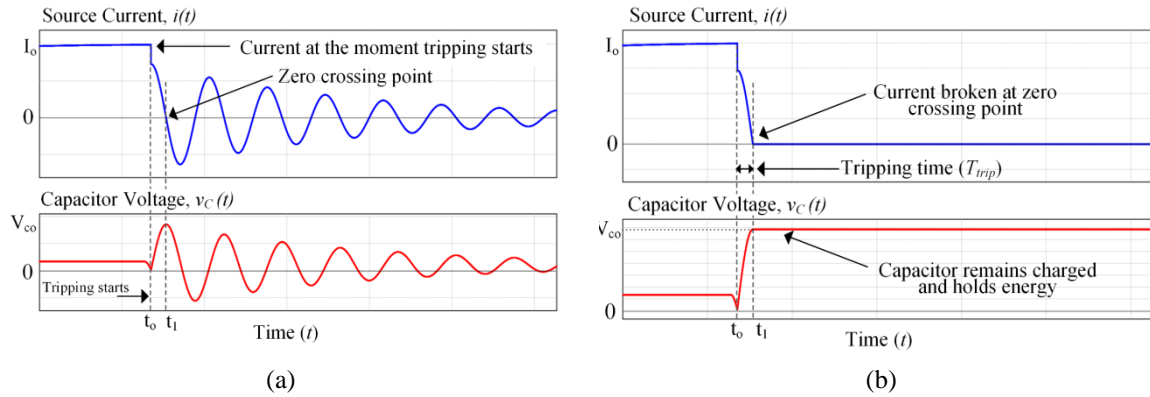


Figure 6. Dynamic responses during current breaking operation; (a) current and voltage oscillation as per (2), (b) current breaking and capacitor charging

4.2.2. Mathematical model for regeneration

Once the thyristors are turned off, the regeneration cycle starts by turning on the IGBT at time $t = t_2$. As a result, the capacitor C discharges through the inductor L , and thus the stored energy of the capacitor is transferred to the inductor as shown in Figure 7 (a). The current response is governed by (3) whose solution is (4) where V_{co} =initial voltage of the charged capacitor, $i_r(t)$ = regenerated current, and $\omega_r' = \frac{1}{\sqrt{LC}}$ is the resonant frequency. Hence, the inductor current is now forced to flow through diodes (D1 & D2) towards the source as shown in Figure 7(b).

$$L \frac{di_r(t)}{dt} + \frac{1}{C} \int i_r(t) dt = 0, i_r(t = t_2) = 0, V_C(t = t_2) = V_{co} \quad (3)$$

$$i_r(t) = V_{co} \sqrt{\frac{C}{L}} (\sin \omega_r' t) \quad (4)$$

As shown in (4) is a simple sinusoidal response which cyclically transfers energy back and forth between L and C , as can be seen in Figure 8 (a). But as soon as the capacitor discharges completely in this oscillation, the control system turns off the IGBT at time $t=t_3$.

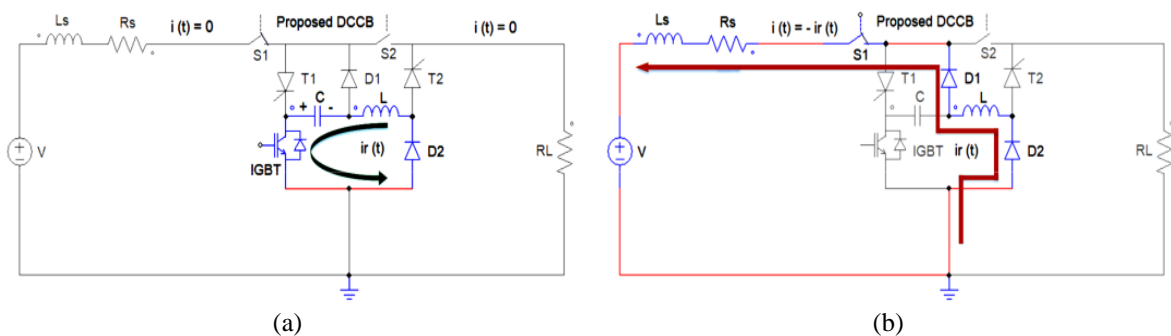


Figure 7. Regeneration operation in the proposed circuit breaker; (a) capacitor transfers energy to the inductor, (b) Inductor releases energy towards the source

This phenomenon of feeding energy back to the source side network is defined as regeneration. The equation for the regenerated current and its time domain response are given by (5) and (6) respectively and the responses are visualized in Figure 8 (b).

$$(L_s + L) \frac{di(t)}{dt} + R_s i(t) = V, i(t = t_3) = -I_{r0} \quad (5)$$

$$i(t) = -I_{r0} e^{-\frac{R_s}{L_s+L}t} + \frac{V}{R_s} (1 - e^{-\frac{R_s}{L_s+L}t}) \quad (6)$$

where, I_{r0} = inductor current at the moment the IGBT turns off. The regenerated current $i(t) = -i_r(t)$ has a peak value of $-I_{r0}$ that exponentially reduces to zero while being fed back. Once the regenerated current becomes zero, the auxiliary switch (S1) turns off and the breaker resets for the next operation.

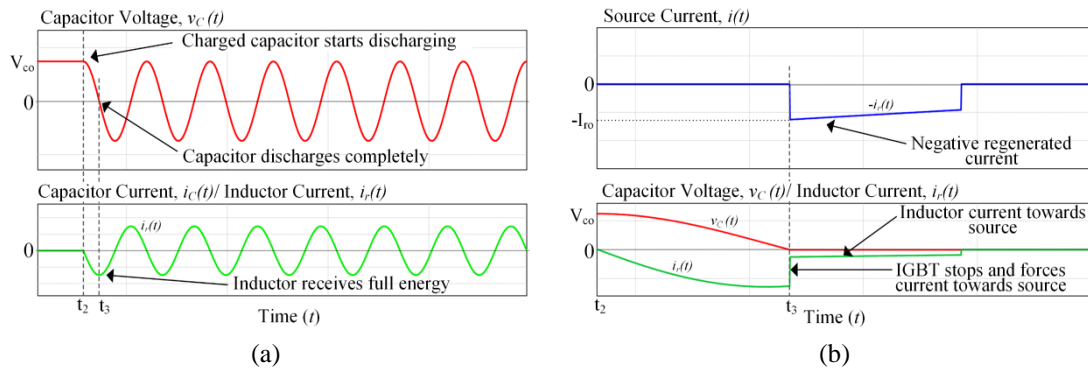


Figure 8. Dynamic responses during regeneration; (a) current and voltage oscillation as per (4), (b) regenerated current as per (6)

5. RESULTS AND DISCUSSION

This section discusses the results of the simulation and experimental studies and thus validates the proposed concept. For simplicity, the network shown in Figure 3 (b) was modelled and simulated in PSIM software. Later, a scaled down prototype of the DCCB model was built and tested. Both the current breaking and regenerative function of the proposed topology were demonstrated and validated.

5.1. Simulation

The PSIM simulation model as shown in Figure 9 was simulated using the following simulation parameters: $V_{DC}=400$ V, $L_s=200$ mH, $R_s=0.1$ Ω , $R_L=0.9$ Ω , $L=50$ mH, and $C=2000$ μ F. The network parameters were chosen in such a way that it became a high-current network with moderate network inductance. The circuit breaker parameters were then chosen based on the design calculations in line with the mathematical modeling.

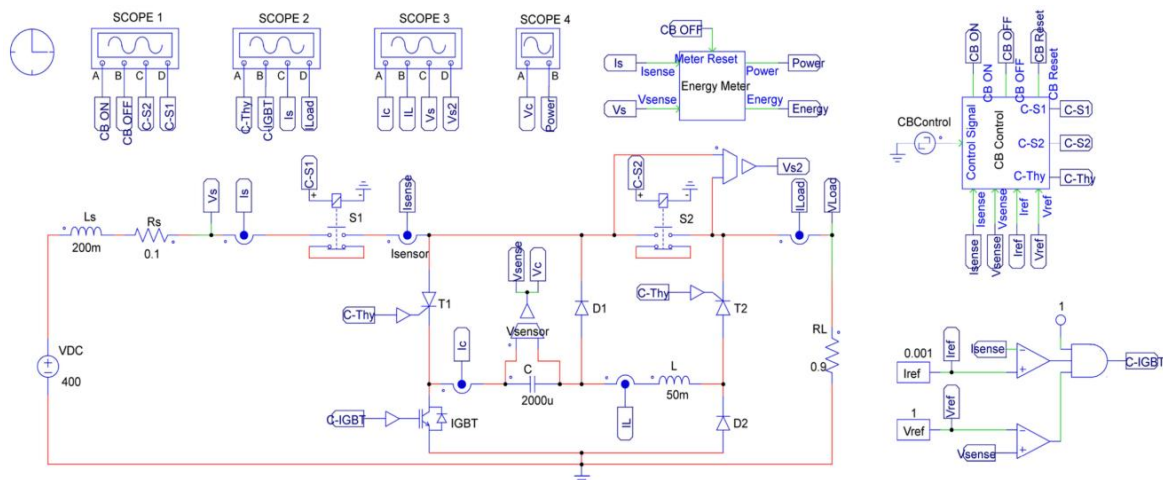


Figure 9. PSIM simulation model

5.1.1. Current breaking

A simple control algorithm generates the coordinated switching signals for the switching devices. The current commutation, reduction, and regeneration along with coordinated switching signals are shown in Figure 10 (a) which shows that the DCCB turns on at time $t = 0.055$ s upon receiving a closing pulse and the source current I_s rises and reaches to 400 A. At time $t = 1.5$ s, a trip signal is received by the circuit breaker and the tripping process starts. At the initiation of tripping, the control voltage for main contact S2 goes low that turns it off after a switching delay of 15 ms. The gate pulse V_{gT} turns the thyristors on, and the arc voltage induced due to the separation of S2 contacts forces I_s to shift to the impedance network and the current becomes I_o/I_L as shown in Figure 10 (a). Resonance is formed in this impedance network, which creates the current zero point, and the thyristors turn off at this zero-crossing point, forcing I_s and I_{LOAD} to become zero, ensuring 51.75 ms of current breaking time. As the current passes through the impedance network, it charges the capacitor C , and the capacitor voltage V_C rises and remains charged until it discharges during regeneration as shown in Figure 10 (b). In addition, a voltage surge induced due to high di/dt during the current breaking period is also visible in the source voltage V_s and switch voltage V_{S2} . Moreover, a surge in source power P_s due to sudden energy release from the source inductance is also visible in Figure 10 (b). This is the energy which is usually wasted in the conventional DCCB topologies. The regeneration operation is explained in the next subsection.

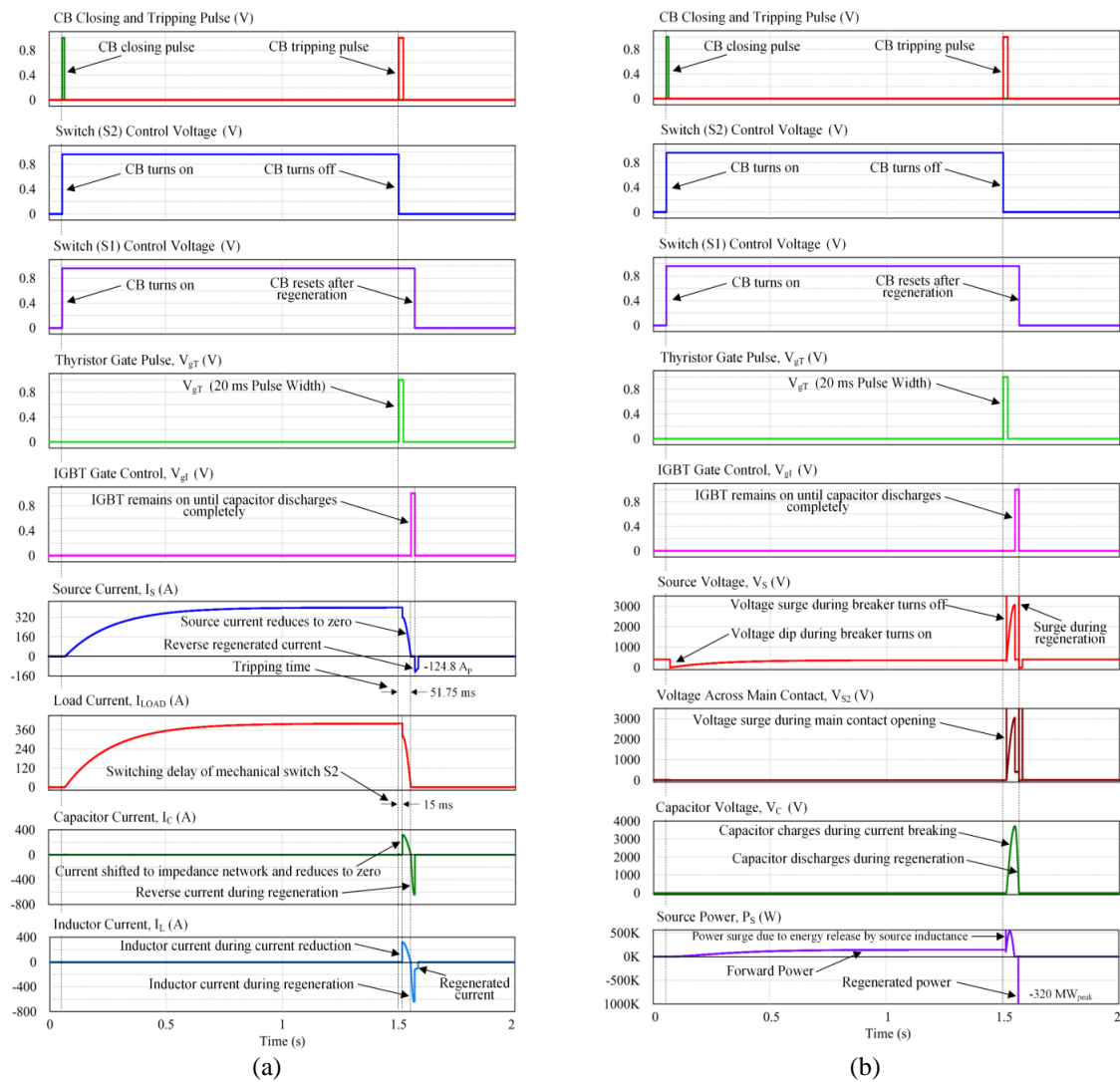


Figure 10. Control signals and synchronized current and voltage responses during circuit breaker operation; (a) control signals and current responses, (b) control signals and voltage and power responses

5.1.2. Regeneration

When the source current becomes zero, the DCCB gets ready for the regeneration sequence. The gate control voltage V_{gt} turns the IGBT on at a time, $t = 1.57$ s, and the charged capacitor starts discharging to the inductor. The negative discharging current I_c and I_L are visible in Figure 10 (a). As the capacitor discharges, energy is transferred from the capacitor to the inductor. The moment the capacitor discharges completely, and V_c becomes zero, the IGBT turns off, forcing I_L to conduct through diode D1 towards the source. As a result, the inductor now releases the energy back into the source side network and regeneration takes place. The inductor current which becomes the regenerated current is depicted as the negative source current in Figure 10 (b) with a peak value of -124.8 A. The average value of the regenerated current is measured as -109.85 A. The regenerated power as shown in Figure 10 (b) is measured as around -320 MW_p, which is very high due to the high energy density caused by the very small regeneration period, e.g., 0.15 ms only. The amount of regenerated energy is measured as 11.99 kJ, which is around 40.3% of the total energy released from the source network during the current breaking operation.

5.2. Performance evaluation

The transient responses during current breaking operation in a conventional topology, such as MCB, and in the proposed topology are shown in Figure 11 where the distinctions are clearly visible. Though the main novelty of the proposed topology is its regeneration capability, its tripping speed is also faster than the conventional MCB, as can be seen in the figure. MCB dissipates energy in the absorber circuit as shown in Figure 11 (a) while the proposed topology regenerates it as can be seen in Figure 11 (b). Other conventional topologies such as SSCB, HCB, ZSCB, and their modified versions also dissipate energy either through an absorber circuit or through an MOV or snubber network. A comparative statement of the current breaking performances of some conventional DCCB and the proposed DCCB is presented in Table 2. Lower conduction loss and provision of galvanic isolation are two of the important criteria of a DCCB for high voltage, high current applications where both the SSCB and ZSCB suffer greatly. ZSCB operation even becomes unreliable in a highly inductive network. In a nutshell, in terms of overall performance, the proposed topology genuinely outshines others.

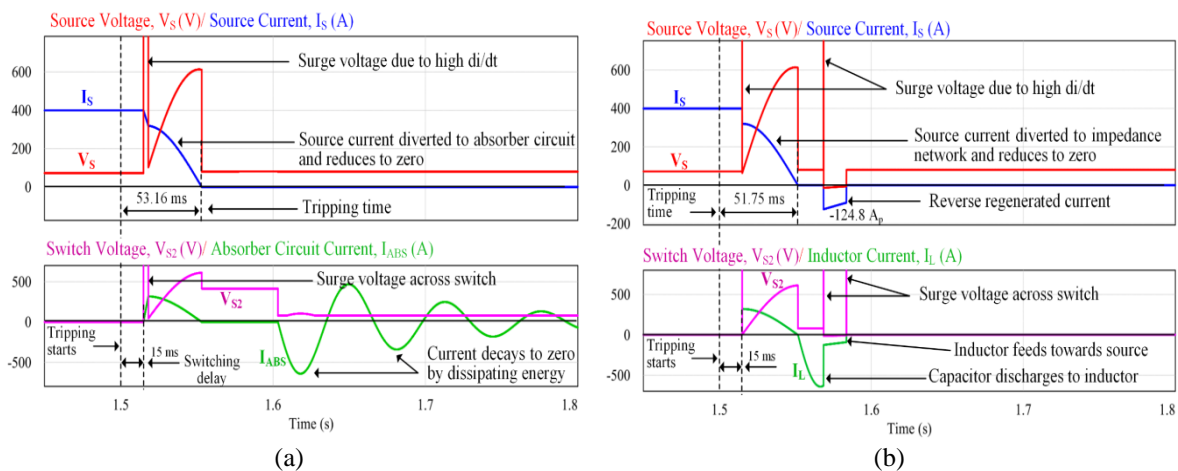


Figure 11. Transient responses during current breaking in conventional and proposed topology (All the voltages have been scaled down to 1/5th of the actual value); (a) current breaking in a conventional topology, (b) current breaking in the proposed topology

Table 2. Performance comparison

S.L.	Criteria	Topology				Proposed
		MCB	SSCB	HCB	ZSCB	
1	Current Breaking Time (T_{trip})	53.16 ms	17.33 ms	32.56 ms	*	51.75 ms
2	Regenerated Current (I_R)	0	0	0	0	-109.85 A (Average)
3	Regenerated Energy (E_R)	0	0	0	0	11.99 kJ
4	Energy Recovery Efficiency (η)	0	0	0	0	40.3%
5	Provision of Galvanic Isolation	Yes	No	Yes	No	Yes

*Fails to trip in highly inductive network. Requires higher values for CB parameter

5.3. Experimentation

A prototype of the proposed topology was built using Lab volt modules. An Arduino UNO microcontroller board was used for generating the control signals. A similar DC network as shown in Figure 3 (b) but with scaled down parameters, was built for the experimental set up with the following experimental parameters: $V_{DC} = 48$ V, $L_S = 2.6$ H, $R_S = 20.7$ Ω , $R_L = 27.3$ Ω , $L = 325$ mH, and $C = 50$ μ F. The experimental set up is shown in Figure 12. The coordinated switching signals and the synchronized voltage and current responses are shown in Figure 13. The current breaking time is measured as 35.58 ms as per Figure 13 (a). It is also found from the experimental results that the peak value of the regenerated current is -0.3 A with an average value of -0.16 A while the amount of regenerated energy is measured as -0.93 J. The peak value of the regenerated power is measured as -160.4 W as shown in Figure 13 (b), and yet again, this is due to the high energy density. The experimental results are found to be fully consistent with the simulation results.

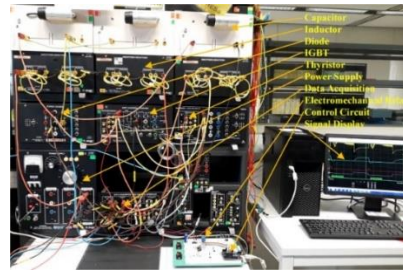


Figure 12. Experimental set up

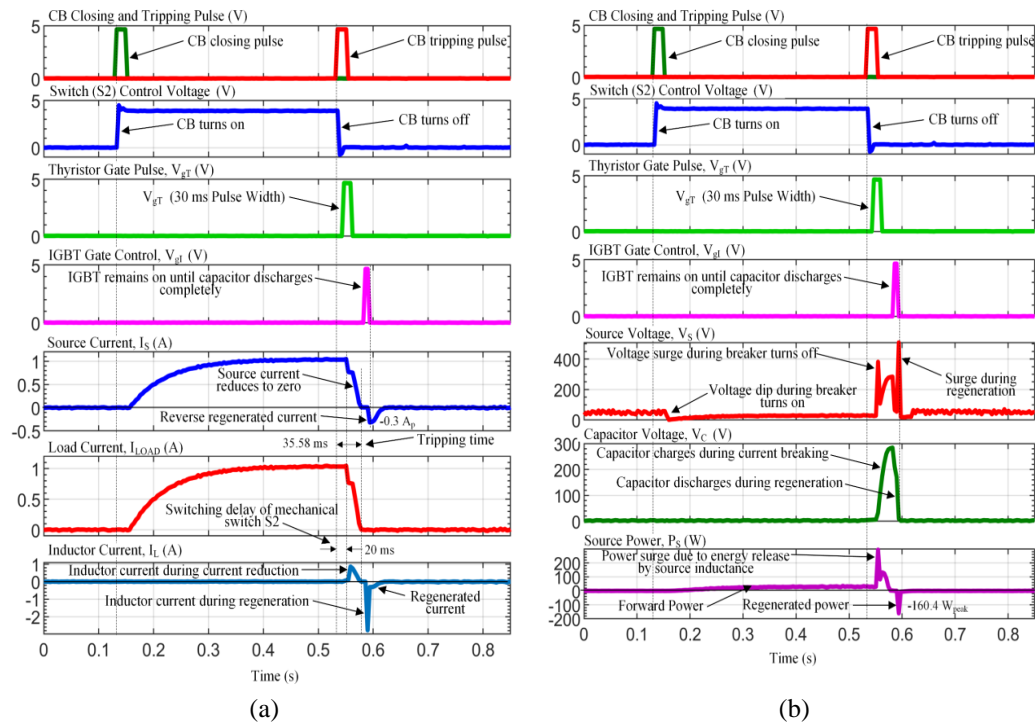


Figure 13. Control signals and synchronized current voltage responses during circuit breaker operation; (a) control signals and current responses, (b) control signals and voltage and power responses

6. CONCLUSION

This paper discusses the DC circuit breaker technology and exploits the weakness of the conventional DCCB topologies. One of the common limitations of the existing topologies was found to be their inefficient current breaking technique. So, a new and efficient current breaking technique along with a new topology was proposed and validated through simulation and experimentation. The amount of energy

that can be regenerated totally depends on the current that needs to be broken and the system inductances. Hence, the highly inductive DC network is going to be a very suitable application area for the proposed topology as it will ensure efficient current breaking and will conserve energy. However, it was found that the short time duration of the regenerated current had created a high-power surge due to high energy density. It might be possible to minimize the power surge by regulating the regenerated current. A high voltage surge was also generated at the start of the breaker turn off process and regeneration process, and this surge voltage also needs to be limited to keep it within acceptable equipment ratings. In addition, the energy recovery efficiency of the proposed model was found to be 40.3%, which is still very low. So, future scopes are there to extend this study further to resolve issues such as regulating the regenerated current to make it smoother, keeping the system voltage within an acceptable limit, and increasing the energy recovery efficiency.

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REFERENCES

- [1] S. Beheshtaein, R. Cuzner, M. Savaghebi, and J. M. Guerrero, "Review on microgrids protection," *IET Generation Transmission & Distribution*, vol. 13, no. 6, pp. 743-759, 2019, doi: 10.1049/iet-gtd.2018.5212.
- [2] S. Beheshtaein, R. M. Cuzner, M. Forouzesh, M. Savaghebi, and J. M. Guerrero, "DC Microgrid Protection: A Comprehensive Review," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, doi: 10.1109/JESTPE.2019.2904588.
- [3] D. Kumar, F. Zare, and A. Ghosh, "DC Microgrid Technology: System Architectures, AC Grid Interfaces, Grounding Schemes, Power Quality, Communication Networks, Applications, and Standardizations Aspects," in *IEEE Access*, vol. 5, pp. 12230-12256, 2017, doi: 10.1109/ACCESS.2017.2705914.
- [4] W. Kim, Y. J. Kim, and H. Kim, "Arc voltage and current characteristics in low-voltage direct current," *Energies*, vol. 11, no. 10, pp. 1-14, 2018, doi: 10.3390/en11092511.
- [5] G. P. Adam, T. K. Vrana, R. Li, P. Li, G. Burt, and S. Finney, "Review of technologies for DC grids – power conversion, flow control and protection," *IET Power Electronics*, vol. 12, no. 8, pp. 1851-1867, 2019.
- [6] J. Ma, M. Zhu, X. Cai, and Y. W. Li, "DC Substation for DC Grid—Part I: Comparative Evaluation of DC Substation Configurations," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9719-9731, Oct. 2019, doi: 10.1109/TPEL.2019.2895043.
- [7] N. B. Jemaa, "Short arc duration laws and distributions at low current (<1 A) and voltage (14-42 VDC)," in *IEEE Transactions on Components and Packaging Technologies*, vol. 24, no. 3, pp. 358-362, Sept. 2001, doi: 10.1109/6144.946480.
- [8] Y. Wang, Z. Yuan, W. Wen, Y. Ji, J. Fu, Y. Li, and Y. Zhao, "Generalised protection strategy for HB-MMCMTDC systems with RL-FCL under DC faults," *IET Generation Transmission & Distribution*, vol. 12, no. 5, pp. 1231-1239, 2018, doi: 10.1049/iet-gtd.2016.1943.
- [9] B. Ni, W. Xiang, Z. Yuan, X. Chen, and J. Wen, "Operation and transient performance of a four-terminal MMC based DC grid implementing high power mechanical DC circuit breaker," *The Journal of Engineering*, vol. 2019, no. 18, pp. 5167-5171, 2019, doi: 10.1049/joe.2018.9257.
- [10] D. Jovicic, "Series LC DC circuit breaker," *High Volt. High Voltage*, vol. 4, no. 2, pp. 130-137, 2019, doi: 10.1049/hve.2019.0003.
- [11] B. Li, J. He, Y. Li and R. Li, "A Novel Solid-State Circuit Breaker With Self-Adapt Fault Current Limiting Capability for LVDC Distribution Network," in *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3516-3529, April 2019, doi: 10.1109/TPEL.2018.2850441.
- [12] Y. Guo, G. Wang, D. Zeng, H. Li and H. Chao, "A Thyristor Full-Bridge-Based DC Circuit Breaker," in *IEEE Transactions on Power Electronics*, vol. 35, no. 1, pp. 1111-1123, Jan. 2020, doi: 10.1109/TPEL.2019.2915808.
- [13] J. Xu, X. Zhao, N. Han, J. Liang and C. Zhao, "A Thyristor-Based DC Fault Current Limiter With Inductor Inserting-Bypassing Capability," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 3, pp. 1748-1757, Sept. 2019, doi: 10.1109/JESTPE.2019.2914404.
- [14] A. Shukla and G. D. Demetriades, "A Survey on Hybrid Circuit-Breaker Topologies," in *IEEE Transactions on Power Delivery*, vol. 30, no. 2, pp. 627-641, April 2015, doi: 10.1109/TPWRD.2014.2331696.
- [15] C. C. Peng, I. Husain, A. Q. Huang, B. Lequesne and R. Briggs, "A Fast Mechanical Switch for Medium-Voltage Hybrid DC and AC Circuit Breakers," in *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 2911-2918, July-Aug. 2016, doi: 10.1109/TIA.2016.2539122.
- [16] L. Liu, J. Zhuang, C. Wang, Z. Jiang, J. Wu and B. Chen, "A Hybrid DC Vacuum Circuit Breaker for Medium Voltage: Principle and First Measurements," in *IEEE Transactions on Power Delivery*, vol. 30, no. 5, pp. 2096-2101, Oct. 2015, doi: 10.1109/TPWRD.2014.2384023.
- [17] G. Li, J. Liang, S. Balasubramaniam, T. Joseph, C. E. Ugalde-Loo and K. F. Jose, "Frontiers of DC circuit breakers in HVDC and MVDC systems," *2017 IEEE Conference on Energy Internet and Energy System Integration (EI2)*, 2017, pp. 1-6, doi: 10.1109/EI2.2017.8245743.

- [18] S. G. Savaliya and B. G. Fernandes, "Analysis and Experimental Validation of Bidirectional Z-Source DC Circuit Breakers," in *IEEE Transactions on Industrial Electronics*, vol. 67, no. 6, pp. 4613-4622, June 2020, doi: 10.1109/TIE.2019.2928284.
- [19] C. Peng, X. Song, A. Q. Huang and I. Husain, "A Medium-Voltage Hybrid DC Circuit Breaker—Part II: Ultrafast Mechanical Switch," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 5, no. 1, pp. 289-296, March 2017, doi: 10.1109/JESTPE.2016.2609391.
- [20] X. Pei, O. Cwikowski, A. C. Smith and M. Barnes, "Design and Experimental Tests of a Superconducting Hybrid DC Circuit Breaker," in *IEEE Transactions on Applied Superconductivity*, vol. 28, no. 3, pp. 1-5, April 2018, Art no. 5000205, doi: 10.1109/TASC.2018.2793226.
- [21] C. M. Franck, "HVDC Circuit Breakers: A Review Identifying Future Research Needs," in *IEEE Transactions on Power Delivery*, vol. 26, no. 2, pp. 998-1007, April 2011, doi: 10.1109/TPWRD.2010.2095889.
- [22] K. A. Corzine, "A New-Coupled-Inductor Circuit Breaker for DC Applications," in *IEEE Transactions on Power Electronics*, vol. 32, no. 2, pp. 1411-1418, Feb. 2017, doi: 10.1109/TPEL.2016.2540930.
- [23] A. Mokhberdoran, A. Carvalho, N. Silva, H. Leite, and A. Carrapatoso, "Design and implementation of fast current releasing DC circuit breaker," *Electric Power Systems Research*, vol. 151, pp. 218-232, 2017.
- [24] S. M. Sanzad Lumen, R. Kannan and N. Z. Yahaya, "DC Circuit Breaker: A Comprehensive Review of Solid State Topologies," 2020 *IEEE International Conference on Power and Energy (PECon)*, 2020, pp. 1-6, doi: 10.1109/PECon48942.2020.9314300.
- [25] Z. Miao, G. Sabui, A. Moradkhani Roshandeh and Z. J. Shen, "Design and Analysis of DC Solid-State Circuit Breakers Using SiC JFETs," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 863-873, Sept. 2016, doi: 10.1109/JESTPE.2016.2558448.
- [26] F. Xu, Y. Lu, X. Xuan, H. Yu, P. Qiu, and D. Jiang, "Self-energy device for HVDC breakers and its control strategy," *The Journal of Engineering*, vol. 2019, no. 16, pp. 2397-2400, 2019, doi: 10.1049/joe.2018.8700.
- [27] Patent and scholarly data source: <https://www.lens.org>. [accessed 2021]

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