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Simulation study of pulse width modulation schemes for three-phase impedance source inverter

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ABSTRACT

To avoid a short circuit of the input direct current (DC). source, a 3-phase inverter cannot run two switches in the same leg at a time, and it always operates in buck mode, with the output voltage being less than the input voltage. The Impedance source inverter features a feature that allows both switches in one leg to operate at the same time, and it can operate in buck/boost mode, which means the output voltage can be greater than the input voltage depending on the shoot-through time. In the literature, there are a few pulse width modulation (PWM) techniques for Impedance source inverter control. This research includes a simulation study as well as an examination of existing PWM schemes in the literature, as well as a proposal for TESVPWM for inverters. The inverter performance has evaluated using total harmonic distortion and fundamental components, validating by simulation findings.

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1. INTRODUCTION

The dynamic evolution of power and microelectronics devices demonstrates consistent advancement in the design and implementation of modern variable speed drives. There has been much study on the inverter side to regulate the required output while minimizing switching losses, thanks to developments in power electronic semiconductor devices. Voltage-source inverters (VSI) and current-source inverters (CSI) are discussed in the literature. A direct current (DC) source is connected to an alternating current (AC). load at the output of 3-phase VSI and CSI inverters by six semiconductor devices that comprise three legs, each containing two semiconductor devices. These inverters are used to convert DC to AC, although they have significant drawbacks, such as: i) applications like as fuel cells and solar arrays necessitate the use of a boost converter to enhance the dc-link voltage to achieve the appropriate output voltage. This raises the complexity and cost of the circuit while lowering its reliability; and ii) to avoid a short circuit in the input dc-link, the switches on the same leg must never activate at the same time. The dead time between switching must be provided to ensure VSI protection, but this creates harmonics and distortion in the output voltage.

The use of a customized impedance network between the inverter circuit and the power source can overcome this problem with impedance source inverters. The impedance network is a two-port system with two split inductors (L1 & L2) and two x-shaped capacitors (C1 & C2). A voltage-source and impedance network is followed by 3 phase inverter and loaded in a 3-phase impedance source inverter (Impedance source inverter). The DC power source is connected to the 3-phase inverter via an impedance circuit, which is nothing more than a second-order filter.

This paper presents a simulation analysis of three pulse width modulation (PWM) schemes for 3-phase impedance source inverters: carrier-based pulse width modulation (CBPWM), third harmonic pulse width modulation (THPWM), and Offset-addition based PWM, which have been applied to the Impedance source inverter and the output has been evaluated using total harmonic distortion and fundamental component. Then, for Impedance source inverters, a time equivalent PWM method is proposed, and the output is evaluated again using the same parameters. The final section is a comparison of the PWM system. The simulation data has been provided for Matlab/Simulink analysis.

2. IMPEDANCE-SOURCE INVERTER

The z-source inverter is a power conversion scheme that bucks and boosts the input voltage using passive components. The shoot-through (ST) state of the z-source inverter can be exploited to boost and buck the input voltage, considerably enhancing the inverter's dependability and giving an appealing single-stage DC to AC conversion. Power circuit diagram for impedance source inverter is given in Figure 1. The duty cycle of shoot-through is used to track the voltage boost on the dc connection and, as a result, the inverter's output voltage boost [1].

The impedance source inverter overcomes the restrictions of traditional inverters and can convert AC-AC, DC-DC, DC-AC, and AC-DC voltages [2]-[4]. When a DC connection voltage is applied to classic inverters, eight voltage vectors are formed, six of which are active and two are null. These switching states are arranged in various ways to create PWM schemes [5].

Regardless of the input voltage, the output of the impedance source inverter is any value between zero and a big value. This is the main characteristic of the Impedance source inverter, which makes it a buck-boost inverter with a wide output voltage range. This feature is not available in typical inverters. Additional Shoot-through switching state (null vector) is offered in impedance source inverter, which is not included in standard inverters [6]. The fundamental challenge of the control schemes becomes the instructions to incorporate this Shoot-through state. Because the output voltage of the load is zero during this time, as it is with a standard inverter, due to a short circuit at the inverter's load terminal, as a result, in order to output a sinusoidal voltage, the active state's duty ratio must be maintained, suggesting that shoot-through only eliminates a few or all of the typical zero states. The shoot-through state can be achieved by the impedance source inverter in seven different ways: all 3-phase legs, any two-phase leg combination, and any phase leg. The active states, null states, and Shoot-through states of the impedance source inverter are all shown in Table 1. The mpedance source inverter functions as an analogous current source throughout every non-shoot-through switching state (active as well as null states) out of eight [7], [8].

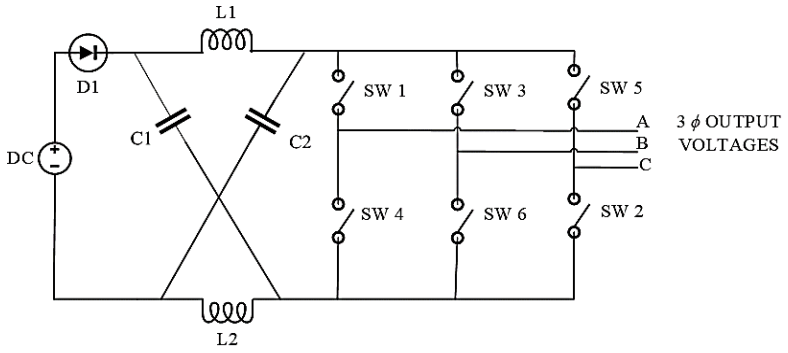

Figure 1. Power circuit diagram of impedance source inverter

Table 1. All the possible shoot-through states of z-source inverter

Output Voltage Vector	Switching States	SW 1	SW 4	SW 3	SW 6	SW 5	SW 2
E_1	ST_1	1	1	1	0	1	0
E_2	ST_2	1	0	1	1	1	0
E_3	ST_3	1	0	1	0	1	1
E_4	ST_4	1	1	1	1	1	0
E_5	ST_5	1	1	1	0	1	1
E_6	ST_6	1	0	1	1	1	1
E_7	ST_7	1	1	1	1	1	1

3. PWM TECHNIQUES FOR 3-PHASE IMPEDANCE SOURCE INVERTER

Controlling the result and creating variable voltage and recurrence are expected to gain the ideal result from the Impedance source inverter. Different customary PWM ways for exchanging a voltage-type z-source inverter are framed in [7]. Ali and Kamaraj [8] proposed depicts another space vector pulse width modulation (SVPWM) procedure for a 3-stage z-source inverter, and [9] portrays an altered SVPWM system for spreading shoot-through states into zero vectors. Sangari *et al.* [10] presents the examination and control of a solitary stage z-source inverter for consonant decrease and burden voltage guideline utilizing molecule swarm advancement particle swarm optimization (PSO) changed relative vital (PI) based SVPWM and second request sliding mode control (SOSMC) based SVPWM. Sabeur *et al.* [11] introduced a one-layered SVPWM (OD-SVPWM) modulator method to accomplish the most extreme voltage gain by choosing shoot-through states to such an extent that each switch is locked to the positive or negative dc rail for a span of (2π/3). Das *et al.* [12], suggested a clever exchanging design in the SVPWM was utilized to raise the capacitor voltage by dealing with a shoot-through time for z-source inverter AC. yield voltage the executives. Tang *et al.* [13] portrays a superior z-source inverter plan in which the capacitor voltage stress is significantly decreased, and the inrush current is restricted. To keep away from inrush current and reverberation among capacitors and inductors, the delicate beginning strategy has been talked about [14]. Zhu *et al.* [15] portrays an exchanged inductor (SL) z-source inverter that utilizes an S.L. organization to interface the power source with the fundamental circuit to increment voltage adaptability. This will further develop voltage support reversal capacity by using a short shoot-through zero state to accomplish high voltage transformation proportions.

The geography for exchanged impedance source inverter has been proposed in [16], which assists with diminishing weight, size, and cost by utilizing a larger number of dynamic components and a lower number of capacitors and inductors. Fathi *et al.* [17] portrays an exchanging strategy for an upgraded help z-source inverter that utilizes two impedance organizations and a low shoot-through obligation cycle. The capacity to surpass adjustment files in the straight region has been analyzed for impedance source inverter [18] utilizing two tweak strategies: changed space vector beat width balance technique miniature stereo vision machine (MSVM) and straightforward lift control session border controller (SBC). Hossam-Eldin *et al.* [19] used led and gave a nitty-gritty investigation of (ZSI) schemes upgrades for a very long time. Tang *et al.* [20] proposed talks about a PWM method that limits inductor swell current by modifying the shoot-through time stretches for 3-stage legs. Double exchanging recurrence regulation is accomplished by consolidating a high-recurrence beat width adjustment with a low-recurrence sinusoidal PWM (SPWM), which decreases the converter's exchanging misfortunes and kills the relationship between obligations cycle and balance record, as displayed in [21]. By adding an extra switch and diode to the result terminals of regular inverters, a P.V. framework utilizing exchanged impedance-source/semi-impedance-source dc-dc converters (SZSC/SQZSCs) has been shown to upgrade the low voltage to high voltage [22]. Most of the writing on z-source inverters centers around 3-stage or single-stage span inverters, despite the fact that [23] talks about single-stage z-source push-pull inverter geography. The incorporated enhanced-boost z-source inverter (EEB-ZSI) portrayed in [24] permits dc sources, for example, P.V. boards, to be installed into an even impedance organization, bringing about nonstop dc current and decreased voltage stress across exchanging gadgets. Because of spillage and stray inductances in the high-recurrence circle, attractively coupled impedance source (MCIS) converters are inclined to significant voltage spikes across the inverter span. To defeat this issue, [25] proposed a conventional inactive regenerative inductor-capacitor-diode (L-C-D) snubber that requires no progressions to the first circuit. A constant conduction mode (CCM) ZSI AC little sign identical circuit model in view of state-space averaging by scattering the shoot-through states into the no vectors without compromising the dynamic space vector has been proposed in [26].

Among these, the author described a few basic existing strategies for controlling and generating 3-phase sinusoidal output voltage, as well as a PWM switching scheme. An impedance network connects the dc-link voltage at the input to the 3-phase inverter circuit. An LC filter connects a 3-phase ac variable load to the inverter's output.

3.1. Carrier-based PWM scheme

The CB PWM system provides a sinusoidal output waveform with changing duration after filtering the pulse waveform. This approach compares a modulation signal to a triangular carrier signal. Figure 2 depicts the carrier-based PWM [27] principal. Modulation signals are created by adding a zero-sequence signal to all 3-phase sinusoidal signals that are shifted by 2π/3. Three inverter legs switching functions are formed when these signals are compared to a triangular-shaped high-frequency carrier signal. These switching capabilities are introduced to the impedance source inverter's legs. The DC-link voltage of the z-source inverter is at unity, with a switching frequency of 2 kHz, and the fundamental frequency at 50 Hz as simulation parameters. Figure 3 depicts the filtered output voltage of the impedance source inverter, whereas Figure 4 shows the harmonics for phase 'a' output voltage, i.e., 0.3927 p. u. at a fundamental frequency of 50 Hz.

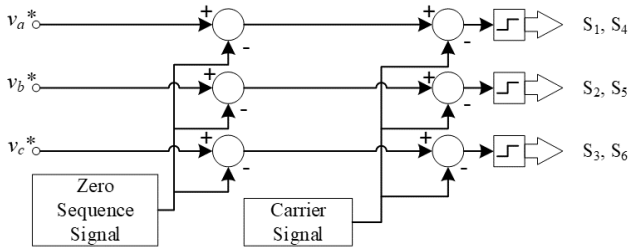

Figure 2. Operation of a carrier based PWM

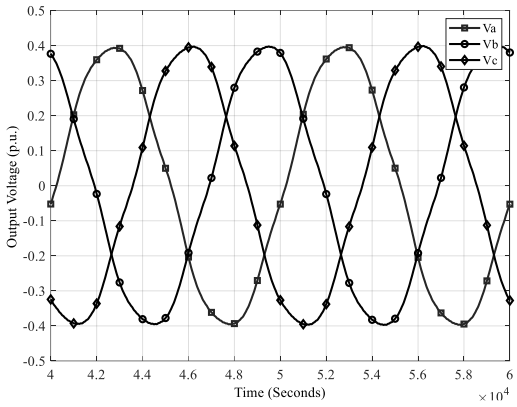

Figure 3. Output voltage

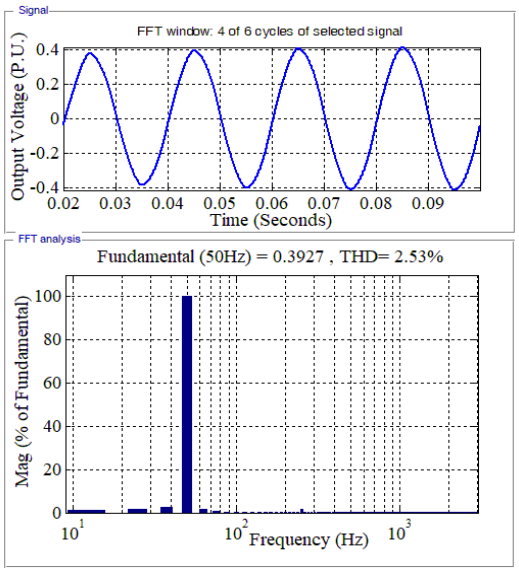

Figure 4. Harmonic for output phase' a voltage

3.2. Third-harmonic injection based PWM scheme

A PWM system based on third-harmonic injection [27] was devised to improve the inverter's efficiency. The magnitude of the reference must be decreased as much as possible to obtain high output voltage and higher dc bus utilization so that the reference can become equal in magnitude to the carrier without harming efficiency. When a reverse polarity harmonic is added to any signal, the amplitude of the reference signal is diminished. This scheme has the benefit of limiting the third-harmonic to the leg voltages and excluding it from the output.

The consequences of the third-harmonic injection in fundamental are seen in Figure 5. The simulated filtered output voltage results are shown in Figure 6, and the harmonic for phase 'a' output voltage is shown in Figure 7. The simulation results are identical to those in the preceding phase. The filtered output voltage is 0.3899 p. u. at the fundamental frequency.

3.3. Offset addition based PWM scheme

The index modulation is a metric that measures the magnitude of carrier signal modulation. It's vital because if it's not done correctly, the modulated signal will be distorted. To increase the modulation index, the offset voltage is added to the reference. The following equation can be used to compute the offset voltage:

$$V_{offset} = -\frac{V_{max} + V_{min}}{2} \; ; where \; V_{max} = max(V_a, V_b, V_c) \; and \; V_{min} = min(V_a, V_b, V_c)$$

Actually, the third-harmonic triangular-shaped signal with a magnitude of 25% of the fundamental is offset voltage. Due to the necessity for additional processes, this method is ideally suited for realistic implementation

The simulated results are shown in Figures 8-10. Figures 8 and 9 depict reference voltages with offset voltages, respectively, and Figure 9 depicts the filtered output voltage of an impedance source inverter utilizing an offset-addition based PWM scheme [27]. Figure 10 shows the harmonic of one phase 'a' output voltage at 50 Hz has a value of 0.3963 p. u. The simulation parameters are similar to those described in the previous section.

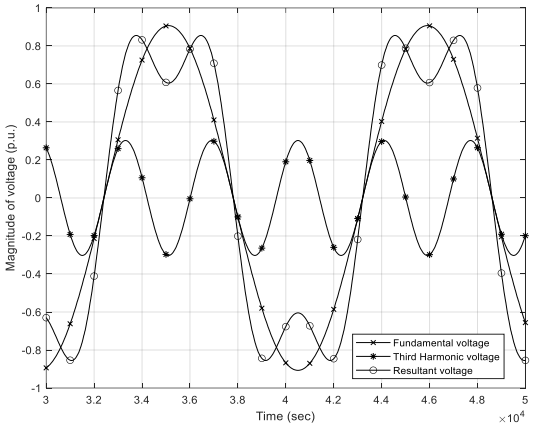

Figure 5. Simulation results showing the result of third-harmonic injection

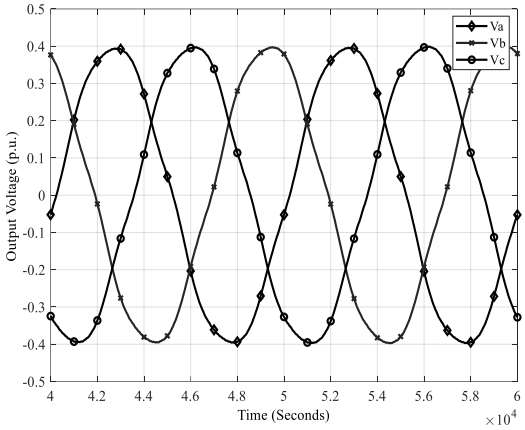

Figure 6. Output voltage

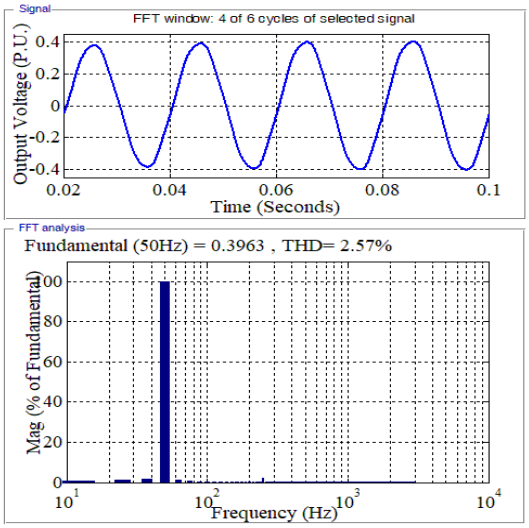

Figure 7. Harmonic for output phase 'a' voltage

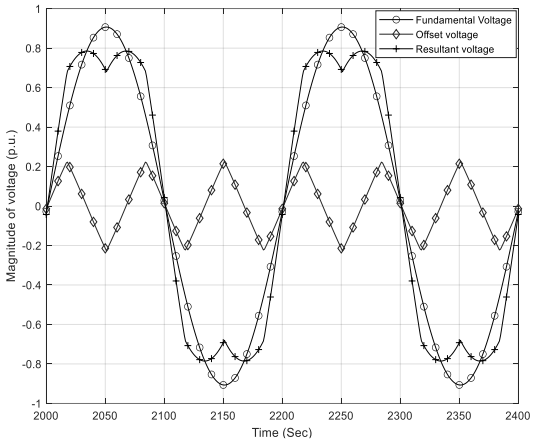

Figure 8. Reference voltage with offset addition

3.4. Time equivalent SVPWM scheme [28], [29]

To generate sinusoidal output, using TESVPWM, an algorithm for the scheme is

- Reference voltages *Vx; x=a, b, c* i.e., V_a, V_b & V_c, in every switching period T_s.
- Equivalent times of reference phase voltages T_1, T_2 & T_3 expression is, $T_{xs} = V_{xs}\, x\, \frac{T_s}{V_{dc}}$; *where* $x = a, b$ *and* c
- Determine T_{offset} using the equation; $T_{offset} = \frac{T_s}{2} - \frac{T_{max}+T_{min}}{V_{dc}}$; T_{max} is the maximum value, and T_{min} is the minimum value during sampling interval *Tx*.

– Then the inverter leg switching times are obtained as $T_{gx} = T_x + T_{offset}$; where x = a, b and c

Figure 11 shows the filtered output of an impedance source inverter using a time equivalent space vector pulse width modulation scheme, while Figure 12 shows the harmonic for phase 'a' output voltage is 0.3971 p. u. at the fundamental frequency of 50 Hz, using a dc value of unity as the base value.

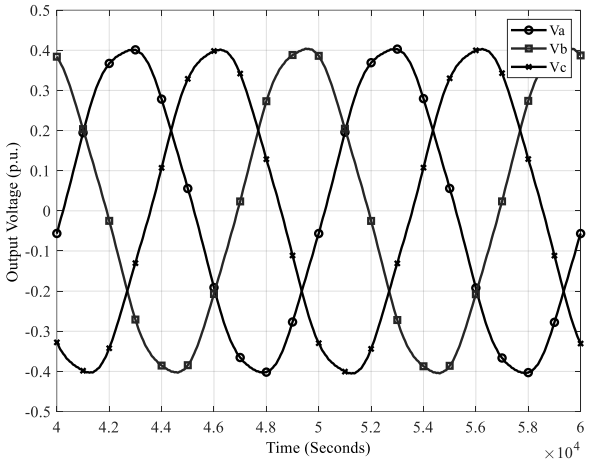

Figure 9. Output voltage

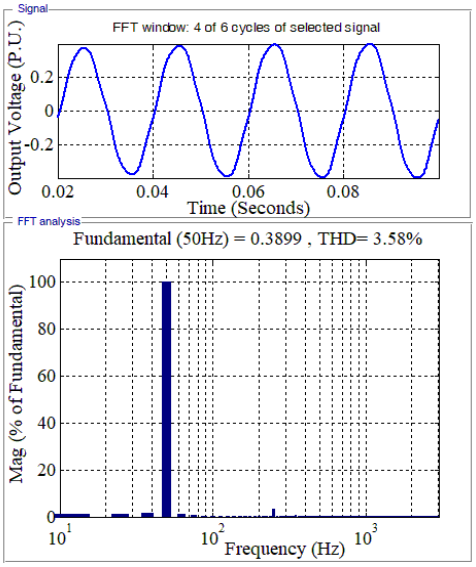

Figure 10. Harmonic for output phase' a voltage

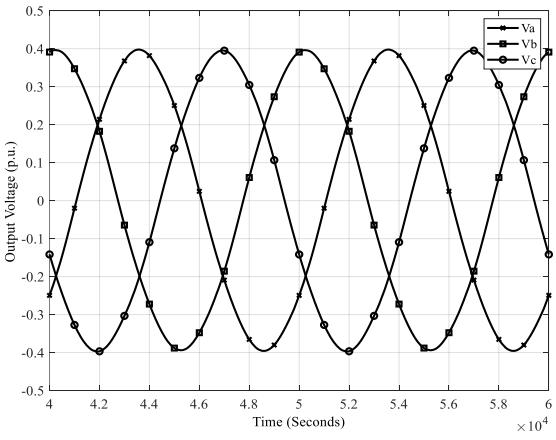

Figure 11. Output voltage

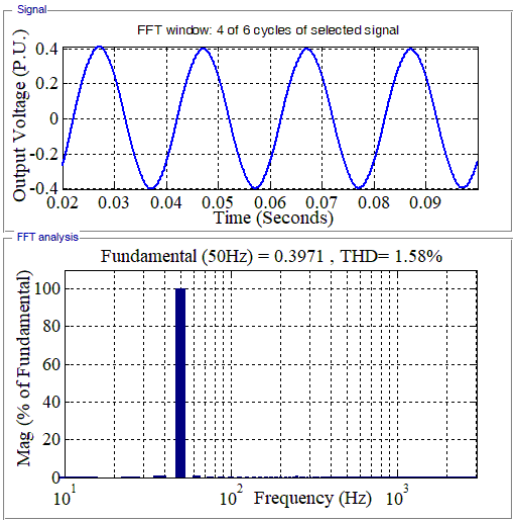

Figure 12. Harmonic for output phase 'a' voltage

4. COMPARATIVE STUDY

A bar chart of the various PWM schemes investigated for a 3-phase impedance source inverter is in Figure 13. The essential component of carrier-based PWM schemes has a peak value of 39.27% and a THD of 2.53%, according to the analysis. The fundamental component peak value of PWM based on third-harmonic injection is 39.63%, with a THD of 2.57%. Offset-addition based PWM's basic component has a peak value of 38.99% and a THD of 3.58%. While the suggested time equivalent SVPWM has a fundamental component peak value of 39.71% and a THD of 1.58%, the proposed time equivalent SVPWM has a fundamental component peak value of 39.71% and a THD of 1.58%. It is concluded that, when compared to other systems, the suggested Impedance source inverter system has the lowest THD.

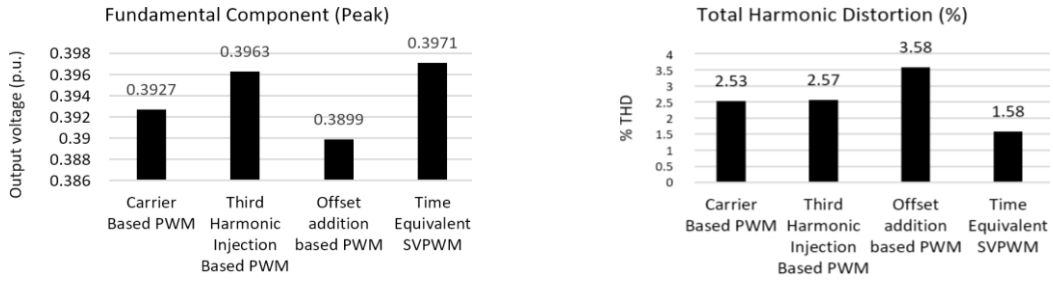

Figure 13. Bar chart of PWM schemes of 3-phase impedance source inverter

5. CONCLUSION

This research compares the proposed time equivalent SVPWM for Impedance source inverter to three pulse width modulation approaches. According to the analysis, the recommended approaches have the least total harmonic distortion with almost the same value as the fundamental component. As a result, the suggested time equivalent space vector PWM approaches are recommended for usage in fuel cell and high-power applications, as they will outperform other existing systems. All of the results are confirmed in the MATLAB/Simulink environment.

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