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A modified bridge-type nonsuperconducting fault current limiter for distribution network application

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ABSTRACT

The electrical distribution network is undergoing tremendous modifications with the introduction of distributed generation technologies which have led to an increase in fault current levels in the distribution network. Fault current limiters have been developed as a promising technology to limit fault current levels in power systems. Though, quite a number of fault current limiters have been developed; the most common are the superconducting fault current limiters, solid-state fault current limiters, and saturated core fault current limiters. These fault current limiters present potential fault current limiting solutions in power systems. Nevertheless, they encounter various challenges hindering their deployment and commercialization. This research aimed at designing a bridge-type nonsuperconducting fault current limiter with a novel topology for distribution network applications. The proposed bridge-type nonsuperconducting fault current limiter was designed and simulated using PSCAD/EMTDC. Simulation results showed the effectiveness of the proposed design in fault current limiting, voltage sag compensation during fault conditions, and its ability not to affect the load voltage and current during normal conditions as well as in suppressing the source powers during fault conditions. Simulation results also showed very minimal power loss by the fault current limiter during normal conditions.

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1. INTRODUCTION

In recent years, the electrical distribution network has grown in complexity with the introduction of distributed generation (DG). These additional technologies have led to issues of increased power losses, voltage sags/swells, and increased fault currents [1]. Research shows that high penetration of photovoltaic (PV) systems can lead to an increase in fault current magnitude in the order of 7% [2]. These fault currents are higher in locations closer to PV generations [3]. An increase in PV penetration leads to an increase in fault currents which also leads to an increase in protective relays fault currents, and these relays fault currents depend on the locations of the PV systems [4]. A sensitivity analysis on the impact of rooftop PV systems on the distribution network showed that the presence of PV systems on a low voltage feeder increased short circuit fault levels by 10% [5]. A single PV system will have very minimal contribution to fault current but when considering the collective contribution from all PV systems installed across the network, the fault

current contribution gets significantly higher with high PV penetration which could cause considerable problems in the fault clearing operation of protective devices [6]. The integration of DGs has led to today's power systems having a short circuit current greater than what the operating equipment can handle [7], [[8]. This could greatly affect the reliability of existing protective mechanisms and that of the network, but these reliabilities could be improved by using fault current limiting techniques such as fault current limiters [9].

Fault current limiters (FCLs) have been widely introduced in power systems as the most promising technology to effectively and efficiently suppress fault currents to satisfactory levels [10]. The main goal of FCLs is to lower the fault current to a level that the circuit breaker can conveniently and safely clear [11]. The utilization of FCLs in power system has not only been to suppress fault currents but has also been to enable voltage ride-through capabilities of wind farm doubly-fed induction generators [12], [13], enhance transient stability [14], eliminate voltage sags [15], improve power quality, limit inrush current in transformers [14] and increase the power transfer capability of the power system [16]. Various types of FCLs have been developed [17]; the most common being the superconducting fault current limiters (SFCLs), solid-state fault current limiters (SSFCL) and saturated core fault current limiters (SCFCL) [18]. SFCLs are the leading fault current limiting technology in the world and this is because of their high efficiency in suppressing fault currents, fast response, automatic recovery after fault clearance, and their superconducting ability that permits them to be invisible in the network during normal operation [19]. Notwithstanding, they are still not yet widely deployed because of the technology and the expensive nature of the superconductors [20]. This has led to the search for nonsuperconducting coils to be used in place of the superconducting coils to achieve simpler and cost-effective fault current limiters [21]; this type being the nonsuperconducting fault current limiters (NSFCLs). NSFCLs offer substantial alternatives to SFCLs due to their simplicity, affordability, and minimal power losses during normal operation [22], [23]. FCLs of any type are designed to be as close to ideal as possible; with an ideal FCL having the following qualities [24], a) an impedance of zero during normal operation, b) fast and automatic impedance appearance at the occurrence of a fault, c) sufficiently large impedance during fault conditions, d) rapid recovery after the fault has been cleared, e) should reliably limit the defined fault current, f) no power losses, and g) low cost.

However, achieving all these specifications on a single FCL is almost impossible [24]. A lot of research has been done on nonsuperconducting fault current limiters. For example, in [25], the authors compared the current limiting capabilities of a DC reactor-type NSFCL with those of SFCL and noticed that both fault current limiters led to the distortion of the line current and the load voltage, and consequently, affecting the power quality of the network. Testing results of the NSFCL showed a line current during fault being higher than that during normal conditions though far lower than the fault current when the NSFCL was not used. Hence, despite using that NSFCL, the source still produces a considerably high current (above the rated), unhealthy to the system during fault conditions until the fault is cleared. To cater for the line current and load voltage distortions, the authors proposed the use of a DC source in series with the DC reactor for the case of the NSFCL. In [26], a bridge-type fault current limiter that employs two isolation transformers was proposed but this made the design not cost-effective. Other researchers have proposed substantial topologies for fault current limiting, each presenting some drawbacks which include load current and voltage distortions, power losses, and cost ineffectiveness [21]-[27]. In this research work, the problems enumerated are addressed using a bridge-type NSFCL with a novel topology.

This paper proposes a modified bridge-type NSFCL for distribution network applications. The NSFCL is made up of a bridge rectifier, two DC reactors, a semiconductor switch, and a simple command circuit. The rest of this paper is structured as follows. The next section presents the simulation of the test network used to validate the efficiency of the proposed NSFCL. In Section 2.3, the proposed NSFCL is depicted and analytical analysis is carried out with the FCL inserted into the test network. In Section 3, the simulation results are presented and discussed, and this is followed by a conclusion.

2. RESEARCH METHOD

2.1. Simulation of the test network

In this work, a single-phase extraction of the balanced IEEE 4 node test feeder with the transformer removed is utilized as a test circuit or network. To obtain the test circuit, the load is referred to the primary side of the transformer and the transformer removed. A single phase of the resulting network is then extracted and used as a test circuit. The test network was built and simulated in PSCAD/EMTDC. The circuit is shown in Figure 1 and the network parameters are shown in Table 1. It is noted that the simulation results obtained agree very closely with those published by IEEE as seen in Table 2 [28].

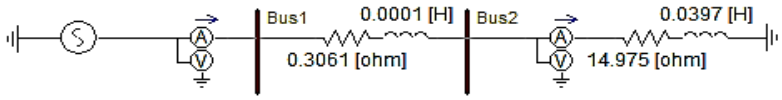


Figure 1. Test network

Table 1. Test network parameters

Component	Parameters
Source	Source Voltage, Vs = 7.2kV, Frequency, f_s = 60Hz
Transmission line impedance	Z_{line} = 0.3061 + jω0.0001 ohm
Load impedance	Z_{load} = 14.975 + jω0.0397 ohm

Table 2. Comparison of test network simulation results with published IEEE 4 node results

Parameter	Bus	IEEE	Test Network
Line to ground Voltage (kV)	01	7.199	7.199
	02	7.164	7.117
Phase Current (A)	01-02	336.8	336.133

2.2. Faults and fault current calculation

A fault is an abnormal condition in the electrical network that comes as a result of the failure of operating equipment. Two categories of faults can occur [29], a) The open-circuit fault that results in the seizure of current flow in the circuit, and b) the short-circuit fault that is as a result of insulation failure due to overloading and overstressing of feeders or degradation of feeder's insulation which leads to high current flow in the circuit.

Various methods are used for short-circuit fault current calculations, amongst them is the sequence method. The sequence method of fault calculation involves building the impedance matrix of the circuit and calculating the fault current. For an electrical circuit with a sending end voltage V_s, a line impedance Z_k and a load node *j*, the voltage V_j at node *j* before the occurrence of a ground fault at that node is given by;

$$V_j = V_s - I_j Z_k \quad (1)$$

After the fault occurrence, the voltage V_j is zero giving a change in voltage of $-V_j$. As a result, the current flow, I_{fj} from node *j* into the circuit is;

$$I_{fj} = -\frac{V_j}{Z_T} \quad (2)$$

Where I_{fj} is the current from node j due to the fault and Z_T the total impedance due to the fault given by;

$$Z_T = Z_k + Z_f \quad (3)$$

Where Z_k is the line impedance and Z_f is the fault impedance.
Since before the fault, no current was flowing into the circuit from node *j*, the fault current, I_f from the circuit into node *j* is then calculated as;

$$I_f = -I_{fj} = \frac{V_j}{Z_T} \quad (4)$$

The various types of short-circuit faults which are three-phase fault, single line-to-ground fault, double line-to-ground fault, and line-to-line fault differ in their calculations by their expressions for Z_T.

2.3. Proposed modified bridge-type nonsuperconducting fault current limiter

The topology of the proposed bridge-type NSFCL is shown in Figure 2 (a). The NSFCL is made up of 3 main parts; a bridge rectifier, DC reactors, and a semiconductor switch. An insulated gate bipolar transistor (IGBT) is used as the semiconductor switch. Two DC reactors; one of smaller value placed in series with the IGBT and one of larger value placed in parallel with the IGBT. The IGBT is controlled by a command circuit that turns it ON during normal conditions and OFF during fault conditions. The series reactor is aimed at limiting the abrupt change in the current flow through the IGBT during a fault condition. The DC reactors are modelled each with a reactance and a parasitic resistance.

2.3.1. Operation principle of the proposed NSFCL

The proposed modified bridge-type NSFCL operates as follows;

a. During normal conditions (no fault), the IGBT is turned ON and the parallel branch (R_p, L_p) short-circuited. The series reactor (L_s, r_s) is fully charged to the maximum current supplied by the source and therefore acts like a short-circuit. This makes it invisible to the network during normal conditions. The IGBT is kept ON by a command circuit that monitors the series reactor current and compares it with a predefined threshold value so that inasmuch as the series reactor current is lesser than the threshold current, the IGBT remains ON.
b. During a fault condition, the IGBT is turned OFF because the series DC reactor current, I_d becomes greater than the threshold current. The parallel reactor (L_p, R_p) is automatically and quickly inserted into the circuit, thereby limiting the fault current. The IGBT will continuously switch ON/OFF during fault conditions until the fault is cleared; leading to a distorted supplied current waveform during a fault condition. To solve this, an appropriate switching time is chosen for effective fault current limiting capabilities and a relatively smooth limited current during fault conditions.

2.3.2. Analytical analysis

The proposed NSFCL inserted into the test network is shown in Figure 2 (b) and analyzed as follows;

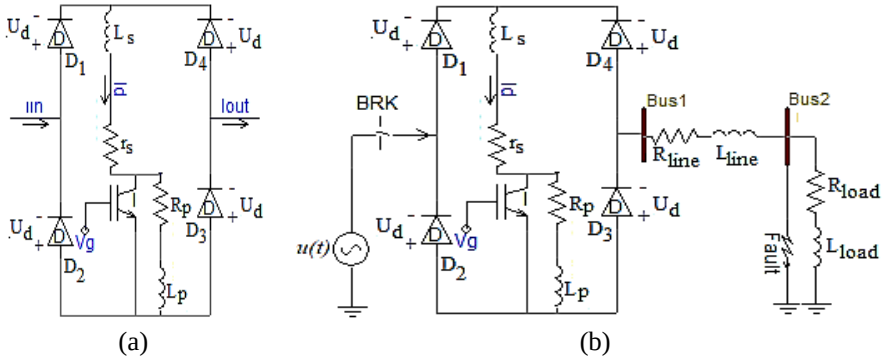


Figure 2. Proposed Bridge-type NSFCL, (a) standalone, (b) inserted into the test network

a. During normal conditions

The waveforms of the line and series DC reactor currents during normal conditions are shown in Figure 3. During normal conditions, the reactor charges during the positive cycle of the line current and discharges during the negative cycle. During charging, current flows from the source through D_1, L_s, r_s, IGBT, and D_3 to the load through the transmission line. The voltage equation, in this case, is given by;

$$u_{(t)} = U_d + L_s\frac{di_{(t)}}{dt} + r_s i_{(t)} + U_d + R_{line}i_{(t)} + L_{line}\frac{di_{(t)}}{dt} + R_{load}i_{(t)} + L_{load}\frac{di_{(t)}}{dt} \quad (5)$$

$$Usin(\omega t) = 2U_d + (L_s + L_{line} + L_{load})\frac{di_{(t)}}{dt} + (r_s + R_{line} + R_{load})i_{(t)} \quad (6)$$

$$Usin(\omega t) = 2U_d + L\frac{di_{(t)}}{dt} + Ri_{(t)} \quad (7)$$

where:

$$L = L_s + L_{line} + L_{load} \quad (8)$$

$$R = r_s + R_{line} + R_{load} \quad (9)$$

$$\text{The impedance, } Z = \sqrt{R^2 + (L\omega)^2} \quad (10)$$

$$\text{and } \tan\theta = \frac{L\omega}{R} \quad (11)$$

making $i_{(t)}$ the subject of the (9), we obtain

$$i_{(t)} = e^{-\left(\frac{R}{L}\right)(t-t_0)}\left[i_0 - \frac{U}{Z}\sin(\omega t_0 - \theta) + \frac{2U_d}{Z}\right] + \frac{U}{Z}\sin(\omega t_0 - \theta) - \frac{2U_d}{R} \quad (12)$$

$$i_{(t)} = i_{L(t)} = i_{d(t)}$$

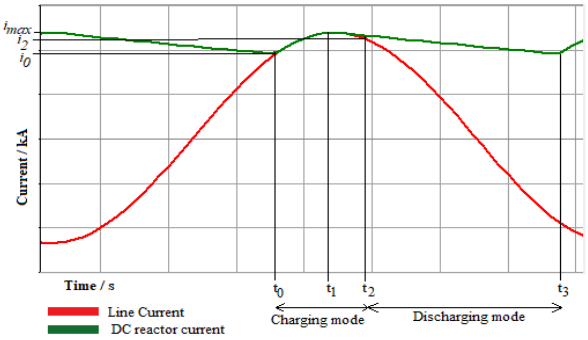


Figure 3. Line current and reactor current waveforms during normal operation

During the negative sequence of the line current, the series DC reactor is in the discharging mode which begins at t_2 as shown in Figure 3. In this mode, all the diodes are turned ON and the series DC reactor is short-circuited. Hence do not interfere in the normal operation of the network, implying.

$$2U_d + L_s\frac{di_{(t)}}{dt} + r_s i_{d(t)} = 0 \quad (13)$$

$$i_{d(t)} = e^{-\left(\frac{r_d}{L_d}\right)(t-t_2)}\left[i_2 + \frac{2U_d}{r_d}\right] - \frac{2U_d}{r_d} \quad (14)$$

the supplied line current in this mode can be obtained from;

$$U\sin(\omega t) = L\frac{di_{(t)}}{dt} + Ri_{(t)} \quad (15)$$

where:

$$L = L_{line} + L_{load} \quad (16)$$

$$R = R_{line} + R_{load} \quad (17)$$

therefore, from (17), line the current is obtained to be,

$$i_{L(t)} = e^{-\left(\frac{R}{L}\right)(t-t_2)}\left[i_2 - \frac{U}{Z}\sin(\omega t_2 - \theta)\right] + \frac{U}{Z}\sin(\omega t_2 - \theta) \quad (18)$$

where: $Z = \sqrt{R^2 + (L\omega)^2}$, $\theta = \tan^{-1}\frac{L\omega}{R}$ and $i_2 = i_{2(t)}$

The discharging of the series DC reactor is a result of its parasitic resistance. At $t = t_3$, the series DC reactor current again equalizes the line current. In the discharging mode; from t_2 to t_3, the DC reactor has no effect on the network because it is not being charged. Similarly, the effect the series DC reactor has on the network in the charging mode is very negligible because the current it carries is almost equal to that of the line current. The charging and discharging currents of the series DC reactor are shown in equations (12) and (18). From these equations, it is seen that both charging and discharging currents consist of ripple and DC components. It is important to minimize the ripple component as much as possible because it is responsible for the voltage drop across the series DC reactor's inductance, L_s during normal operation [30]. The series DC reactor current is given by

$$i_{DC} = i_{max} - \frac{i_{rd,p-p}}{2} \quad (19)$$

where i_{max} is the reactor's maximum current and $i_{rd,p-p}$ is the peak to peak value of the reactor AC current. From Figure 3,

$$i_{rd,p-p} = i_{max} - i_2 \quad (20)$$

integrating the discharging equation (18), we obtain

$$i_{rd,p-p} \cong \frac{T}{L_s}\left(\frac{r_s i_{max}}{2} + U_d\right) \quad (21)$$

where: $T = (t_3 - t_0) = 10ms$ for 50Hz networks [30].

From (19) and (20).

$$i_{DC} \cong i_{max}\left(1 - \frac{r_s T}{4L_s}\right) - \frac{U_d T}{2L_s} \quad (22)$$

for $r_s = 0$

$$i_{DC} \cong i_{max} - \frac{U_d T}{2L_s} \quad (23)$$

$$i_{rd,p-p} \cong \frac{T}{L_s} U_d \quad (24)$$

from (23) and (24), it is seen that increasing L_s increases I_{DC} and reduces the ripple component.

b. During fault conditions

During fault conditions, the IGBT is turned OFF and the parallel path is automatically and instantly inserted into the network. In the charging mode in fault conditions, the source voltage is given by

$$U\sin(\omega t) = 2U_d + L\frac{di_{(t)}}{dt} + Ri_{(t)} \quad (25)$$

where:

$$L = L_s + L_{line} + L_p + L_{load} \quad (26)$$

$$R = r_s + R_{line} + R_p + R_{load} \quad (27)$$

$$Z = \sqrt{R^2 + (L\omega)^2} \quad (28)$$

$$\theta = \tan^{-1}\left(\frac{L\omega}{R}\right) \quad (29)$$

making $i_{(t)}$ the subject of (25), we obtain

$$i_{(t)} = e^{-\left(\frac{R}{L}\right)(t-t_7)}\left[i_7 - \frac{U}{Z}\sin(\omega t_7 - \theta) + \frac{2U_d}{Z}\right] + \frac{U}{Z}\sin(\omega t_7 - \theta) - \frac{2U_d}{R} \quad (30)$$

$i_{(t)} = i_{L(t)} = i_{d(t)}$ and $i_7 = i_{7(t)}$

Where t_7 is the time instant during fault when charging mode begins and i_7 the current at that time. During the discharge mode, just like in the normal condition, all the diodes enter into conduction and isolate the reactors from the circuit.

Applying Kirchhoff's voltage law;

$$2U_d + L_s\frac{di_{(t)}}{dt} + r_s i_{d(t)} + L_p\frac{di_{(t)}}{dt} + r_p i_{d(t)} = 0 \quad (31)$$

$$i_{d(t)} = e^{-\left(\frac{R_d}{L_d}\right)(t-t_9)}\left[i_8 + \frac{2U_d}{R_d}\right] - \frac{2U_d}{R_d} \quad (32)$$

where

$$R_d = r_s + R_p \quad (33)$$

$$L_d = L_s + L_p \quad (34)$$

t_9 is the start of discharging during fault condition. The supplied current (inrush current) in this mode is obtained from

$$U\sin(\omega t) = L\frac{di_{(t)}}{dt} + Ri_{(t)} \quad (35)$$

where:

$$L = L_{line} + L_{load} \quad (36)$$

$$R = R_{line} + R_{load} \quad (37)$$

therefore, the inrush current could be obtained from (35),

$$i_{L(t)} = e^{-\left(\frac{R}{L}\right)(t-t_9)}\left[i_9 - \frac{U}{Z}\sin(\omega t_9 - \theta)\right] + \frac{U}{Z}\sin(\omega t_9 - \theta) \quad (38)$$

where

$$Z = \sqrt{R^2 + (L\omega)^2},\ \theta = \tan^{-1}\frac{L\omega}{R},\ i_9 = i_{9(t)}$$

c. Power losses through the FCL during normal operation

The active power loss through the DC reactor is given by;

$$P_{DCloss} = r_s i_{DC}^2 = r_s\left[\left[i_{max}\left(1 - \frac{r_s T}{4L_s}\right) - \frac{U_d T}{2L_s}\right]^2 \quad (39)$$

Assuming the ripple component of the reactor current being very small compared to the DC component and negligible,

$$i_{DC} = i_{max} \quad (40)$$

hence,

$$P_{DCloss} = r_d i_{max}^2 \quad (41)$$

load active power is given by

$$P_{load} = U_{load} i_{load}\cos\theta \quad (42)$$

$$P_{DCloss} = r_s i_{DC}^2 = r_s\left[\left[i_{max}\left(1 - \frac{r_s T}{4L_s}\right) - \frac{U_d T}{2L_s}\right]^2 \quad (39)$$

Assuming the ripple component of the reactor current being very small compared to the DC component and negligible,

$$i_{DC} = i_{max} \quad (40)$$

hence,

$$P_{DCloss} = r_d i_{max}^2 \quad (41)$$

load active power is given by,

$$P_{load} = U_{load} i_{load}\cos\theta \quad (42)$$

the ratio of active power loss by the NSFCL to that of the load reactive power, n is given by,

$$n = \frac{P_{DCloss}}{P_{load}} = \frac{r_s i_{max}^2}{U_{load} i_{load} \cos(\theta)} \quad (43)$$

therefore, for our test network of U_{load}=7.2kV, i_{load}=336.128A, cosθ=0.9, r_d=0.003 and i_{max}=475.357A,

$$n = 0.31\%$$

It is seen that the power loss as a result of the introduction of the fault current limiter is very small and negligible compared to the overall feeder losses.

d. Voltage drop and power loss compensation

The voltage drop in the proposed modified bridge-type NSFCL is across the power electronic switch (IGBT) and the series DC reactor during normal operation. This voltage drop can be resolved by appropriately sizing a DC power source or rectifier circuit and placing it in series with the series reactor as shown in Figure 4. The DC voltage source will aid in smoothening the DC reactor current during normal operation. Hence eliminating the ripple component of the DC current and thereby reducing the power loss in the NSFCL. The voltage of the DC source is calculated as:

$$U_{bat} = 2U_d + U_{sw} + r_s I_d \quad (44)$$

where:
U_{bat} is the DC source voltage, U_d is the voltage drop across a single diode, U_{sw} is the voltage drop across the IGBT, r_s is the series DC reactor resistance and I_d is the reactor current.

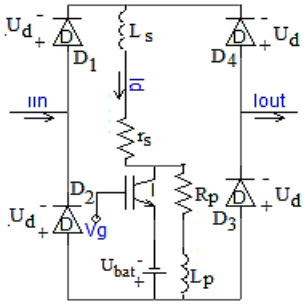


Figure 4. Voltage drop compensation using a DC source

3. RESULTS AND DISCUSSION

The parameters chosen for the simulation of the proposed bridge-type NSFCL using PSCAD/EMTDC are shown in Table 3. Electromagnetic transient analysis of the test network was done without the proposed modified bridge-type NSFCL, with the NSFCL, and with the NSFCL with battery. The simulation settings were; a) simulation runtime of 0.5s, b) a line-to-ground fault occurred at 0.3s and lasted for 0.05s, and c) the circuit breaker cleared the fault 0.03s after its occurrence (that is at 0.33s) and restored the network 0.07s later (at 0.4s). The simulation results are:

Table 3. Simulation parameters

	Parameters
Source	Source Voltage, Vs = 7.2kV, Frequency, f_s = 60Hz
Transmission line impedance	Z_{line} = 0.3061 + jω0.0001 ohm
Load impedance	Z_{load} = 14.975 + jω0.0397 ohm
Fault	Fault ON resistance, R_f = 0.01 ohm
Fault Current Limiter	L_s = 0.01H, r_s = 0.003 ohm, L_p = 0.2H, R_p = 20 ohm, U_d = 1V

3.1. Line current

The line current shoots to more than 30kA during fault conditions when no NSFCL is used as can be seen in Figure 5. With the insertion of the proposed bridged-type NSFCL, the fault current is limited to the desired value (below 0.6kA), thereby protecting the source and the load during fault and enabling the circuit breaker to safely clear the fault as shown in Figures 6 (a) and (b). This also removes any possible stress on the network during fault conditions. The introduction of a DC source in the NSFCL smoothens the DC reactor current during normal conditions (Figure 6 (b)) compared to without the DC source (Figure 6 (a)). Hence reduces power losses in the NSFCL as shown in Table 4. In addition, the designed bridge-type NSFCL does not affect the line current waveform during normal conditions as seen in Figures 7 (a)-(c).

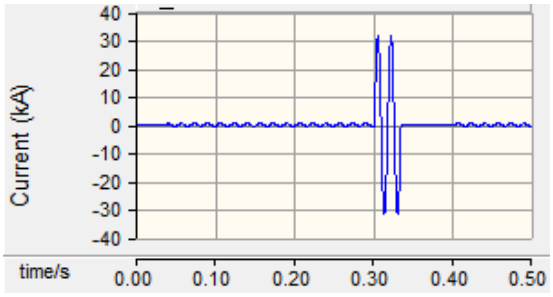


Figure 5. Line current during normal, fault, fault cleared and system restored conditions with no NSFCL

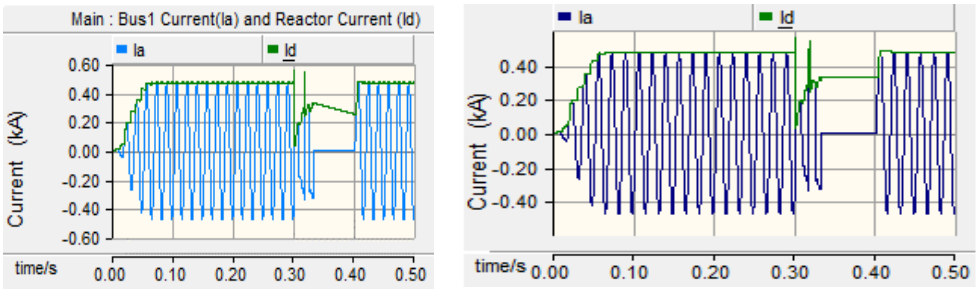


Figure 6. Line current (Ia) and reactor current (Id) during normal, fault, fault cleared and system restored conditions with NSFCL, (a) NSFCL with no DC source, (b) NSFCL with DC source

Table 4: Comparison of power losses and voltage drop with no FCL, with FCL and with FCL with battery

	No FCL			With FCL with no battery			With FCL with battery		
	Sending End	Receiving End	Losses	Sending End	Receiving End	Losses	Sending End	Receiving End	Losses
Active Power/kW	1.851	1.784	0.067	1.818	1.772	0.046	1.82	1.778	0.042
Reactive Power / kVar	1.564	1.563	0.001	1.559	1.552	0.007	1.562	1.557	0.005
Voltage / kV	7.199	7.117	0.082	7.199	7.097	0.102	7.199	7.107	0.092

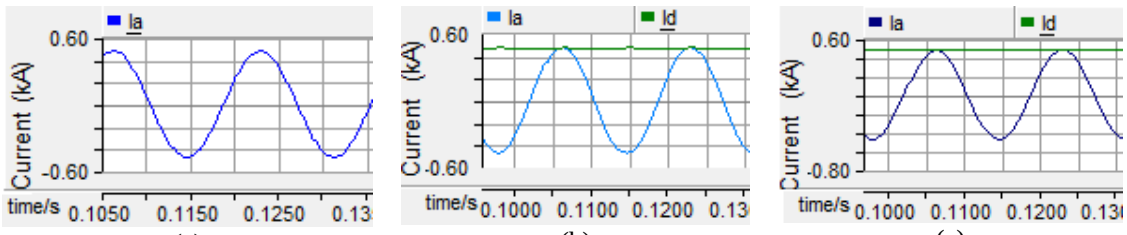
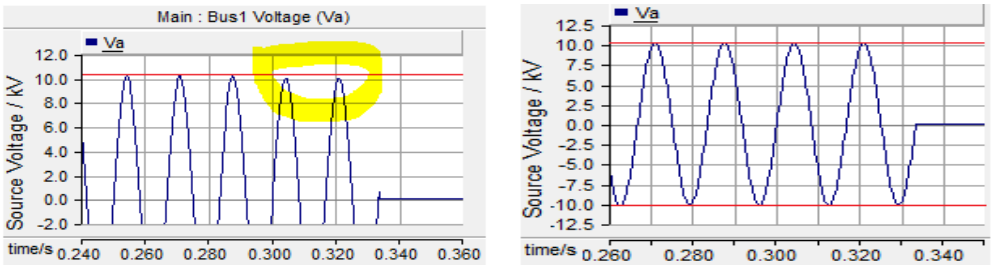


Figure 7. No Distortion in line current during normal conditions, (a) No NSFCL, (b) NSFCL with no DC source, and (c) NSFCL with DC source

3.2. Sending end voltage

During a fault condition, the sending end voltage experiences a slight drop in magnitude when no NSFCL is used as is seen in Figure 8 (a). This voltage drop is a result of stress on the power source due to the fault. This stress is removed by the proposed NSFCL and therefore no voltage drops during fault condition Figure 8(b). This makes the proposed NSFCL suitable for voltage ride-through applications.

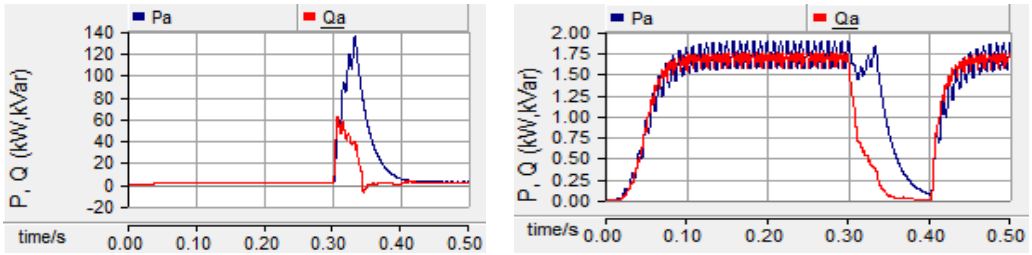


(a) (b)

Figure 8. Sending end voltage, (a) No NSFCL, and (b) with NSFCL

3.3. Sending end active and reactive power

The occurrence of the line-to-ground fault leads to an overshoot of the active and reactive powers supplied by the source when no NSFCL is used leading to dangerous stress on the generating units and excess system overload as shown in Figure 9 (a). This situation is adequately solved by the proposed NSFCL which keeps the supplied active and reactive powers within limits during fault conditions until the fault is cleared by the circuit breaker as can be seen in Figure 9 (b).

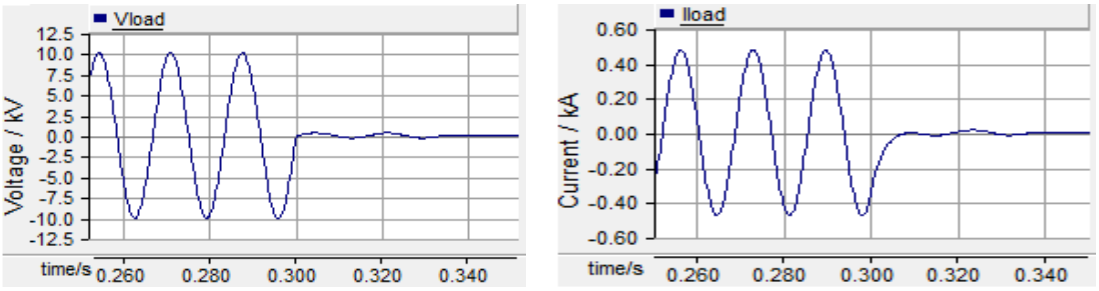


(a) (b)

Figure 9. Supplied active (Pa) and reactive (Qa) power during a fault condition (a) No NSFCL, and (b) with NSFCL

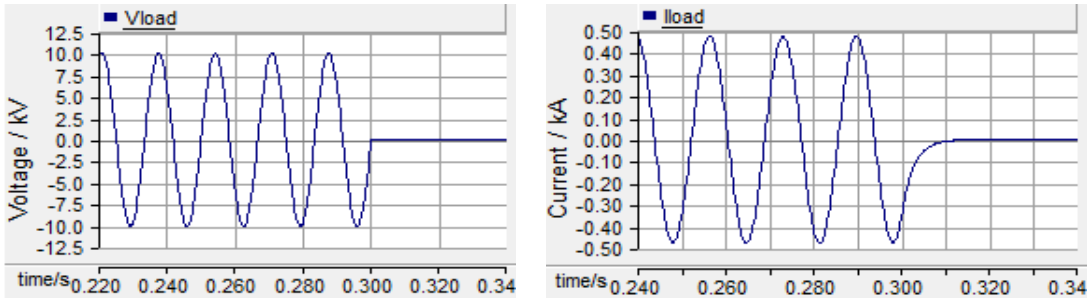
3.4. Load (receiving end) voltage and current

When no NSFCL is used in the network, the load continues to receive small voltage and current during fault condition until the fault is cleared as shown in Figures 10 (a), and (b). The insertion of the proposed NSFCL into the network suppresses these ripples during fault conditions as illustrated in Figures 11 (a) and (b). It should also be noted that the proposed modified bridge-type NSFCL does not distort load voltage and current waveforms during normal conditions even without the DC source. Therefore, the proposed design does not introduce total harmonic distortions in the network.



(a) (b)

Figure 10. Load Voltage at fault occurrence, (a) No NSFCL, and (b) With NSFCL



(a) (b)

Figure 11. Load current at fault current occurrence, (a) No NSFCL, and (b) With NSFCL

4. CONCLUSION

In this paper, the necessity of fault current limiters in power systems were examined and the drawbacks of existing NSFCLs were outlined. The aim was to propose an efficient and effective bridge-type nonsuperconducting fault current limiter with a novel topology for distribution network applications. The target was to develop an NSFCL that is almost invisible to the network during normal network operation and therefore leading to very minimal power losses, and on the other hand, adequately limiting the fault current to desired values during fault conditions. The proposed modified bridge-type NSFCL was designed and simulated using PSCAD/EMTDC and results showed outstanding performance of the novel NSFCL in, i) fault current limiting, ii) sending end voltage sag compensation during the fault, iii) suppression to desired values of supplied active and reactive powers during fault conditions, iv) not distorting load voltage and current waveforms, and v) minimal power losses during normal condition.

The proposed modified bridge-type NSFCL proves to be better than existing NSFCLs in terms of the reduced number of components used and the novel series and parallel DC reactors configuration used. The proposed novel NSFCL is a cost-effective and all-in-one efficient solution for distribution network fault current limiting, voltage ride-through capability enhancement, power quality improvement, and voltage sag compensation. These problems are problems that are faced by the distribution network with the increasing number of DGs being integrated into the network. With the proposed bridge-type NSFCL, there will be no need for protective equipment upgrades or replacement. The future of this research work will be the practical implementation of the proposed NSFCL to validate its practical effectiveness as simulation results have demonstrated its effectiveness in distribution network applications.

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