

A proposed asymmetrical configuration of cascaded multilevel inverter topology for high level generation

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ABSTRACT

Multilevel inverters are having high demand in high power applications. It works in medium voltage range. In this converter, for specific time intervals fewer switches will be conducting so switching loss is also reduced. This paper represents overall total harmonic distortion (THD) for different levels and different carrier frequencies. Switching loss, conduction loss of inverter has been discussed and hence inverter efficiency can be calculated. Phase displacement pulse width modulation method has been proposed in order to generate pulses. The proposed topology is well presented by its practical implementation with two current direct sources. All the simulations are being carried out using MATLAB/Simulink platform to validate the hardware results.

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1. INTRODUCTION

Multilevel inverters are highly in demand in high power and medium voltage applications [1]. There are mainly three different types of multilevel inverters are being focused for industrial applications. Various topologies had been developed since 1970. It can be interfaced to renewable sources i.e., solar photo voltaic, wind and fuel gas [2]–[4]. Considering the number of components, high reliability cascaded multi level inverter (MLI) is being chosen. As the number of level increases, the number of H-bridges also increases [5], [6]. This makes the system more complicated. By increasing the number of levels in the inverter, the output voltages have more steps generating a staircase waveform, which has a reduced harmonic distortion. Depending upon the voltages sources cascaded MLI are classified into two, i.e. symmetrical and asymmetrical Cascaded MLI [7]. Direct voltages are having different values in asymmetrical Cascaded multilevel inverter [8]. So, the Inverter achieves higher number of voltage levels compared with symmetrical configuration for same number of level generation [9], [10]. Several newly developed MLI topologies, popularly known as “reduced device count (RDC),” have been reported in recent years [11]–[15]. In this paper a novel topology has been proposed and its asymmetrical configuration has been emphasized to produce more number of levels. As the number of levels increased the output waveforms become more sinusoidal in nature. Hence total harmonic distortion (THD) reduces. Phase-shifted and level-shifted are the two modulation schemes using carrier based pulse width modulation (PWM). Using the same frequency modulation index in the different modulation techniques, the equivalent switching frequency in the level shifted technique is significantly lower than in the phased shifted method [16]–[21]. This turns into a better

harmonic performance. Hence level shifted PWM techniques are being used. The main features of the proposed topology is it has reduced number of dc sources and semiconductor switches also.

2. RESEARCH METHODOLOGY

2.1. Existing topology

The existing topology as shown in Figure 1 has two voltage sources V_1 and V_2 . It has two capacitors C_1 and C_2 connected to one voltage source side i.e., V_1 and seven switches. If the values of V_1 and V_2 are equal it is treated asymmetrical configuration. It can produce up to 11 levels with certain voltage combination. Hence to generate higher levels a new modified topology has been proposed in Figure 2.

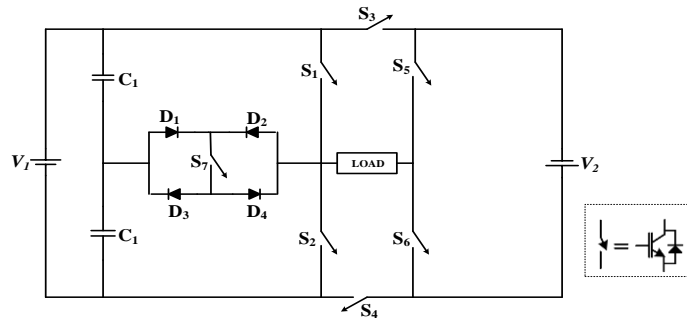


Figure 1. Existing topology

2.2. Proposed topology

The existing topology has been modified and represented in Figure 2 in order to generate higher levels. As the proposed topology also generates same levels of output voltage and current waveforms in symmetrical configuration of existing topology, its asymmetrical configuration has been highlighted and presented in this section. It has two voltage sources i.e., V_1 and V_2 and four capacitors i.e., C_1 - C_4 connected as shown in Figure 2. It has six unit directional i.e., S_1 , S_2 , S_3 , S_4 , S_7 , and S_8 and two bidirectional switches i.e., S_5 and S_6 in the circuit.

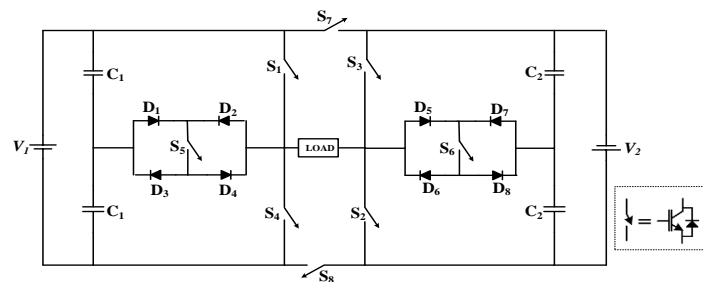


Figure 2. Modified topology

3. MODES OF OPERATION

In this section different modes of operation of the proposed converter for thirteen level generation have been represented from mode 1 to mode 13 order to generate first level i.e., V_{dc} , S_5 , S_2 and S_8 are conducting. Similarly, to generate second level, in mode 2 operation, S_6 , S_4 , and S_8 are turned on keeping capacitor C_2 charged. In mode 3 operation, C_2 discharged by charging capacitor C_1 . In order to generate all the six positive levels, the lower switch i.e., S_8 is being turned on and to generate all the six negative levels, switch S_7 has been turned on in the Figure 2. Similarly, S_1 , S_7 , S_3 , or S_2 , S_4 , and S_8 are turned ON, short circuiting the load, to generate zero level respectively.

4. SWITCHING STATES

This section represents various switching states of the proposed topology. It shows $V_1=V/2$, $V_2=V$ where $V_{dc}=V/4$ which is known as unsymmetrical binary configuration, to generate 13 level and $V_1=V$, $V_2=3V$ where $V_{dc}=V/2$, which is called as unsymmetrical trinary configuration, to generate 17 levels respectively. Figure 3 depicts to generate first level i.e., V_{dc} in thirteen level generations Switches S_5 , S_2 , S_8 are conducting. To generate second level i.e., $2V_{dc}$ in thirteen level generations switches S_6 , S_4 , S_8 are conducting. Similarly, six positive levels are generated and six negative levels are generated along with zero level as represented in different modes of operation in Figure 3 (see Appendix). Table 1 explains the different switching strategies of the proposed converter. It also depicts about the switches and diodes are conducting for particular level generation.

Table 1. Different switching strategies

13 Levels			17 Levels		
Output	Conducting switches	Conducting Diodes	Output	Conducting switches	Conducting Diodes
V_{dc}	S_5, S_2, S_8	D1, D4	V_{dc}	S_5, S_2, S_8	D1, D4
$2V_{dc}$	S_6, S_4, S_8	D5, D6	$2V_{dc}$	S_1, S_2, S_8	NIL
$3V_{dc}$	S_5, S_6, S_8	D1, D4, D5, D8	$3V_{dc}$	S_8, S_4, S_6	D5, D8
$4V_{dc}$	S_8, S_4, S_3	NIL	$4V_{dc}$	S_8, S_5, S_6	D1, D2, D3, D4
$5V_{dc}$	S_8, S_5, S_3	D1, D4	$5V_{dc}$	S_1, S_6, S_8	D5, D8
$6V_{dc}$	S_8, S_1, S_3	NIL	$6V_{dc}$	S_8, S_4, S_3	NIL
0	S_1, S_3, S_7	NIL	$7V_{dc}$	S_8, S_5, S_3	D1, D4
$-V_{dc}$	S_5, S_3, S_7	D2, D3	$8V_{dc}$	S_8, S_1, S_3	NIL
$-2V_{dc}$	S_7, S_1, S_6	D7, D6	0	S_1, S_2, S_3	NIL
$-3V_{dc}$	S_5, S_6, S_7	D7, D6, D2, D3	$-V_{dc}$	S_7, S_3, S_5	D2, D3
$-4V_{dc}$	S_2, S_1, S_7	NIL	$-2V_{dc}$	S_7, S_3, S_4	NIL
$-5V_{dc}$	S_2, S_5, S_7	D2, D3	$-3V_{dc}$	S_6, S_1, S_7	D7, D6
$-6V_{dc}$	S_2, S_4, S_7	NIL	$-4V_{dc}$	S_6, S_5, S_7	D2, D3, D7, D6
x	x	x	$-5V_{dc}$	S_7, S_6, S_4	D7, D6
x	x	x	$-6V_{dc}$	S_2, S_1, S_7	NIL
x	x	x	$-7V_{dc}$	S_2, S_7, S_5	D2, D3
X	x	x	$-8V_{dc}$	S_2, S_4, S_7	NIL

5. SIMULATION RESULT ANALYSIS

Various types of the pulse width modulation (PWM) techniques are existing out of which level shifted PWM technique is being considered because of its many advantages over other conventional techniques. Figure 4 depicts the simulation diagram of the proposed converter at carrier frequency 10 KHz and modulation index at 1. S_5 and S_6 are two bidirectional switches and $S_1, S_2, S_3, S_4, S_7, S_8$ are unidirectional switches in Figure 2. Figure 4 represents load voltage and load current wave form at carrier frequency = 10 KHz. Simulation has been carried out for $R=10\ \Omega$, $L=25\text{ mH}$ at modulation index 1.

Figure 4 (a) indicates output load voltage for 13 level. Average output voltage is 43.85 V at THD=5.44%. The fundamental cycle has been represented in voltage waveform which is from 0 to 0.02 sec. Voltage THD also within IEEE standard. Six positive levels, six negative levels of unequal voltage distribution represented in Figure 4 (a) which shows the asymmetric nature of the proposed multilevel inverter. Figure 4 (b) indicates output load current for 13 level. Average output load current is 3.45 A at THD = 0.28%. Current THD is also within IEEE standard.

Fundamental cycle has been represented in voltage waveform which is from 0 to 0.02 sec. Figure 4 (c) indicates average output voltage is 38.85 V with THD=3.9%. Figure 4 (d) indicates average output current is 3.5A with THD=1.7%. Voltage THD also within IEEE standard. Eight positive levels, eight negative levels of unequal voltage distribution along with zero level represented in Figure 4 (c) which shows the asymmetric nature of the proposed multilevel inverter. Figure 4 (d) indicates output load current for 17 level. Average output load current is 3.5 A at THD=1.7%. Current THD is also within IEEE standard. Figures 4 (a) and 4 (b) also depict with increase in level generation of the same converter THD is reduced.

Table 2 depicts various losses occurred across the semiconductor switches i.e., at 10 KHz carrier frequency. Table 2 also describes that conduction loss across the switches is same where, as switching loss depends on the usability of the switch. Switches S_7 and S_8 are mostly used when the converter is working to generate positive levels and negative levels respectively. Hence switching losses are more in S_7 and S_8 compared to other switches.

Table 3 depicts about the inverter loss. According to the various researchers [22]–[25] an inverter has major two types of losses i.e., switching loss which occurs when a switch is conducted (turn on) and also when it is in off state (turn off), conduction loss when the switch is in conduction state. It has been calculated from its input power and output power with its voltage THDs and current THDs. Table 3 depicts with increase in

carrier frequency voltage THD enhanced and current THD decreased. At 10 KHz carrier frequency voltage THD and current THD are found to be minimum. Hence it is the optimum condition of the converter which can be considered for hardware realization.

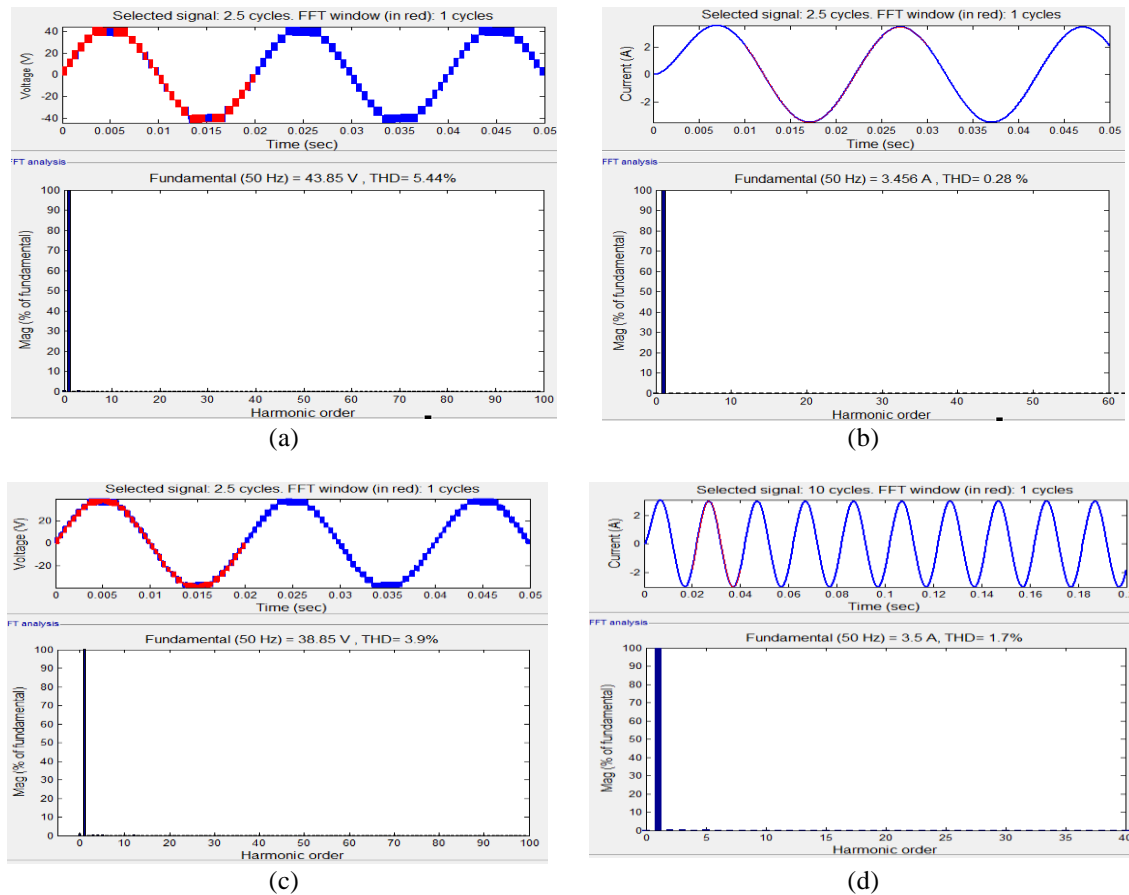


Figure 4. Simulation results of voltage across load and current for (a) asymmetrical output voltage signals, (b) asymmetrical output current signal, (c) asymmetrical output voltage signal, and (d) asymmetrical output current (17 level)

Table 2. Loss calculation at 10 KHz carrier frequency

	S_1	S_2	S_3	S_4	S_5	$S_6 S_7$	S_8 Total
Switching loss (in W)	0.035	0.0016	0.0012	0.0023	0.05	0.0489	0.06 0.259
Conduction Loss (in W)	0.0051	0.0052	0.005	0.0052	0.0055	0.0051	0.005 0.045 0.081
Total Loss (in W)	0.0401	0.0068	0.0062	0.0075	0.0555	0.054	0.065 0.105 0.249

Table 3. Inverter loss and THD across the RL-load

Carrier Frequencies (in KHz)	Input power (in W)	Output power (in W)	Inverter (in W)	VTHD	ITHD
1	62.26	56.7	8.56	6.36	1.91
3	65.9	57.20	8.7	6.72	1.45
5	66.83	57.6	9.23	6.89	1.05
7	68.11	58.6	9.51	6.98	0.74
10	69.49	59.22	10.27	5.44	0.28

Table 4 depicts voltage THD is reduced and current THD is increased with increase in modulation index. Hence it is always advised to operate the converter at high carrier frequency and at modulation index 1. At 10 KHz carrier frequency voltage THD and current THD are found to be minimum at modulation index 1. Figure 5 represents current THD at various carrier frequencies of the inverter. Current THD has been reduced as the carrier frequency increases. It indicates that current becomes more sinusoidal at higher carrier

frequencies. With high modulation index voltage THD reduces which has been observed in Figure 6. Hence it was advised to operate the inverter at modulation index 1 in order to make the inverter output more distortion free. Also, in Table 4 it was mentioned clearly.

Table 4. Modulation index versus THD of proposed topology (13 level)

Modulation Index	V_{THD}	I_{THD}
0.6	12.2	0.12
0.7	11.8	0.18
0.8	10.42	0.22
0.9	7.72	0.25
1	5.44	0.28

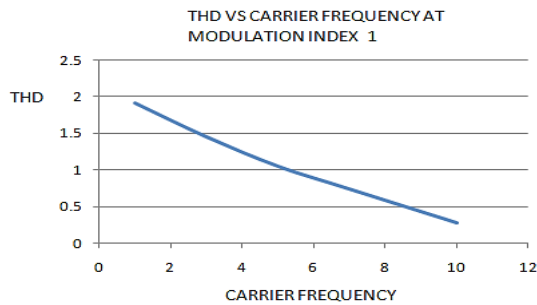


Figure 5. Current THD vs carrier frequency

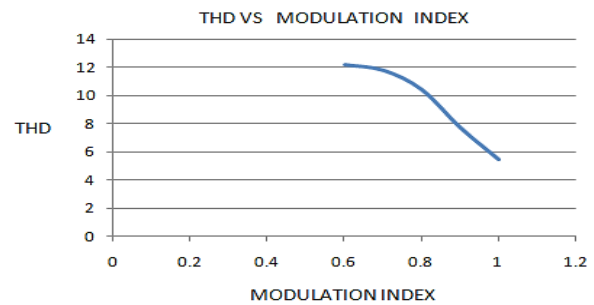


Figure 6. Voltage THD vs modulation index at 10 KHz

6. HARDWARE REALIZATION

To verify the effectiveness of the proposed topology, experimental results have been presented in this section. In Figure 7 the entire converter has been considered as a system/Plant to which two sources are attached. The output of the inverter is PWM controlled and it is controlling the system operation. The block diagram of hardware which has been designed in research lab-III of Kalinga Institute of Industrial Technology deemed to be university (KIIT). Circuit is designed using EAGLE software. They are fed to gate driver circuits. Gate driver circuits have input supply from 230/15 V, 1A step down transformer. Pulses generated from driver circuits have been fed to each MOSFET IRF540 N gate terminals. Output of the power circuit is given to the load RL type RO2. Power supply of MOSFET gate driver circuit 3. Gate drive circuit 4. Main power circuit 5. Output connector from DSPACE. Figure 8 explains the hardware diagram of the proposed converter where input power supplies are through MOSFET gate driver circuits. MOSFET IRF540 Ns are taken as switches. Six MOSFETs work with six gate driver circuits. DSPACE has been connected to output waveforms in order to describe the turn off and on state of the inverter.

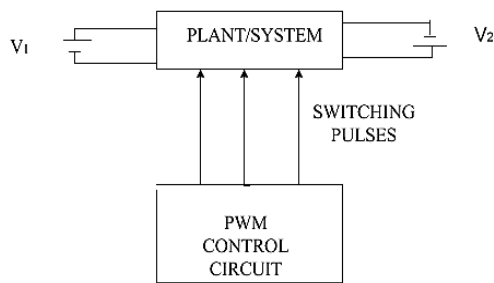


Figure 7. Overall scheme of the system

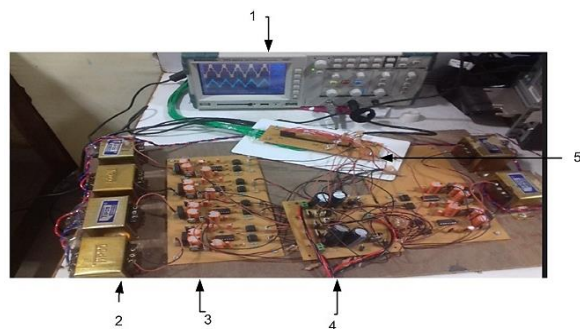


Figure 8. Overall hardware design of the proposed topology

Figures 9 (a) and 9 (b) depict the two input signals of the inverter. V_1 is 10 V and V_2 is 5 V. It shows the asymmetrical configuration of the proposed inverter. Figure 9(c) represents the output signals. It shows output voltage as 14 V and current as 0.125 A respectively with $R=120\ \Omega$, $L=50\ \text{mH}$ at carrier frequency 1 KHz and input capacitors of 470 μF each.

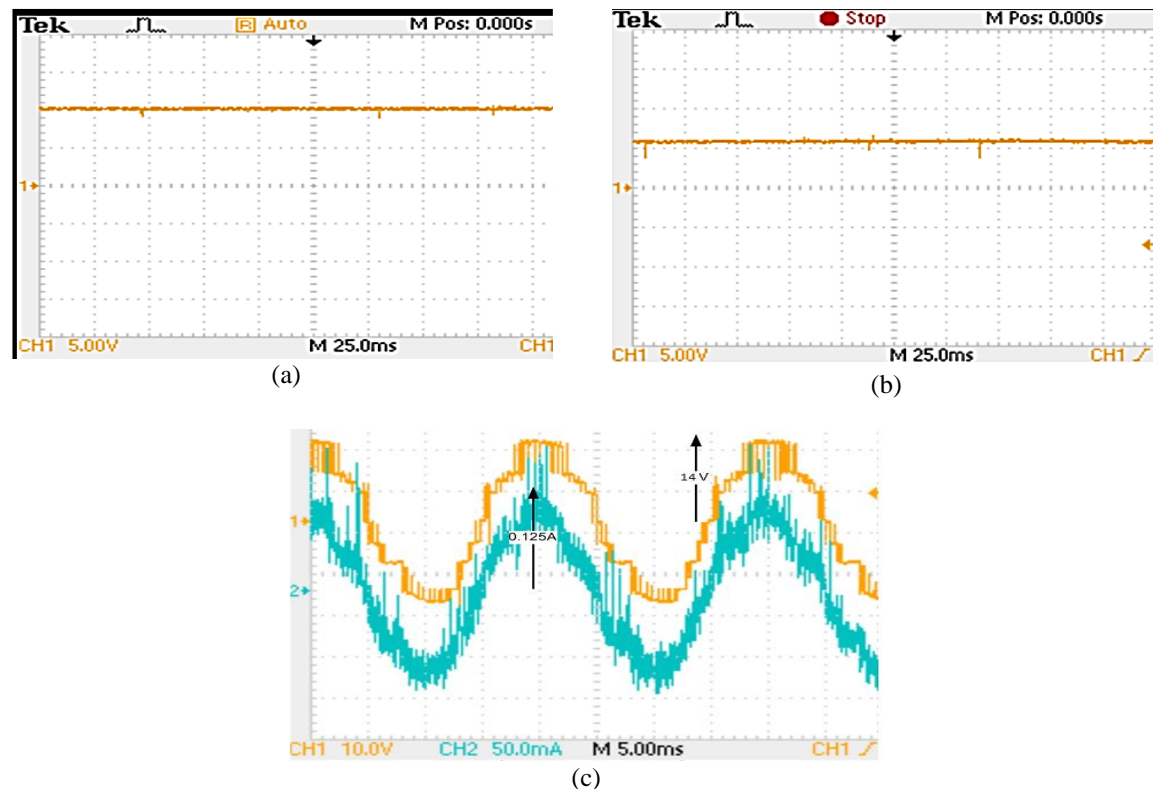


Figure 9. Hardware results for (a) input voltage $V_1=10$ V, (b) input voltage $V_2=5$ V, and (c) peak voltage and current across RL-load

7. CONCLUSION

In this research article, the detailed analysis of the proposed asymmetrical cascaded multi level inverter has been carried out successfully at different modulation index and carrier frequencies. The output waveforms are more sinusoidal and hence better power quality can be obtained at higher carrier frequencies. The proposed topology has been fabricated and verified with its simulation result also. Input voltage of 15 V and output voltage is 14 V which is quite high compared to other existe topologies as cited in the references. Also THDs if the proposed topology are nominal.

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APPENDIX

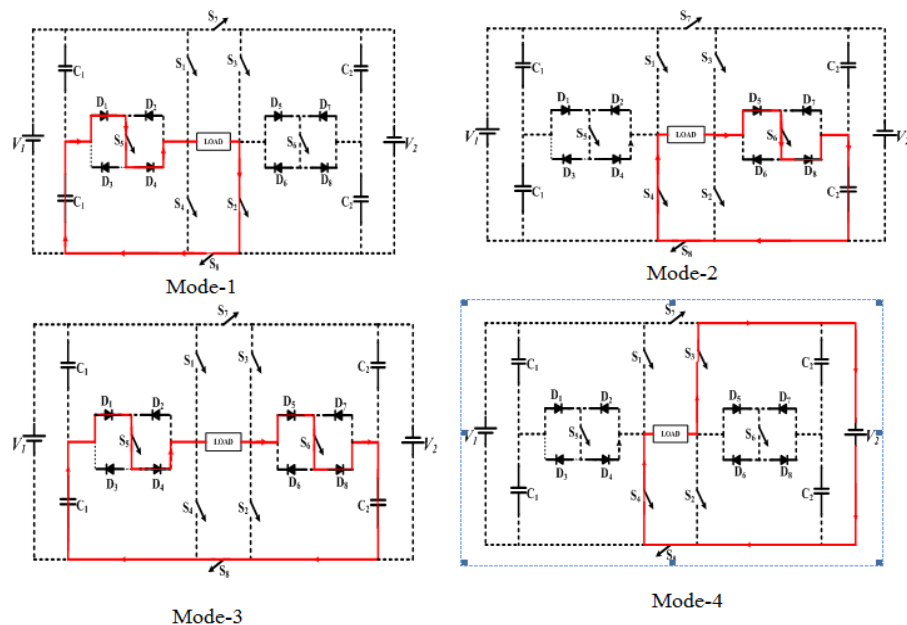


Figure 3. Modes of operation

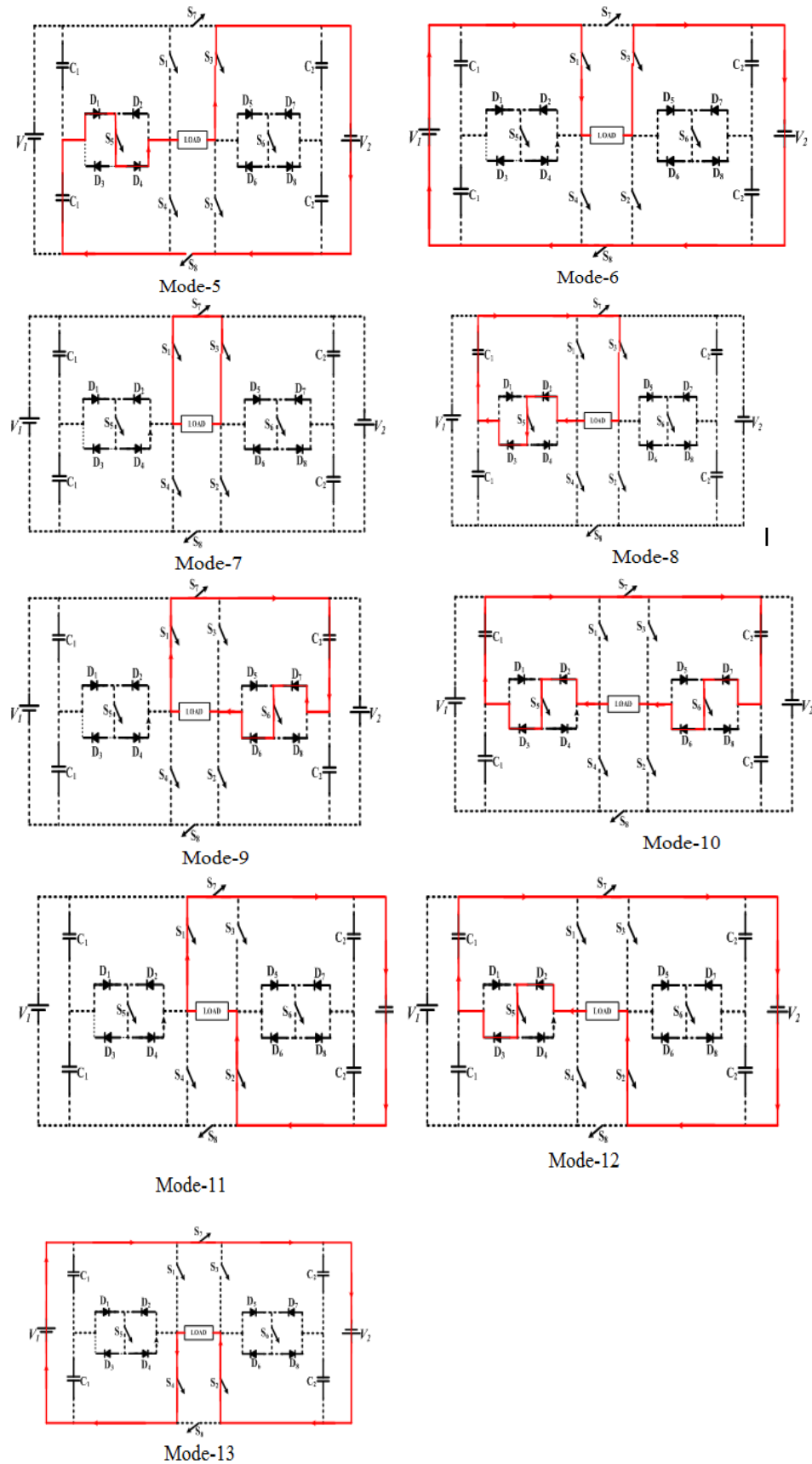










Figure 3. Modes of operation (continue)





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Lipika Nanda     is working as an assistant professor since 2007 in KIIT University. Her broad working area is design of power converters, multi-level inverter and its applications. She is a life member of various professional societies like SESI, ISTE, ISLE, ISCA, and IEEE. She has 3 Australian patents, 2 book chapters. She has published around 20 papers in international journals and conferences. She can be contacted at email: lnandafel@kiit.ac.in.







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