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Asymmetrical four-wire cascaded h-bridge multi-level inverter based shunt active power filter supplied by a photovoltaic source

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ABSTRACT

This paper presents a novel shunt active power filter (SAPF). The power converter that is used in this SAPF is constructed from a four-leg asymmetric multi-level cascaded H-bridge (CHB) inverter that is fed from a photovoltaic source. A three-dimensional space vector modulation (3D-SVPWM) technique is adopted in this work. The multi-level inverter can generate 27-level output with harmonic content is almost zero. In addition to the capability to inject reactive power and mitigating the harmonics, the proposed SAPF has also, the ability to inject real power as it is fed from a PV source. Moreover, it has a fault-tolerant capability that makes the SAPF maintaining its operation under a loss of one leg of the multi-level inverter due to an open-circuit fault without any degradation in the performance. The proposed SAPF is designed and simulated in MATLAB SIMULINK using a single nonlinear load and the results have shown a significant reduction in total harmonics distortion (THD) of the source current under the normal operating condition and post a failure in one phase of the SAPF. Also, similar results are obtained when IEEE 15 bus network is used.

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1. INTRODUCTION

Recently, the research on active power filters (APFs) fed from renewable energy sources has witnessed a significant increase due to the ability of such filters to solve many power quality issues [1]. However, the performance of these filters will be dramatically degraded if a failure in one leg of the inverter is introduced to the SAPFs. Hence, many techniques have been proposed in the literature to enhance the reliability of the inverter and to maintain the performance of the SAPF post a failure. Most of these techniques are based on the use of some kind of redundancies that exist in the 2-level inverters [2]. This redundancy can be inherited in the structure of the 2-level inverter [3] or it is introduced intentionally to the 2-level inverter to make it fault-tolerant [4]. This is done by adding a fourth leg to the conventional 2-level inverter as reported in [5], [6].

Multi-level inverters have many advantages over the 2-level inverters in terms of the low THD in the output, less dv/dt, and higher output voltages. These characteristics have encouraged the researcher to use the multi-level inverters in many applications especially in APFs [7]-[11]. A fault-tolerant multi-level inverter can be achieved through different techniques including neutral-shift, DC-bus voltage reconfiguration, and redundant modules installation is employed [12]-[14]. Various pulse width modulation

(PWM) and control techniques have been reported and discussed in the literature [15]. These techniques aim to control the currents of the inverter that is used in the APFs and to convert the output voltage of the controllers to a digital signal that will be used to gate the inverter. One example of these control techniques is the Hysteresis control. Hysteresis control has many advantages such as it is simple and has a fast dynamic response. But on the other hand, it has a variable switching frequency and produces relatively large current ripples in the system [16]. Another example is the predictive control which has a lower current ripple and constant frequency [16]. Many modulation techniques were proposed to convert the output voltage signals of the control to digital pulses to switch the multi-level inverter such as selective harmonics, multi-level PWM, and multi-level SVPWM [17]. Among these modulation techniques, SVPWM can be considered as an ideal solution to be used in APFs. This is related to the ability to implement it in 3 and 4-wire systems. In addition to its ability to reduce the switching losses, minimize the capacitor balancing problem, and reduce the total harmonic content in the output [18]. In a 3-wire system, 2D-SVPWM can be used [19] while 3D-SVPWM is used in a 4-wire system to control the neutral current [20].

In this paper, a SAPF using the 3-phase 4-wire (leg) asymmetric CHB 27-level inverter system is implemented with the 3D-SVM algorithm. The 3-phase 4-leg multi-level inverter is powered from a PV system to have better reliability and control. The SAPF can maintain the operation pre and post a non-healthy operating condition for both the load such as asymmetry and the SAPF such as the failure in one leg of the SAPF.

2. RESEARCH METHOD

2.1. Shunt active filter

The structure of the SAPF that is proposed in this paper is shown in Figure 1. The SAPF is consisting of the CHB inverter. The multi-level inverter has an extra leg that is connected permanently to the neutral of the load or the power system. Moreover, it is supplied from batteries that are fed from photovoltaic arrays. P&O maximum power point (MPPT) technique is used to get maximum possible power from the solar energy [21]. The controller is using 3D-SVPWM to generate the pulses that trigger the multi-level inverter. A brief view in each part of the SAPF is introduced:

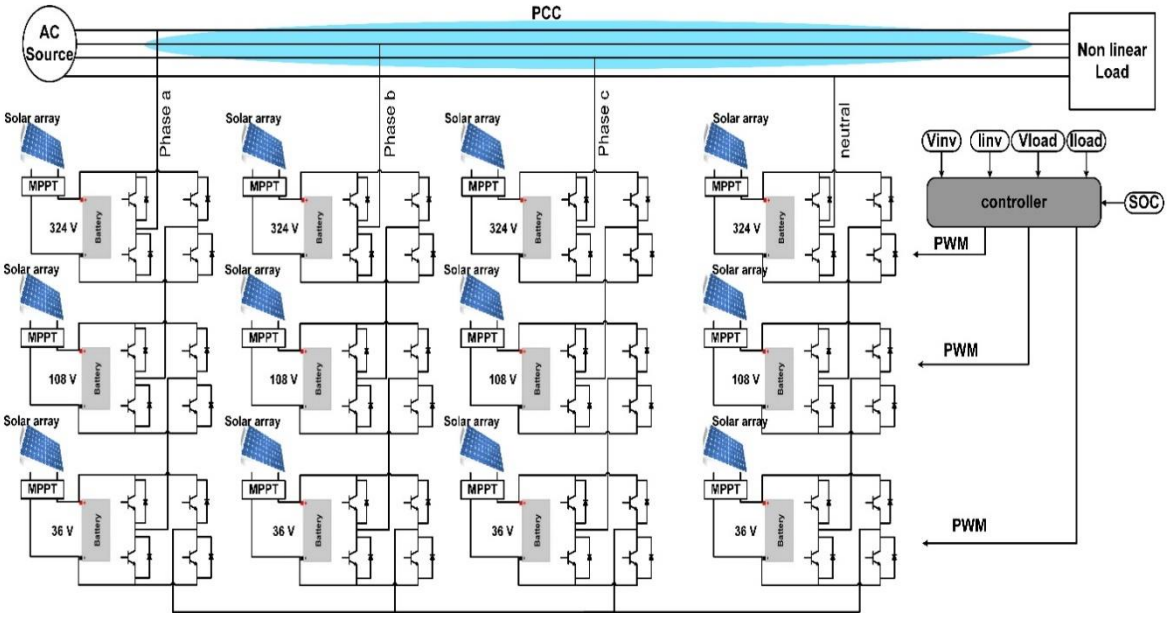

Figure 1. the structure of the proposed SAPF

2.1.1. Fault-tolerant 27-level inverter

Each leg of the multi-level inverter is composed of three H-Bridges connected in series. Each H-Bridge is fed from seperate battery. The voltage levels of the three batteries in each leg will be 36 V, 108 V, and 324 V which means that the ratio is 1:3:9 [14], [22]. This ratio makes it is possible to connect the SAPF to the PCC directly without the need for any transformer. Moreover, it makes the multi-level inverter

generates the maximum number of levels (27-level) while using only three H-Bridges per leg. This is quite important to minimize the harmonic content of the output voltage of the multi-level inverter and produce a sinusoidal output which helps to eliminate the need for any kind of filtering at the output of the multi-level inverter. The output of each H-Bridge and the output of one leg of the 27-level inverter are shown in Figure 2. The H-Bridge that is interfaced to the 324 V battery will generate 69% of the total power generated by the multi-level inverter. Also, The H-bridge that is connected to the 108 V battery will be responsible for generating about 23.1% of the total power while the H-Bridge interfaced with the 36 V battery will generate about 7.7 % of the total power. the switching frequency of each bridge varies from 50 Hz which is the switching frequency of the H-Bridge interfaced with the 324V battery to reach 5 kHz which is the frequency of the H-Bridge connected to the 36 V battery and the switching frequency of the multi-level inverter too. This low switching frequency especially for the high power H-Bridges helps to enhance the efficiency of the multi-level inverter by reducing the switching losses.

In addition to the previously mentioned features of the proposed multi-level inverter, it has another important feature which is the fourth leg connected to the neutral of the electrical system. The use of the added leg besides using 3D-SVPWM will enable the SAPF to work under unhealthy operating conditions such as load asymmetry and a failure on one leg of the SAPF due to the open-circuit fault. This will help in enhancing the reliability of the SAPF and maintains its performance post a failure in one leg of the multi-level inverter.

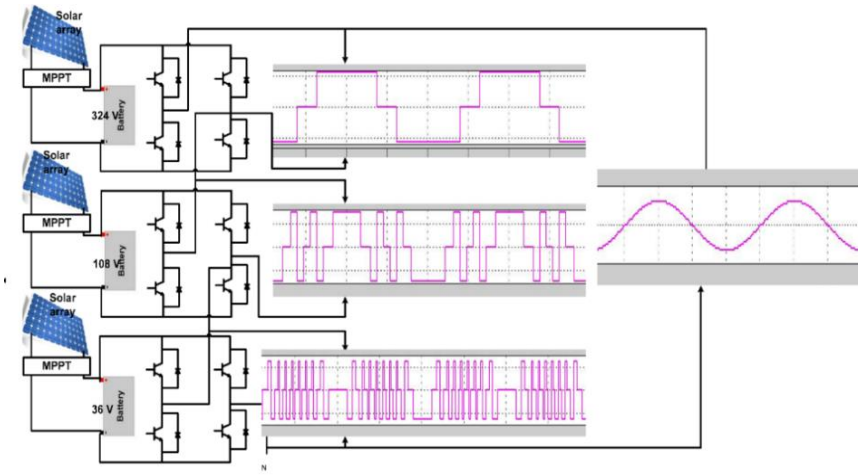

Figure 2. output voltage waveforms of the 27- level 4-leg inverter

2.1.2. PV system design

A 125 W polycrystalline PV modules (BP 3125S photovoltaic module) were used to design all PV arrays. The specifications of these modules are given in Table 1.

Table 1. Specification of BP 3125S photovoltaic module

Maximum power	125 watt
Maximum power voltage	17.6 V
Maximum power current	7.1 A
Open circuit voltage	22.1 V
Short circuit current	7.54 A

According to the load current of the grid, a 30Kwp, 48.3 A, 400 V, and 50 Hz PV source is needed, the design of the PV system will be as:

$$\text{No. pv} = \frac{\text{Ppv}}{\text{Pmpp}} = \frac{30000}{125} = 244 \text{ module} \quad (1)$$

The number of modules connected in series Ns can be obtained as:

$$\text{Ns} = \frac{\text{needed voltage}}{\text{Vmpp for module}} = \frac{300}{17.6} \approx 17 \quad (2)$$

The number of strings connected in parallel can be calculated as:

$$\text{Number of strings} = \frac{\text{total power}}{\text{string power}} = \frac{30000}{17*125} \approx 14 \quad (3)$$

The Boost converter should receive DC voltage from PV which varies between 0 to 299 volts and fixed the output voltage to 324 V (DC). The specifications of the boost converter are given in Table 2.

Table 2. Specification of the boost converter

Specification	Detail
Input voltage	0-299
Output voltage	324

2.1.3. 3D–SVPWM

The proposed 3D-SVPWM technique that is adopted in this work is presented in [20]. This technique is very simple and based on geometrical consideration. Moreover, it is independent of the number of levels of the multi-level inverter. And more importantly, can be used under healthy conditions such as load asymmetry and failure in one phase of the SAPF without modifications. The reference voltage will be pointing to a sub-cube. This sub–cube can be identified using the components (a, b, c) which are the integer values of the reference voltage (V_ref). This cube can be decomposed into six tetrahedrons. These tetrahedrons and the associated PWM waveforms are shown in Figure 3.

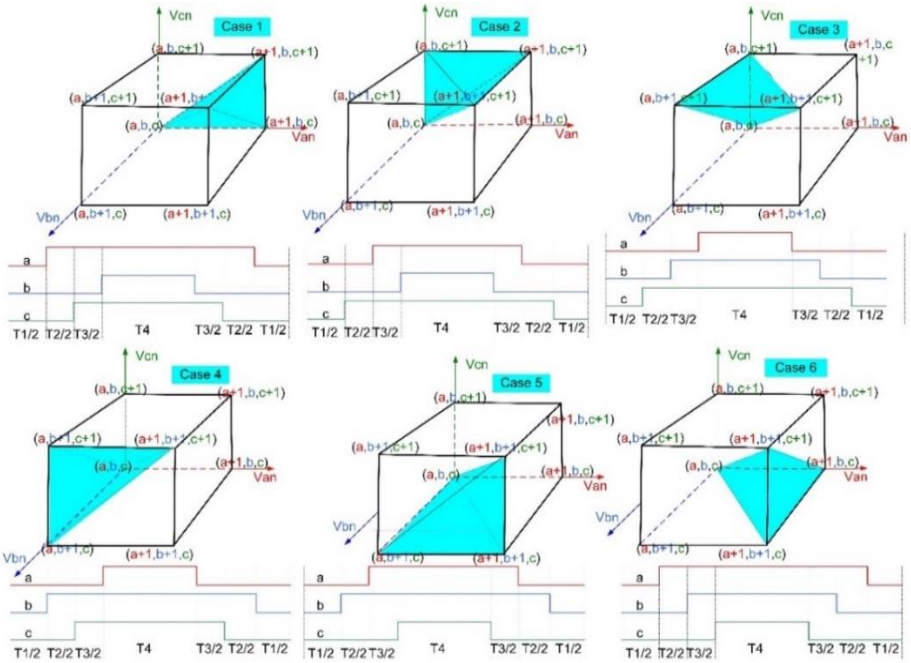

Figure 3. Switching sequence and timing diagram of type 3 used in SVPWM for the multi-level converter

2.2. Control structure of the SAPF

The performance of the SAPF especially in the harmonics mitigation process depends on the harmonic extraction method. Many techniques were proposed in the literature to extract the harmonic signal. These techniques can be divided into two categories. The first one works in the frequency domain [21] while the second one is base on the time domain [23]. In the frequency domain techniques, a transformation from the time domain to frequency domain using fast fourier transform (FFT) is needed while in the time-domain technique, an instantaneous estimation is done without the need for any frequency transformation. The time-

domain method is simpler and needs less calculation compared to the frequency domain so the result will be faster [23].

2.2.1. Harmonic extraction using d-q method

d-q Harmonic extraction method was adopted in this research to calculate the current reference for the SAPF filter [24], [25]. The illustration of the principle of operation of this technique is shown in Figure 4. The voltages (Vabc) and the currents (IL abc) of the non-linear loads are measured firstly. Then, the load currents (IL abc) are transformed to a synchronous frame oriented to voltages of the nonlinear load (VL abc). This step is achieved with the help of the phase locked loop (PLL). The currents of the nonlinear loads (IL abc) become IdL, and IqL at this stage. The d-component of the current of the nonlinear load will be in the direction of the voltage of the nonlinear load (VL abc) and so it will present the real power of the nonlinear load while the q-component of the current of the nonlinear load will be perpendicular to the voltage of the nonlinear load (VL abc) and so it will present the reactive power of the nonlinear load. Due to the presence of the harmonics in the nonlinear load currents (IL abc), then, the nonlinear load power component (IdL) and reactive power component (IqL) that is obtained from the transformation to the synchronous frame will have components as shown in equations (4-5).

$$IdL=\widetilde{IdL}+\overline{IdL} \quad (4)$$

$$IqL=\widetilde{iqL}+\overline{IqL} \quad (5)$$

The DC components ($\overline{idL}, \overline{iqL}$) represent the fundamental component of the non-linear load real and reactive power. While the oscillating components ($\widetilde{idL}, \widetilde{iqL}$) represent the harmonics in the non-linear load currents. The d-q components of the currents of the nonlinear load will be processed further to obtain the reference signals idL _ref and iqL _ref according to the task of the SAPF as follows:

- If the SAPF is wanted to mitigate harmonics only, then the DC components ($\overline{idL}, \overline{iqL}$) are filtered out using s high pass filter.
- If the SAPF is wanted to mitigate harmonics and inject reactive power, then the DC component ($\overline{idL}$) is filtered out using a high pass filter.
- If the SAPF is wanted to mitigate harmonics, inject reactive power, and inject real power, then the DC component ($\overline{idL}$) is filtered out using a high pass filter and then an offset DC value is added to idL_ref.

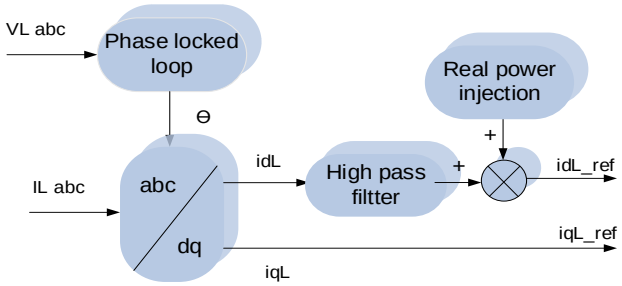

Figure 4. d-q harmonic extraction technique

2.2.2. Modelling and controlling the SAPF

Assuming that the SAPF is connected to the PCC through cable that has a small resistance and inductance as shown in Figure 5. The (6)-(8) hold true:

$$van_{inv} = ia_{inv} * r + L\frac{dia_{inv}}{dt} + van_{pcc} \quad (6)$$

$$vbn_{inv} = ib_{inv} * r + L\frac{dib_{inv}}{dt} + vbn_{pcc} \quad (7)$$

$$vcn_{inv} = ic_{inv} * r + L\frac{dic_{inv}}{dt} + vcn_{pcc} \quad (8)$$

The (6)(8) are transformed into the load voltage-oriented frame (d-q-0) frame as:

$$L\frac{did_{inv}}{dt} = -id_{inv} * R + \left(Vd_{inv} - Vd_{pcc}\right) - \omega * L * iq_{inv} \quad (9)$$

$$L\frac{diq_{inv}}{dt} = -iq_{inv} * R + \left(Vq_{inv} - Vq_{pcc}\right) + \omega * L * id_{inv} \quad (10)$$

$$L\frac{dio}{dt} = -io * R + +\text{Vo} \quad (11)$$

The (9)-(11) can be rewritten as:

$$vd = id_{inv} * R + L\frac{did_{inv}}{dt} \quad (12)$$

$$vq = iq_{inv} * R + L\frac{diq_{inv}}{dt} \quad (13)$$

$$vo = io_{inv} * R + L\frac{dio_{inv}}{dt} \quad (14)$$

where

$$vd = \left(Vd_{inv} - Vd_{pcc}\right) - \omega * L * iq_{inv} \quad (15)$$

$$vq = \left(Vq_{inv} - Vq_{pcc}\right) + \omega * L * id_{inv} \quad (16)$$

Figure 6 shows the closed-loop through which the controllers can be designed. In this work three proportional-integral (PI) controllers are designed to regulated the currents of the multi-level inverter ($idq0_{inv}$) to make the SAPF capable of mitigating harmonics, injecting reactive power, and injecting real power-based on the reference currents (idq0L_ref.) obtained from the dq-harmonic extraction technique. The outputs of the controllers (Vdq0_ref) are then transformed to digital pulses using 3D-SVPWM technique as illustrated in Figure 7.

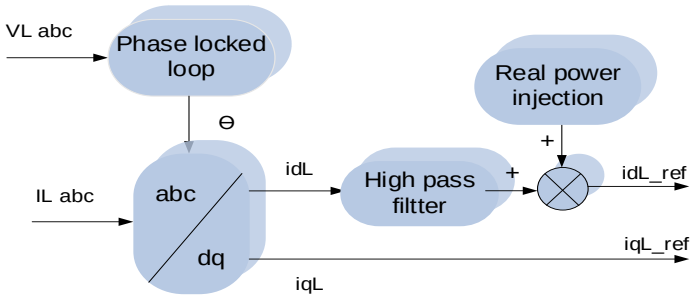

Figure 5. Dynamic modelling of the shunt active filter

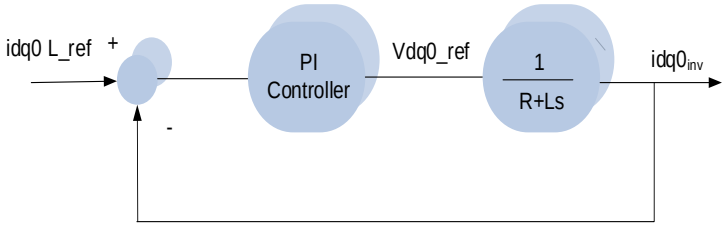

Figure 6. SAPF controller design

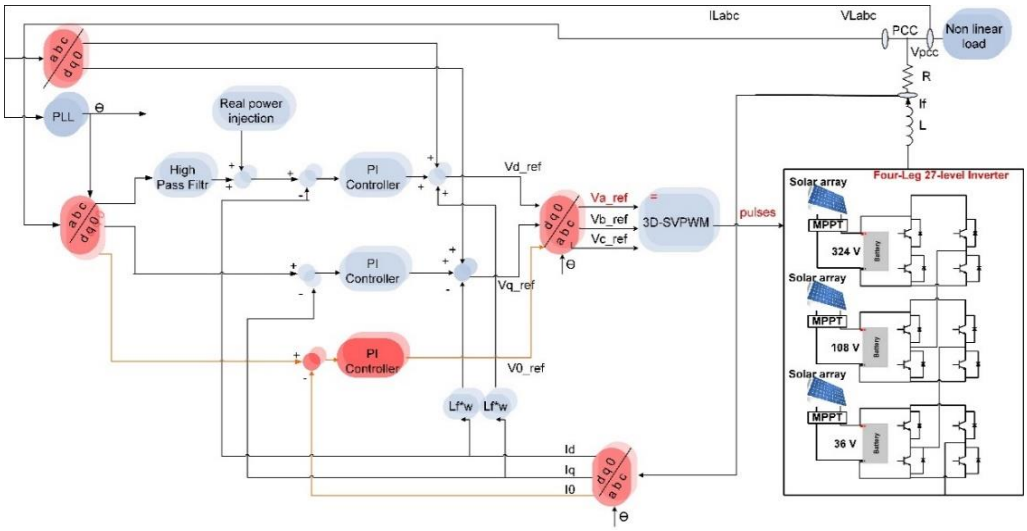

Figure 7. The control structure of active filter

3. RESULTS AND DISCUSSION

The proposed SAPF is simulated in MATLAB/Simulink environment to check its performance and reliability. Many scenarios have been considered as:

- The first scenario was about testing the performance of the proposed SAPF when the load is a single nonlinear load.
- The second scenario was about investigating the functionality of the proposed SAPF on the IEEE fifteen bus system where the load at bus 5 was made nonlinear. In this case, the SAPF was put near the source (i.e the harmonics inside the network are out of scope).
- The third scenario was about investigating the effect of the SAPF on the loesses and harmonics of the whole IEEE fifteen bus system when the SAPF was put near to the bus that has the nonlinear load (bus 5).

3.1. Fist scenario

The structure of the whole electrical system during this test is shown in Figure 8. There are two objectives of this test:

- The first objective is to check the ability of the SAPF to inject the reactive power, real power, and to mitigate the harmonics
- The second objective is to check the fault-tolerant capability of the SAPF in the case of a loss of one
- phase during operation

The results obtained from the above test under healthy operating conditions and in the cases of an open circuit in phase ‘c’ of the SAPF are given in Figure 9 and Figure 10 respectively. Figure 9 demonstrates the effectiveness of the system in mitigating the harmonics, injecting reactive power, and injecting real power under healthy operating conditions. The SAPF was disabled till t= 0.2s. after that, at t=0.2s, the SAPF was commanded to mitigate the harmonics only. It can be noticed that the source currents became almost pure sinusoidal as the Total Harmonic Distortion was reduced from 20.86% before the use of the SAPF to 2.43% after using it. Then at t= 0.4s, the APF was commanded to inject reactive power in addition to the mitigating of the harmonics. The results of reactive power measurements of the source in Figure 9 show that the APF was responded to this command properly. It can be noticed from the results that the reactive power that comes from the source at this time became zero which means that all the reactive power needed by the load no was generated from the SAPF and the p.f at the source became 1. Finally, at t=0.6s, a command was sent to the SAPF to inject a real power in addition to the mitigating of the harmonics, and the injection of the reactive power. The results show that the SAPF at that time started to inject real power. The evidence of that can be obtained from two things: the first one is the reduction of the source current which means that part of the real power consumed by the load was generated by the SAPF. The second one is the reduction of the measurements of the source real power due to the same reason mentioned previously.

Figure 10 demonstrates the enhancement of the reliability of the SAPF obtained by adding a fourth leg connected permanently to the neural and using a 3D-VPWM technique. Before t= 0.8s, the SAPF was running under healthy operating conditions. Also, it was used to inject real and reactive power in addition to mitigating the harmonics. After that, at t=0.8s, an open-circuit fault on phase ‘c’ was introduced to the SAPF without enabling the fourth leg. It can be noticed from the results that the SAPF was no longer able to

mitigate harmonics in the failure leg. At t, 1s the fourth leg was enabled and the SAPF returned to work as before the failure and could maintain the system performance.

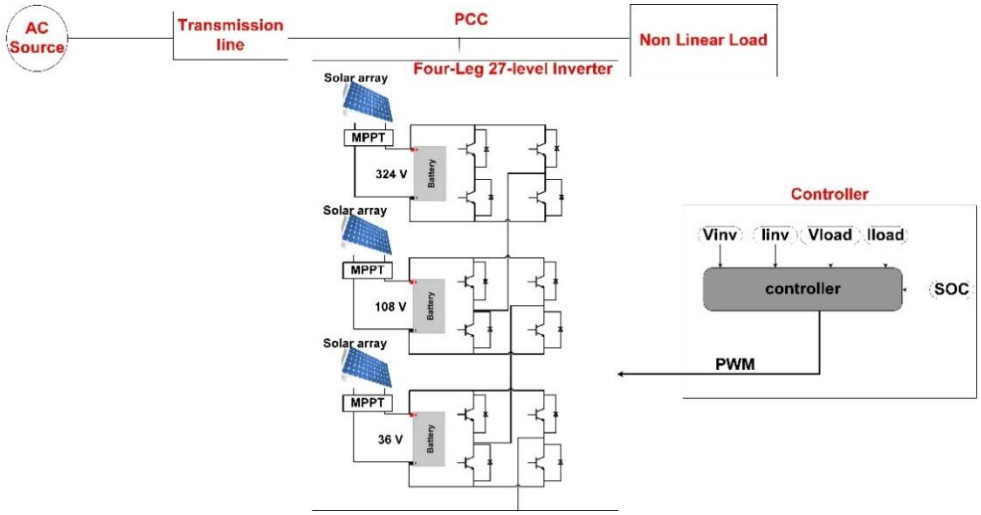

Figure 8. Four-leg 27-level inverter APF supplying nonlinear load

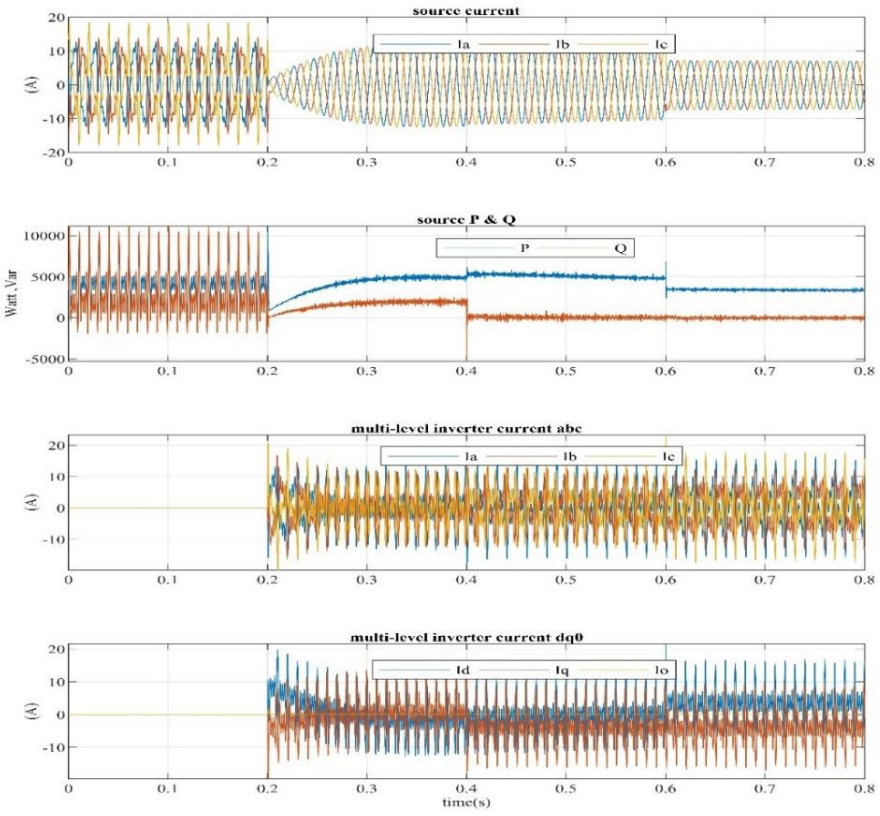

Figure 9. Results of the APF with single nonlinear load under healthy operating condition

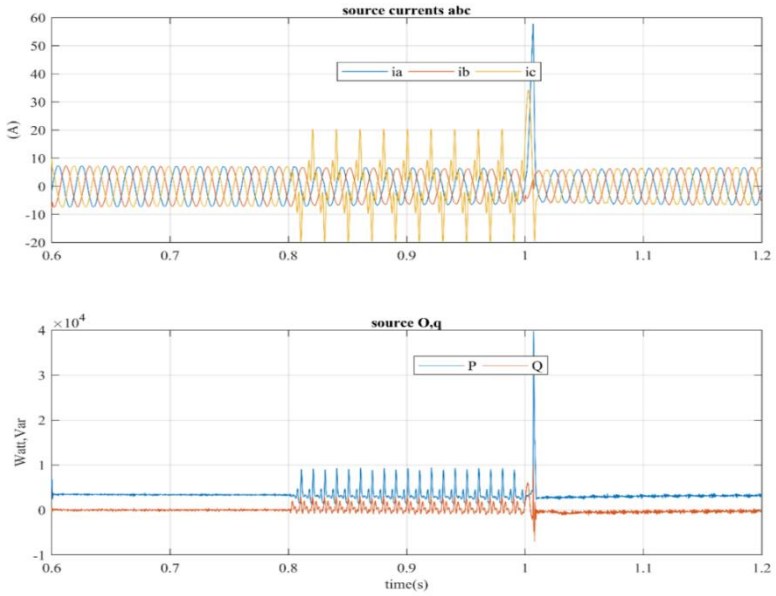

Figure 10. Results of the APF with single nonlinear load under a failure in phase 'c'

3.2. Second scenario

In this test, the IEEE 15 bus network was utilized with the nominal voltage of 400 V as shown in Figure 11. The load at the bus no 5 was made nonlinear. The SAPF was connected to bus no 1 and the whole network is treated as a single load. The current waveform of the source currents at Bus no 1 was measured and the THD was calculated as shown in Figure 12. The current waveforms in addition to the Fast Fourier Transform (FFT) show a significant reduction in the harmonic content of the source currents which became near sinusoidal. The above-mentioned results also were confirmed from the calculated values of the THD of the source currents. The THD was reduced from 13% before using the SAPF to 4.5% after using it.

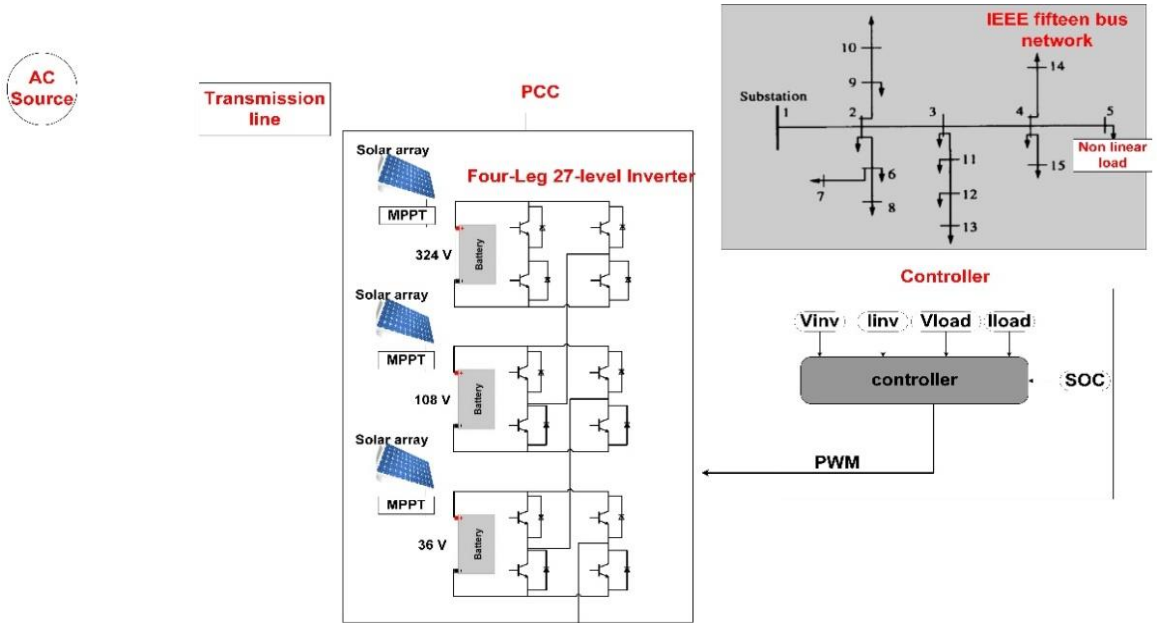

Figure 11. SAPF connected to bus no 1 of the IEEE 15 bus network

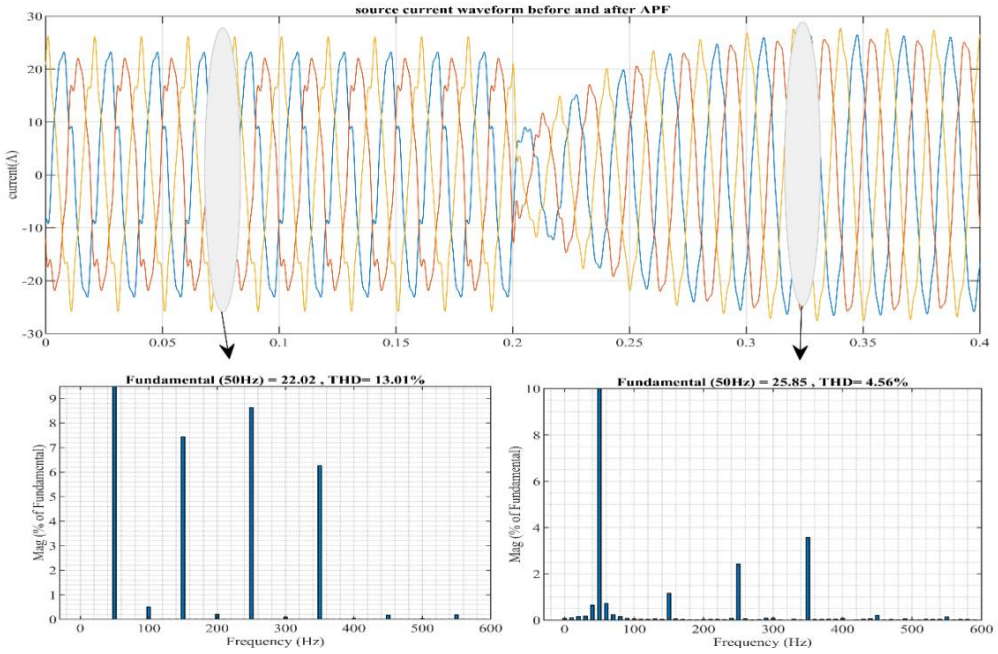

Figure 12. Source current when APF connected to bus no 1 of the IEEE 15 bus network

To investigate the effect of the SAPF on the THD in the whole network in this case, the currents waveforms were measured at buses 7,9,11, and 15. The results are given in Figure 13. Figure 13 shows that there is a slight improvement in the current waveforms at these buses which means that the total harmonic distortion inside the network is still high. Figure 14 shows the calculation of the THD at these buses before and after using the SAPF. The results confirm that the SAPF at this place is inefficient in reducing the THD in the network since it is far away from the place of the nonlinear load at bus 5.

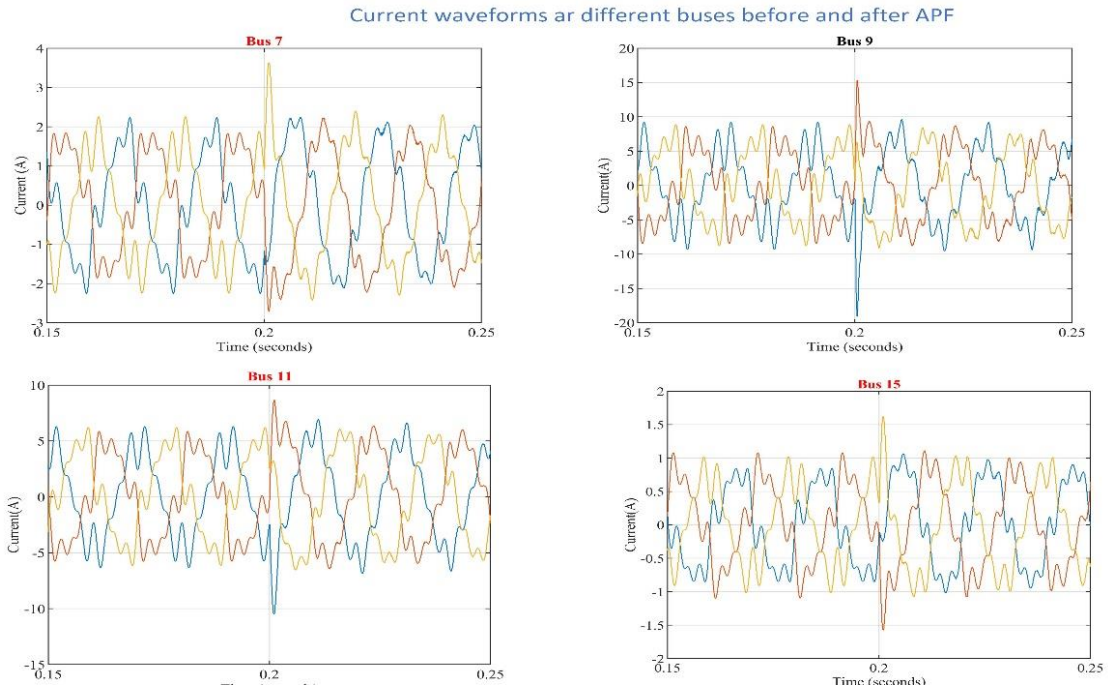

Figure 13. Currents waveforms at buses 7, 9, 11, 15 when APF connected to bus no 1

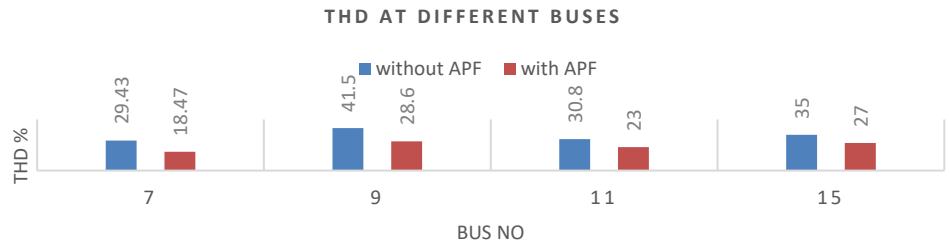

Figure 14. Currents waveforms at buses 7,9,11,15 when APF connected to bus no 1

3.3. Third Scenario

The results obtained from the previous scenario (i.e connecting the SAPF at bus no 1 and far from the nonlinear load) shows an improvement in the THD of the source currents but the currents in the network still distorted and the THD of these currents is still high which will cause many power quality issues to the network. In this scenario, the SAPF was connected at bus no 5 near the nonlinear load as shown in Figure 15.

The current waveform of the source currents at Bus no 1 was measured and the THD was calculated as shown in Figure 16. The current waveforms in addition to the fast fourier transform (FFT) show a significant reduction in the harmonic content of the source currents which became near sinusoidal. The above-mentioned results were also confirmed from the calculated values of the THD of the source currents. The THD was reduced from 13% before using the SAPF to 2.79 % after using it. These results of the source current are even better than the results obtained by connecting the SAPF at bus 1.

To investigate the effect of the APF on the THD in the whole network in this case, the currents waveforms were measured again at buses 7,9,11, and 15. The results are given in Figure 17. Figure 17 shows that there is a significant improvement in the current waveforms at these buses which means that the total harmonic distortion inside the network is very low. Figure 18 shows the calculation of the THD at these buses before and after using the SAPF. The results confirm that the SAPF at this place is efficient in reducing the THD in the network since it is near the place of the nonlinear load at bus 5.

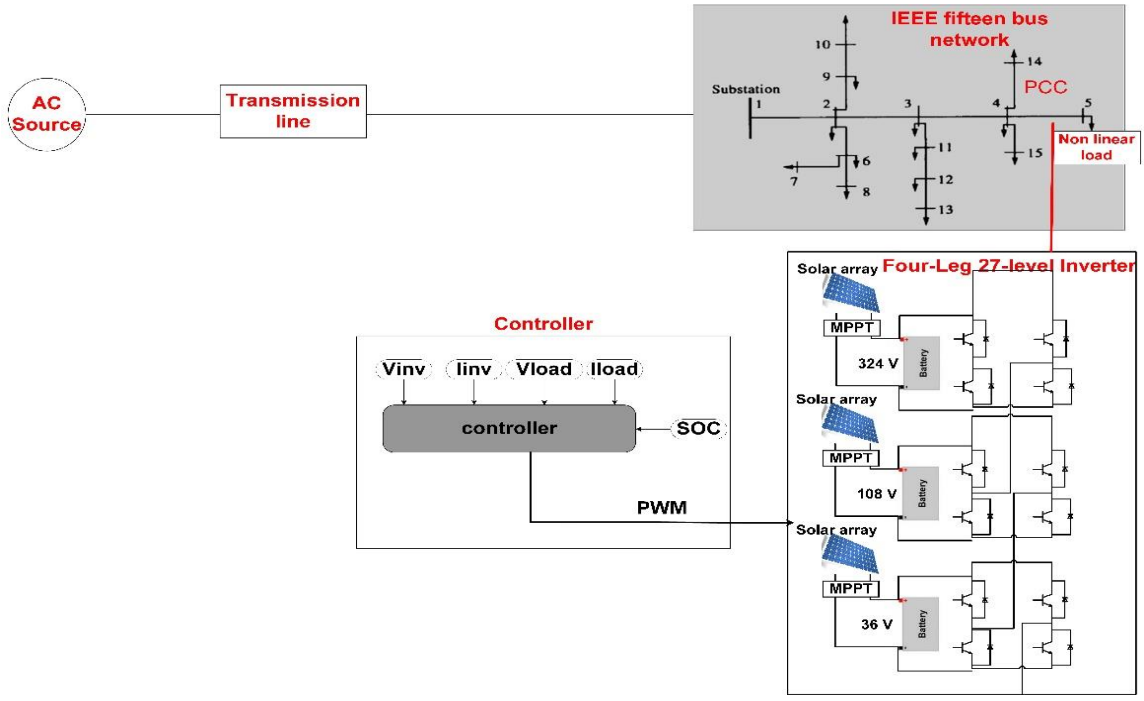

Figure 15. SAPF connected to bus no 5 of the IEEE 15 bus network

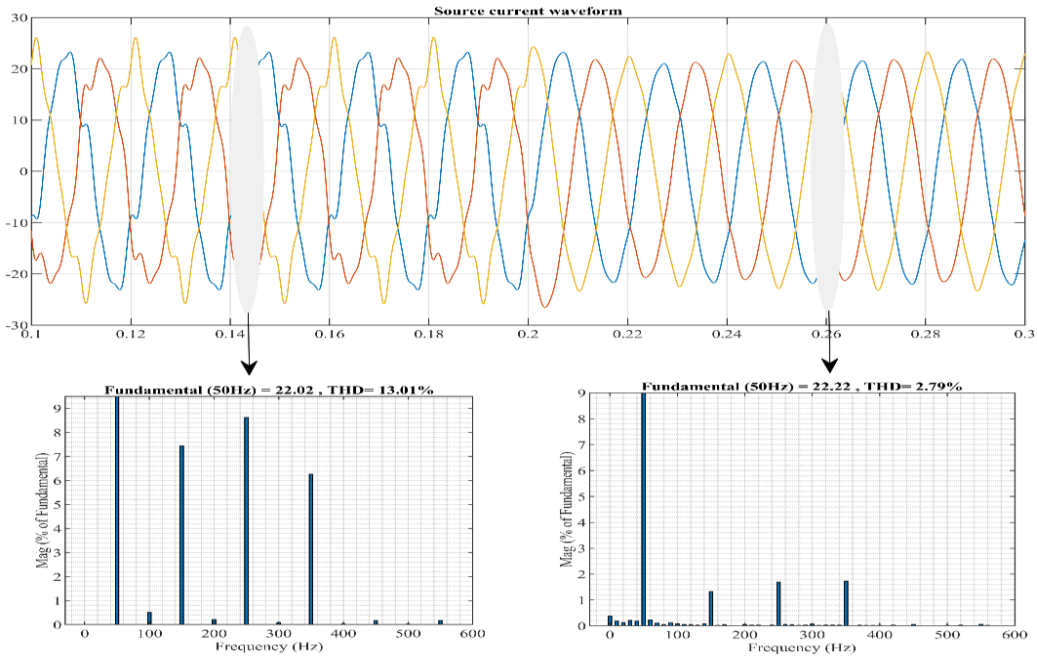

Figure 16 source current when APF connected to bus no 5 of the IEEE 15 bus network

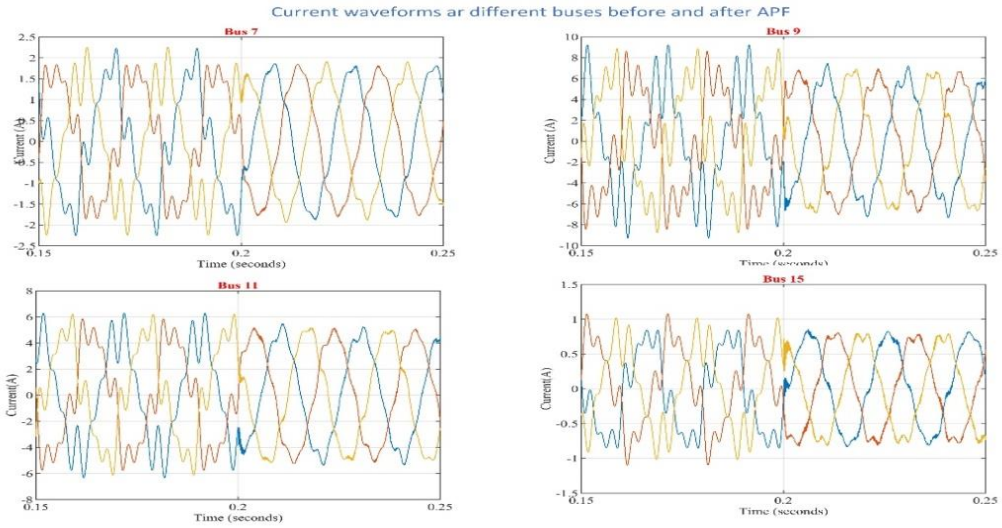

Figure 17. Currents waveforms at buses 7,9,11,15 when APF connected to bus no 5

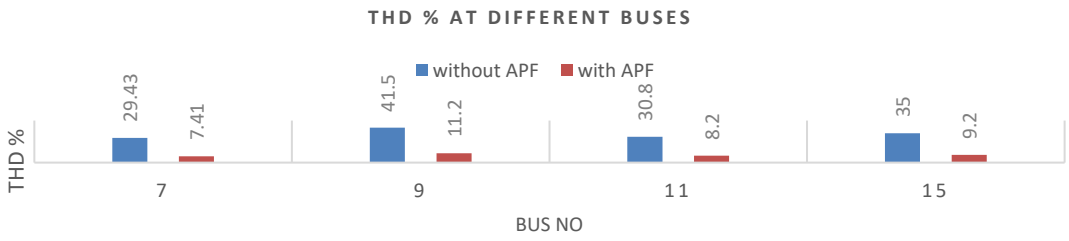

Figure 18. Currents waveforms at buses 7,9,11,15 when APF connected to bus no 5

4. CONCLUSION

This paper has presented a four-leg 27-level SAPF that can maintain operation in the cases of asymmetric nonlinear loads and even in the case of a loss in one phase of the APF due to the open circuit fault. This enhancement in the reliability of the APF is achieved through two things; the first one is the addition of the fourth leg to the multi-level inverter which is connected to the neutral permanently. The second one is the use of the 3D-SVPWM technique instead of the 2D-SVPWM. The proposed SAPF can do many tasks under healthy operating conditions and post and open circuit fault. It can mitigate harmonics in the power system, improve power factor in the system by injecting reactive power, and inject real power to the system. The proposed SAPF can be used if the load just a single nonlinear load and if the load is a complete power system network. In the case that the network is a power system network, the best place of the SAPF is near the load to improve the whole network.

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