Optimization of passive filter components through active filtering of current ripple reduction in an inverter

Jeyaraman Ramakrishnan¹, Chengalvarayan Natarajan Ravi²

¹Department of Electrical and Electronics Engineering, Sathyabama Institute of Science and Technology, Chennai, India ²Department of Electrical and Electronics Engineering, Vidya Jothi Institute of Technology, Hyderabad, India

Article Info ABSTRACT Article history: This paper employs the active input current filtering concept developed and

Received Aug 2, 2021 Revised Jan 21, 2022 Accepted Jan 28, 2022

Keywords:

Direct current-direct current converter Passive filter Push-pull converter Ripple reduction Second-order ripple Two-stage inverter This paper employs the active input current filtering concept developed and explained to optimize the conventional passive filter components in a twostage telecommunication inverter. A prototype inverter has been designed for a rated power of 800 W. Optimization of the passive filter components consisting of inductance inductors tank (LTank) and capacitance capacitors tank (CTank) was performed through simulations. The simulation model used for this optimization was validated using the developed prototype. The focus of this work is to limit the input direct current (DC) current ripple within the limits specified in European Telecommunication inverter and optimize the passive filter components. Using the active filtering technique, limit the input current ripple and simultaneously reducing the filter capacity in DC-link. This advantage of active filtering technology over the conventional passive inductors and capacitors (LC) filter concept is explored and demonstrated in this paper.

This is an open access article under the <u>CC BY-SA</u> license.



Corresponding Author:

Jeyaraman Ramakrishnan

Department of Electrical and Electronics Engineering, Sathyabama Institute of Science and Technology SH 49A, Semmancheri, Chennai, Tamil Nadu 600119, India Email: jeyam.apk@gmail.com

1. INTRODUCTION

In most telecommunication and industrial applications, the inverter is mainly used for power backup. The single-phase two-stage inverter is widely used in telecommunication and data center applications for critical backup solutions. This inverter contains a direct current-direct current (DC-DC) converter stage and a direct current-alternating current (DC-AC) inverter stage. The battery DC supply is boosted to a high voltage by using a DC-DC converter and this stores in the DC link capacitors [1]. Then this high voltage is converted to an AC supply by using a DC-AC converter. The battery power is consumed as a sinusoidal form of power and it causes a second-order current ripple in the battery. The product of the V and I is equal to the power, which is in a sine pattern. Hence, this inverter intermediate stage DC link current has a second-order sinusoidal ripple. It is also reflected in the DC input battery side. The DC input current has an AC ripple signature and it resembles the AC output power of the inverter supply. The DC input has flat DC and AC components of current. The battery is an electrochemical device. This AC ripple current reduces the performance of the battery's backup time [2]-[5]. In the study of battery AC ripple frequency, the battery manufacturers typically specify that the acceptable ripple current percentage is less than 10% and the highfrequency ripple creates a significantly less effect in the battery chemical reaction and low-frequency ripples are creating an overheating issue in the battery and reduce the inverter efficiency [6]–[9]. This affects the overall life span of the telecommunication battery power system. The telecommunication system operates with a -48 V DC supply. It is mainly derived from the battery bank and some equipment operates with an AC supply. In this application, the industrial telecom inverter is employed. The inverter takes DC power from the battery bank and in this case, the inverter injects a second-order noise into the telecommunication equipment. These frequencies create a humming noise in telecommunication networks. The telecommunication European Telecommunications Standards Institute (ETSI) standard specifies the psophometric low-frequency spectrum range and limits. It should be satisfied by all telecommunication equipment. To meet the psophometric noise emission limits, the inverter DC input current ripple percentage should be less than the 3% level [10]. This paper primary focus is on determining the root cause of the second-order ripple generation phenomenon in an inverter and optimizing inductors and capacitors (LC) filter components using passive and active approaches ripple reduction techniques [11]. The amount of DC ripple current can be reduced by increasing the LC filter value in the DC link LC filter or by implementing the ripple reduction technique in the DC-DC converter. The passive method enhances the LC filter used in the DC-DC converter intermediate section DC-link output. It needs a bigger value of inductance and capacitance to archive less than 3% acceptance level and also it needs more room space to accommodate the filter. In the active method, the dual feedback and proportional integral (PI) closed-loop control techniques help to reduce DC ripples [12]-[14]. This paper explains about LC filter method and a very commonly used active filter method and optimizing the LC filter size in comparison with the passive method. In the simulation and experiment, both methods are implemented and the characteristics of ripple and percentage of the DC input ripples are compared.

2. TOPOLOGY

The passive and active DC input current ripple reduction method has been experimented with on a two-stage inverter. The DC-DC converter is a push-pull topology and the DC-AC inverter is a full-bridge topology. The model circuit of the telecommunication inverter is depicted in Figure 1.



Figure 1. The basic circuit of the telecommunication inverter

The DC input current ripple can be reduced using the LC filters. There are two types of LC filters used in this inverter they are DC-link Ltank and Ctank LC filter and Lload and Cload LC filter. The Lload and Cload LC filter is mainly used to filter the AC output of the full-bridge inverter sinusoidal pulse width modulation (PWM) spectrum. The L_{tank} and C_{tank} LC filters employ the DC input ripple reduction. In the active method, the input ripple current shall be reduced by controlling the PWM of the DC-DC converter. Both ripple reduction methods are implemented in a push-pull DC-DC converter and results are analysed [15]-[17]. The push-pull converter has two switches metal-oxide-semiconductor field-effect transistor (MOSFETs) Q1 and Q2 and at a time one switch is ON and the second switch is OFF and vice versa. The complementary PWM signals are given to the metal-oxide-semiconductor (MOS) Q1, Q2, and it operates with a maximum of less than 0.5 duty cycle. The push-pull converter operates with a switching frequency of 50 kHz. The transformer provides galvanic isolation between high voltage circuits and low voltage circuits. The 48 V battery voltage is step up to a 385 V DC by using this transformer. The transformer pulsated secondary voltage is rectified by using rectifiers D1, D2, D3, and D4. The high-frequency switching diodes are used. This rectified DC link voltage ripple is filtered by the inductor L_{tank} and capacitor C_{tank}. The DC link voltage is stored in the buffer capacitor C_{tank}. This DC link voltage is converted to an AC supply with full-bridge insulated gate bipolar transistors (IGBTs) by using sinusoidal PWM techniques. In (1) shows the push-pull converter voltage gain function.

$$V tank = \left(\frac{Ns}{Np}\right) V in x d \tag{1}$$

Where, Vtank – DC link voltage, Vin – Dc input voltage from Battery, Np – Push pull transformer Primary Turns, Ns – Pushpull transformer Secondary turns, d – PWM Duty cycle

3. ROOT CAUSE ANALYSIS OF THE RIPPLE GENERATION AND RIPPLE REDUCTION METHODS

This sinusoidal waveform, which has a distinct fundamental frequency signature, powers the entire power system. The power can be stored in the form of DC in a battery and converted to AC as needed to power the critical backup loads. When the flat DC battery power is sliced and boosted to higher DC link voltage by DC-DC converter and then it is again converted similar to an alternator output sine signature waveform [18]–[20]. The source of the ripple waveform characteristics is theoretically analyzed and depicted in Figure 2. In (4) and this product are in a sine pattern and have a frequency of double times of the fundamental AC frequency.



Figure 2. Theoretical analysis of the ripple current waveform analysis

The DC to AC converter converts DC-link power to the instantaneous AC output power of the inverter in a sinusoidal pattern and, due to the sinusoidal pattern, the DC link current has a second-order ripple [21]. This is also injected through the DC-DC converter transformer and the DC input battery current has the same sinusoidal ripple in the DC input current.

$$v(t) = Vm\sin\omega t \tag{2}$$

$$i(t) = Im \sin \omega t$$
 (3)

 $p_{load} = Vm \sin \omega t \ x \ Im \sin \omega t \tag{4}$

$$p_{load} = Vm \, Im \, \sin^2 \omega t \tag{5}$$

$$p_{in} = \frac{p_{load}}{\eta} = \frac{Vm \, Im \, (1 - \cos 2\omega t)}{2\eta} \tag{6}$$

$$I_{in} = \frac{Vm Im (1 - cos 2\omega t)}{\eta x^2 V_{in}}$$
(7)

Where,

 $\omega = 2\pi f$ ACoutput frequency,

Vm, *Im* – Peak voltage, current of the load.

Vin - input DC voltage, *lin* – Input DC current.

Pload – Load power, *Pin* – Input DC power.

The instantaneous AC output power of the inverter is in a sinusoidal pattern and this power consumes from the DC-link intermediate section. Due to the sinusoidal pattern, DC-link tank capacitor power reflects the same sinusoidal in DC link current [22].

3.1. Inductors and capacitors filter passive method direct current input ripple reduction

This LC filter ripple reduction is done with a passive element like a capacitor and an inductor. Normally, the fixed PWM duty cycle is preferred for the LC filter ripple reduction. The DC link voltage is more sensitive to the PWM duty cycle of the DC-DC converter. If the DC-DC converter operates with a closed loop of DC-link voltage feedback, it has a lot of perturbation in the DC input battery current during the correction of the DC-link voltage using the PWM duty cycle it may need large size of DC input filter. To optimize the cost and complexity of the DC-link control and filtering, it has been designed with open-loop control and high voltage DC-link capacitor being used in industrial practice. Hence, this method is employed with an open-loop control of the DC-DC converter. The Vref setpoint is fixed to a maximum duty cycle of the PWM.

By enhancing either inductor L_{tank} or capacitor of the C_{tank} in the DC link stage of the filter helps to block the injection of the second-order frequency to the DC input side. This method is called the LC filter method. The LC filter ripple reduction control diagram is depicted in Figure 3. Incrementing the Ltank inductor value will cause an increase in the loss of the L_{tank} filter. Hence, in the LC filter, the capacitor C_{tank} is increased for this experiment to evaluate the DC input ripple. An increment in the C_{tank} capacitor value will help to reduce the DC input ripple current. This can be implemented by adding a filter capacitor in the DC link section. The LC ripple-reduction is simulated in a push-pull DC-DC converter. This is a conventional method and is also called a passive method.



Figure 3. LC filter method open-loop control diagram

3.2. The active method of direct current input ripple reduction

In the active method, the push-pull converter triggering pulses are controlled by a closed-loop operation with the feedback of the DC link voltage and current. The Active ripple-reduction technique closed-loop control diagram is depicted in Figure 4. The Vref is compared with DC-link voltage feedback and the difference is given to the PI stage1. This PI stage 1 output is the set point of the current reference. This is compared with the push-pull converter transformer for secondary current feedback. This summer output is given to the PI stage 2. The PI stage 2 output is directly given to the PWM controller to generate the PWM pulses for the push-pull converter. This dual feedback control implementation helps to reduce the second-order fundamental frequency ripple in the DC input [23], [24]. This compensation technique will help to balance the DC-link capacitor energy and maintain the average level of energy consumption from the DC input sources and the DC input current ripples are controlled. The percentage of ripple will be calculated with a formula of:

$$percentage of I ripple = \frac{Irms \ value \ of \ the \ ripple \ ac \ components}{avarage \ dc \ current} \ x \ 100$$
(8)

It is elaborated further,

Percetage of I ripple =
$$\frac{\sqrt{Irms^2 - Iin^2}}{I_{in}} x \, 100$$
 (9)

By using the active ripple current reduction method, with an optimal value of DC-link capacitor, the DC input current ripple-reduction can be achieved. The DC input power consumption is maintained based on the AC output power consumption and the DC input current ripple is controlled [25].



Figure 4. Active method ripple-reduction closed-loop control diagram

4. SIMULATION ANALYSIS

4.1. Inductors and capacitors filter method direct current input ripple reduction

The LC filter method has been verified in a dual-stage inverter simulated model with a help of power simulator (PSIM) simulation tool software. The LC filter PSIM simulation model is depicted in the Figure 5. It is a combination of a push-pull converter and a full-bridge DC-AC converter. The DC input is a 48 V battery source and it is connected to the push-pull converter. The PSIM simulation components parameter details are shown in Table 1.



Figure 5. Simulation model of LC filter method

Table 1. Simulation model PSIM param

Parameters	Values
Input DC voltage (Vin)	48 V
Transformer ratio (Np : Ns)	1:10
Forward inductor (<i>Ltank</i>)	1.5 mH
DC tank voltage (Vtank)	385 V
Switch frequency of DC-DC (<i>fs</i>)	50 kHz
Switch frequency of DC-AC (<i>fs</i>)	19.5 kHz
Power rating (W)	0.8 kW
R Load	66 ohm

The push-pull converter output is rectified by the diode full bridge and the rectified DC link voltage is 385 V. It is connected to the DC-AC IGBT full-bridge inverter section and it converts 385 V to 230 V AC 50 Hz supply. The AC output is connected to the 800 W Load. The inverter ripple analysis is started with the minimum value of the C_{tank} capacitor with 180 μ F capacitor at 48 V DC input. Figure 6 waveform shows the response of the 180 μ F capacitor. The DC input average current of 17.4 A and the ripple current of 10.6 A is observed and the percentage of ripple is 60.8%. Figure 7 waveform shows the response of the Ctank with a 720 μ F capacitor. In the DC input average current of 17.7 A, the ripple current of 3.51 A is observed and the percentage of ripple is 19.8%.



Figure 6. LC filter method DC input current ripple with a 180 μF DC link capacitor

Figure 7. LC filter method DC input current ripple with 720 μ F DC link capacitor

DC link capacitor at 4,140 μ F ripple current reduces to 0.66 A. The percentage of ripple reduces to less than 3.7% and it meets the standard psophometric noise test passing limits. In the simulation, the DC link C_{tank} capacitor value varied from 180 μ F to 4,140 μ F and the DC input ripple current and percentage of ripple are tabulated. By increasing the C_{tank} capacitor value, the DC input current ripple amplitude is gradually reduced. The graph with filter capacitance vs percentage of input ripple current and DC input current ripple amplitude is depicted in Figure 8. This passive method is used in the conventional model industrial telecom inverters to meet the telecom standard requirement.



Figure 8. LC filter passive method: DC-link capacitance vs % of DC input current ripple

4.2. The active method of direct current input ripple reduction

The active method of the closed-loop DC ripple reduction method has been simulated in the PSIM tool and simulation model is depicted in the Figure 9. The active DC ripple reduction has a dual closed-loop operation, the DC link voltage and current are taken as feedback and given to the closed-loop PI system. The first PI stage closed-loop has compared with the fixed Vref of 2.5 V reference and the feedback of DC link voltage and then the error voltage is processed in PI stage1 and this output has compared with the feedback of transformer secondary current and then the error is processed in the second PI stage is a current closed loop.

By this active method of ripple reduction techniques, the less than 5% of DC ripple is achieved with 720 μ F filter capacitors. At 48 V DC input, the DC input ripple current has simulated and the AC output voltage, current and DC input voltage, current waveform response is shown in Figure 10. Due to the narrow bandwidth of the 100 Hz ripple reduction of active filter method at steady-state condition, the input current of inverter begets 3.2% DC ripple current and 0.62 A of ripple current with 720 μ F capacitor and same operating condition of the passive method at 48 Vdc input and 800 W load. From the summary of the simulation study and comparison analysis results, the active filter DC ripple reduction is more effective than the LC filter method. The test result analysis and comparisons are depicted in Figure 11.



Figure 9. Simulation model of active filter method



Figure 10. Active method: DC input current ripple with a 720 μ F DC link capacitor



Figure 11. Simulation results of % ripple current comparison between LC filter method and active filter method

Based on the comparison between the passive and active methods, with the same value of the DC link capacitor, the current ripple is greater with the passive method and less with active methods. The passive method is 19.8% (3.51 A), but it is reduced to 3.2% (0.62 A) by the active method. For the battery, the accepted ripple current limit is less than 5% and also meets the psophometric norm.

5. EXPERIMENTAL RESULTS

The LC filter and active filter ripple control methods have been experimented with and verified in the dual-stage 48 V/230 V, 1 kVA telecom industrial inverter. The experimental test setup of industrial inverter and ripple waveform capture set up has been shown in the Figure 12. The first stage converter is a push-pull-forward converter is designed to operate with the nominal voltage of 48 V and the second stage is a full-bridge inverter stage. The telecom site system is set up with a 48 Vdc operational voltage, and it draws power from the battery, which is connected to a battery charger in parallel. The standard working range of a telecom inverter is 40 to 60 Vdc. The push-pull-forward converter is taking power from the battery and it is switched to 50 kHz. The push-pull converter PWM generation has designed with a UC 2525 PWM controller

and operational amplifier LM2903. These PWM pulses are given to the MOSFET drivers and it is triggering the MOSFET Q1 and Q2. The DC-DC converter transformer is designed with ETD 54 N87 core and the transformation ratio of 1:10 and the transformer secondary pulsated output voltage is rectified with D1 to D4 fast diode full-bridge rectifier. The rectified DC link voltage is filtered with an LC filter. The DC link voltage of 385 V is converted to the AC sinewave by sine PWM techniques. The Atmel 328 microcontroller is used to control the second stage of the full-bridge inverter. The AC sine wave output is generated by using the level 3 sinusoidal PWM technique. Its switching frequency is 19.5 kHz. The second stage full-bridge inverter designed with IGBT T1 to T4. The output of the full-bridge pulsated sine output is filtered by the differential LC filter and its inductor values are 1.2 mH and capacitance is 4.7 μ F/275 V. By this above process, the DC-link 385 V voltage is converter to AC 230 V/50 Hz supply and it supplies to the critical telecom load backup application. In the experimental prototype hardware components, part number details are shown in Table 2.



Figure 12. The experimental test set of dual-stage industrial telecom inverter

Table 2. Prototype major component parts list		
Parameters	Part Numbers	
Microcontroller	ATMEGA328	
PWM Controller U1	TI UC2525	
IGBT T1 to T4	ST STGP19N60KD -600 V, 20 A	
MOSFET Q1, Q2	IR IRFP4127PBF -200 V, 70 A	
Operational Amplifier	TI LM2903	
Diode D1 to D4	Fairchild MUR880 - 800 V, 8 A	

5.1. Inductors and capacitors filter direct current ripple reduction method

The LC filter method and active filter DC ripple reduction methods are implemented in the industrial inverter 48 V/230 V, 0.8 kW telecom inverter and the experimental test results are analyzed. The LC filter method has experiment, the push-pull converter control circuit is modified to generate a full pulse width constant PWM pulses for the UC2525 controller. Since it is operated with an open-loop system, the DC-DC converter is operated up to 43 V input supply and the DC link voltage is maintained less than the maximum operation voltage of the DC link capacitors (450 V). The LC filter method experimental analysis is done at 43 V input supply and waveforms are captures and analyzed. In the LC filter method, the DC input current has a ripple peak to peak of 16 A peak to peak and it has 40 A overall peak current at 800 W resistive load and average current of 26.2 A and the percentage of ripple 21.6%. With an 180 μ F capacitor, the DC input current waveform is shown in Figure 13.

With a 720 μ F (4x180 μ F) C1 DC link capacitor, at 43 V voltage operation, the DC input current has a ripple peak to peak of 10 A peak to peak and it has 25 A overall peak current at 800 W resistive load and average current of 21.2 A and the percentage of ripple 16.7%. With a 720 μ F capacitor, the DC input current waveform is shown in Figure 14. The DC input current has a ripple peak to peak of 1.4 A peak to peak and it has 22 A overall peak current at 800 W resistive load and average current of 21.6 A and the percentage of ripple 2.3%. With a 4,140 μ F capacitor, the DC input current waveform is shown in Figure 15.



Figure 13. LC filter method: DC input current ripple with a 180 µF DC link capacitor



Figure 14. LC filter method: DC input current ripple with a 720 μ F DC link capacitor



Figure 15. LC filter method: DC input current ripple with a 4,140 µF DC link capacitor

5.2. The active method of direct current ripple reduction control

The active method is operating with closed-loop control of operating DC-DC converter system. It gives dual benefits one helps to maintain the DC link voltage at 385 V and the second help to average power consumption for the DC link section. With the active method, the DC input current waveform is shown in Figure 16.



Figure 16. Active filter method: DC input current ripple with a 720 µF DC link capacitor

With 720 μ F DC-link capacitance, the input DC current has a ripple of 1.2 A peak to peak and 22.0 A overall peak current at 800 W resistive load. The average current of 21.5 A and the percentage of ripple 1.97%. It features a low amount of AC components and a flat DC input current. The inverter size is reduced, the weight is reduced, and the cost is reduced using this technology.

It contributes to the battery's improved performance and longevity. This ripple reduction also aids efficient power consumption and enhances the inverter's backup duration. From the summary of the test results, the active filter DC ripple-reduction is more effective than the LC filter method and the test results

comparisons are depicted in Figure 17. The psophometric noise test (ETSI300132-2) measures battery ripple voltage with a standard test procedure and the battery ripple should be lower the 2 mV. The emission of noise is measured with decibel. The passing limit is less than -51 db. This test was conducted in the operating range of 40 to 60 V DC input. With the active method, the noise emission reduces and it passes the limits of the standard.



Figure 17. Experimental results of % ripple current comparison between LC filter method and active filter method

6. CONCLUSION

The low-frequency ripple-reduction active and passive methods has been tested within the telecommunication working with 48 V DC supply and the output of AC 230 V with a power rating of 1 kVA/800 W. The root cause of ripple generation is being investigated. In this paper, the push-pull DC-DC converter DC input ripple-reduction characteristics are investigated by the LC filter method and the active dual PI closed-loop control method. The two different ripple-reduction methods' results are compared. In the LC method, which is evaluated by increasing the C_{tank} capacitance value, the DC input current ripple-reduction is observed and, with a 4,140 μ F capacitance value, the ripple current is reduced to less than 5% and the DC input supply ripple voltage is less than 2 mV (-51 dB). It also complies with the psophometric norm ETSI300132-2. The DC input ripple is reduced in the active ripple-reduction method to a small value of C_{tank} capacitance of 720 μ F, and with this value, the 5% DC input ripple psophometric norm requirement is met. The LC method requires more space to accommodate the large capacitance and is more expensive than the active dual PI ripple-reduction method.

ACKNOWLEDGEMENTS

This material is based upon work supported by the R&D Department of CET Power Solutions India Pvt Ltd, Chennai.

REFERENCES

- L. Zhang, X. Ruan, and X. Ren, "Second-Harmonic Current Reduction for Two-Stage Inverter with Boost-Derived Front-End Converter: Control Schemes and Design Considerations," in *IEEE Transactions on Power Electronics*, vol. 33, no. 7, pp. 6361– 6378, July 2018, doi: 10.1109/TPEL.2017.2746878.
- [2] N. Lu, S. Yang, and Y. Tang, "Ripple Current Reduction for Fuel-Cell-Powered Single-Phase Uninterruptible Power Supplies," in IEEE Transactions on Industrial Electronics, vol. 64, no. 8, pp. 6607–6617, Aug. 2017, doi: 10.1109/TIE.2017.2677329.
- [3] Z. Wei, X. Deng, C. Gong, J. Chen, and F. Zhang, "A novel technique of low frequency input current ripple reduction in twostage DC-AC inverter," *IECON 2012-38th Annual Conference on IEEE Industrial Electronics Society*, 2012, pp. 139–143, doi: 10.1109/IECON.2012.6388818.
- [4] A. H. El Khateb, N. A. Rahim, J. Selvaraj, and B. W. Williams, "DC-to-DC Converter with Low Input Current Ripple for Maximum Photovoltaic Power Extraction," in *IEEE Transactions on Industrial Electronics*, vol. 62, no. 4, pp. 2246–2256, April 2015, doi: 10.1109/TIE.2014.2383999.
- [5] Hong-Ju Jung and Rae-Young Kim, "A Second-order Harmonic Current Reduction with a Fast Dynamic Response for a Two-Stage Single-phase Grid–connected Inverter," *Journal Electrical Engineering and Technology*, vol. 9, no. 6, pp. 1988–1994, 2014, doi10.5370/JEET.2014.9.6.1988.
- [6] Y. Shi, B. Liu, and S. Duan, "Low-Frequency Input Current Ripple Reduction Based on Load Current Feedforward in a Two-Stage Single-Phase Inverter," in *IEEE Trans. on Power Elec.*, vol. 31, no. 11, pp. 7972–7985, 2016, doi: 10.1109/TPEL.2015.2513065.
- [7] H. Deng, Q. Li, Z. Liu, L. Li, and W. Chen, "Low frequency current ripple mitigation of two stage three-phase PEMFC generation systems," *Journal of Power Electronics*, vol. 16, no. 6, pp. 2243–2257, 2016, doi: 10.6113/JPE.2016.16.6.2243.
- [8] H. G. Jeong, G. S. Kim, and K. B. Le, "Second order harmonic reduction technique for photovoltaic power conditioning systems using a proportional-resonant controller," *Energies*, vol. 6, no. 1, pp. 79–96, 201, 2013, doi: 10.3390/en6010079.

- [9] A. A. Ahmad and A. Abbrishamafar, "Low Frequency current ripple reduction in Two stage power converter with a PI Controller and Non Linear Gain," *Iranian Journal of electrical and computer engineering*, vol. 11, no. 2, pp. 102–108, 2012.
- [10] R. Jeyaraman and C. N. Ravi, "Low-frequency DC Input current ripple Reduction in a Two-stage Single-Phase Inverter using DC Input Voltage control," 2020 6th International Conference on Advanced Computing and Communication Systems (ICACCS), 2020, pp. 342–347, doi: 10.1109/ICACCS48705.2020.9074204.
- [11] J. Wang, K. Zou, C. Chen, and L. Chen, "A high frequency battery model for current ripple analysis," 2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition (APEC), 2010, pp. 676–680, doi: 10.1109/APEC.2010.5433598.
- [12] A. D. Kupchinov, N. N. Smotrov, and Y. P. Gusev, "The compatibility verification of batteries and battery chargers to ripples in battery float charge mode," 2018 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering (EIConRus), 2018, pp. 696–700, doi: 10.1109/EIConRus.2018.8317189.
- [13] A. D. Kupchinov, Y. P. Gusev, and Y. V. Monakov, "Batteries current ripples in float charge mode," 2017 IEEE Conference of Russian Young Researchers in Electrical and Electronic Engineering, 2017, pp. 913–915, doi: 10.1109/EIConRus.2017.7910704.
- [14] K. Gupta, M. Sharma, and D. Verma, "Design and Fabrication of Two Stage 2 KVA Inverter using Push-Pull Topology," 2020 International Conf. on Communication and Signal Processing, 2020, pp. 1027–1031, doi: 10.1109/ICCSP48568.2020.9182234.
- [15] B. G. Mayuri and U. S. Swati, "Design of residential photovoltaic power system using current-fed push-pull front end converter," 2017 IEEE Inter. Conf. on Power, Control, Signals and Instr. Engin, 2017, pp. 354–357, doi: 10.1109/ICPCSI.2017.8392314.
- [16] W. Meesrisuk, N. Sarasiri, and A. Jangwanitlert, "Ripple current reduction using interleaving technique for three-level ZVZCS DC-DC converter," 2016 IEEE Region 10 Conference (TENCON), 2016, pp. 837–841, doi: 10.1109/TENCON.2016.7848122.
- [17] L. An and D. D. Lu, "Analysis of DC Bus Capacitor Current Ripple Reduction in Basic DC/DC Cascaded Two-Stage Power Converters," in *IEEE Trans. on Industrial Electr.*, vol. 63, no. 12, pp. 7467–7477, Dec. 2016, doi: 10.1109/TIE.2016.2594162.
- [18] M. Schuck and R. C. N. Pilawa-Podgurski, "Input current ripple reduction through interleaving in single-supply multiple-output dc-dc converters," 2013 IEEE 14th Workshop on Contr. & Model for Power Electr., 2013, pp. 1–5, doi: 10.1109/COMPEL.2013.6626436.
- [19] J. Lee, Y. Jeong, and B. Han, "A Two-Stage Isolated/Bidirectional DC/DC Converter with Current Ripple Reduction Technique," in *IEEE Transactions on Industrial Electronics*, vol. 59, no. 1, pp. 644–646, Jan. 2012, doi: 10.1109/TIE.2011.2109343.
- [20] M. N. Musarrat, M. R. Islam, K. M. Muttaqi and D. Sutanto, "Shunt Active DC Filter to Reduce the DC-Link Ripple Current Caused by Power Converters to Improve the Lifetime of Aluminum Electrolytic Capacitors," in *IEEE Transactions on Industry Applications*, vol. 57, no. 4, pp. 4306–4315, July–Aug. 2021, doi: 10.1109/TIA.2021.3083636.
- [21] W. Lee, B. Han, and H. Cha, "Battery ripple current reduction in a three-phase interleaved dc-dc converter for 5 kW battery charger," 2011 IEEE Energy Conversion Congress and Exposition, 2011, pp. 3535–3540, doi: 10.1109/ECCE.2011.6064247.
- [22] A. K. Singh, M. K. Pathak, and Y. S. Rao, "A new two-stage converter with reduction of DC-link capacitor for plug-in electric vehicle battery charger," 2017 3rd Inter. Conf. on Comp. Intell. & Commun. Tech., 2017, pp. 1–6, doi: 10.1109/CIACT.2017.7977338.
- [23] J.-H. Park, H.-G. Jeong, and K.-B. Lee, "Output Current Ripple Reduction Algorithms for Home Energy Storage Systems," *Energies*, vol. 6, no. 10, pp. 5552–5569, 2013, doi: 10.3390/en6105552.
- [24] H. Wu, V. Pickert, S. Lambert, P. Allanf, X. Deng and H. Zhan, "A ripple reduction method for a two stages battery charger with multi-winding transformer using notch filter," 2017 IEEE 12th International Conference on Power Electronics and Drive Systems (PEDS), 2017, pp. 1,101-1,106, doi: 10.1109/PEDS.2017.8289265.
- [25] C. Bai et al., "Novel input current ripple compensation technique for capacitor-less dual-half-bridge converter," 2017 IEEE Applied Power Electronics Conference and Exposition (APEC), 2017, pp. 2015–2021, doi: 10.1109/APEC.2017.7930976.

BIOGRAPHIES OF AUTHORS



Jeyaraman Ramakrishnan **D** S S S **D** was born in Aruppukottai Tamil Nadu in 1982. He received his B.E degree in Electrical and Electronics Engineering from Madurai Kamaraj University, Madurai, India, in 2004 and his Master degree in Power electronics from P.S.G College of Technology Coimbatore, India, in 2007. Currently he is working as a senior manager-R&D in CET Power Solutions India Pvt Ltd. Chennai and he is purchasing towards his Ph.D degree in Sathyabama Institute of Science and Technology, Chennai, India. He has 15 years of industrial experience. His current research interests include power electronics and its applications such as optimization of the converter and inverter, renewable energy system, reliability and telecommunication inverter safety compliance with safety, EMC standards. He can be contacted at email: jeyam.apk@gmail.com.



Chengalvarayan Natarajan Ravi \bigcirc \bigotimes was born in Chennai, Tamil Nadu, in 1978. He received Bachelor of Engineering degree in Electrical and Electronics Engineering in the year 1999 from Crescent Engineering College, Chennai. Master of Engineering degree in Power Systems in the year 2006 from B.S.A.R Crescent Engineering College, and Ph.D in power system optimization techniques from Sathyabama University, Chennai, Tamilnadu, India at present he is working as professor in Vidya Jyothi Institute Technology, Hyderabad, Telangana State, India. He has 15 years of teaching and 5 years of industrial experience. He received best teacher award in the year 2019 from ESN awards. He has guided several projects in the areas Power Electronics, Power Systems, and Electric Drives. His area of interest is power system optimization, FACTS, power electronics and renewable energy system. He can be contacted at email: ravicn@vjit.ac.in.