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A family of switched-impedance network enhanced-boost quasi-Z-source inverters

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ABSTRACT

This paper proposes a family of novel enhanced-boost quasi-Z-source inverters (EB-qZSIs). For the similar input voltage and shoot-through duty ratio, similar to that of enhanced-boost Z-source inverter/enhanced-boost qZSIs, the presented topologies provide very high voltage boost at high modulation index with improved quality output waveform. Compared to EB-ZSI and EB-qZSIs, these topologies provide less capacitors stress, which reduce the volume and cost of the system. Akin to traditional EB-qZSIs, the presented novel impedance networks share joint ground with the source and inverter bridge, also reduces the initial inrush current. Among the four types of proposed configurations, the type-1 of discontinuous input current (DIC) EB-qZSIs offers fewer stress athwart the capacitors and little inrush current at start-up condition. Consequently, type-1 is considered and illustrated for the examination, simulation, and hardware execution. The steady-state operation and derivation of boost factor, peak direct current-link (DC-link) voltage and capacitor voltages are derived for both continuous conduction mode (CCM) and discontinuous conduction modes (DCM). The Z-network elements design, and evaluation with other Z-networks are also carried out. Lastly, the hypothetical investigation is confirmed with simulation and experimental tests.

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1. INTRODUCTION

Single-stage voltage source inverter (VSI) and current source inverter (CSI) can only offer either step-down or step-up direct current-alternating current (DC-AC) conversion correspondingly [1]. To achieve high output voltage, an additional boost converter has been cascaded among the source and the inverter bridge, or a step-up transformer has to be connected at the output side of the inverter bridge. This two-stage conversion rises the complexity and cost of the system and lowers the efficiency [2]. Besides, the ON state of both the switching devices in any phase leg of both the single-stage and two-stage converter can lead to dead-short circuit of the input supply. To avoid this, an extra dead-band circuit is needed between the phase legs, which increases the cost and distortion in the output waveform.

Therefore, to avoid the above-mentioned drawbacks and to have greater ac output voltage with high reliability, a single-stage Z impedance-source inverter (ZSI) was proposed, which consist of two capacitors, two inductors and the input diode in the Z-network [3]. The traditional ZSI has some problems; those difficulties can be eliminated by some adjustments in the Z-network with same count of elements [4], [5].

Nevertheless, these networks could'nt expand their voltage gain. Consequently, to expand the voltage gain, the inductors in traditional ZSI were swapped with switched-inductor (SL) cells [6]. The downsides of SL-ZSI were minimized in [7]. The protracted quasi(q)-ZSIs were projected in [8] with higher voltage gain and slighter quantity of inductors and diodes. Pan [9], L-ZSI was presented to prohibit the inrush current with only inductors and diodes in the impedance network. The switched-boost inverters (SBIs) which were proposed in [10]–[14] offers about matching voltage gain as that of the ZSI [3] with a reduced quantity of inactive elements but with an additional set of diode and switch.

To further enhance the boost factor by changing together duty cycle and turns ratio easily, numerous magnetically-coupled Z-source (MCIS) configurations were presented in [15]–[21]. Depending on the components used in the impedance network, these MCIS networks can be classified as two winding [16], [17], three winding [18], [19], and active MCIS networks [20], [21]. But either their magnetic coupling must be robust or their leakage inductance must be small enough. Then, massive voltage prickles will appear athwart the dc-link which requires higher voltage rating switching devices, which in turn rises the cost [22].

Consequently, enhanced-boost ZSI (EB-ZSI) was presented, which provides high voltage gain at low duty cycle [23]. Akin to traditional ZSI, the EB-ZSI has certain downsides; such as discrete input current, does not share joint ground with supply, hefty inrush current, and high capacitor stress. Some of these difficulties are eradicated by EB-qZSIs using equal count of elements in the Z-network [24], [25]. The two arrangements of EB-qZSIs are revealed in Figure 1 [25]. In Figure 1 (a), capacitor C_2 negative terminal is connected to positive terminal of capacitor C_3 where as in Figure 1 (b) it is connected to supply positive terminal. The boost factor of EB-ZSI [23] and EB-qZSIs [24], [25] are identical and is given as shown in (1).

$$B = \frac{\hat{V_{PN}}}{V_{DC}} = \frac{1}{1-4D_0+2D_0^2} \quad (1)$$

Where B-boost factor, D_0-shoot-through duty ratio, $\hat{V}_{PN}$-peak dc-link voltage, and V_{DC}-input voltage.

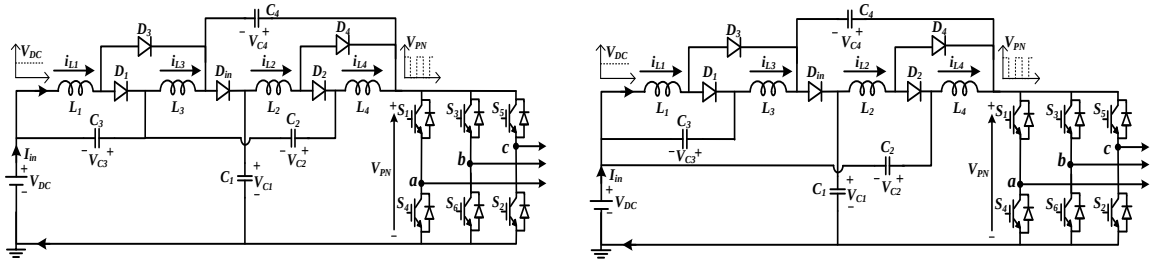


Figure 1. Continuous input current arrangements of enhanced-boost qZSIs in (a) type-1 and (b) type-2 [25]

This paper presents the four novel arrangements of discontinuous input current (DIC) EB-qZSIs with same number of components as that of EB-ZSI/qZSIs, but with low rating due to less capacitor stresses and low starting inrush current. Section 2 describes the working principles, derivation of boost factor and capacitor stresses of type-1 DIC EB-qZSIs for both continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Design of Z-network elements are carried out in section 3. In section 4, the evaluation of current Z-network configurations and the projected configurations are made. Lastly, to confirm the hypothetical examination, the simulation and experimental tests are carried out in section 5.

2. PROPOSED TOPOLOGIES CIRCUIT ARRANGEMENTS AND WORKING PRINCIPLES

The two arrangements of EB-qZSIs operating in continuous input current (CIC) mode are shown in Figure 1 [25] and the four proposed circuit arrangements of the DIC EB-qZSIs topologies are revealed in Figure 2. In Figure 2 (a), the capacitors C_1, C_2, and C_3 are connectected in series due to which it results in less stress across them. The capacitor C_1 negative terminal is connected to negative terminal of C_3 instead of positive terminal and can be depicted in Figure 2 (b). In Figure 2 (c), the capacitors C_1, C_2, and C_3 negative terminals are connected to supply positive terminal, which results in increased voltage stress across them. Figure 2 (d) is similar to Figure 2 (b) except, capacitor C_2 negative terminal is connected to capacitor C_3 positive terminal instead of capacitor C_1. The elements (i.e., both active and inactive) used in these projected configurations are identical as that of the EB-ZSI [23]/EB-qZSIs [24], [25] (i.e., the impedance network is

having five diodes, four capacitors, and four inductors). During zero states, these proposed topologies draw discontinuous input current from the supply with reduced capacitors stress. This discontinuous input current can be avoided using the maximum boost control modulation technique in which all the zero states are converted to shoot-through states [26]. Likewise, these configurations lessen the starting inrush current problem. Akin to traditional EB-qZSIs [24], [25], the presented topologies share common ground with the source and inverter bridge, reduces the capacitors stress, and lessens staring inrush current. All these presented configurations can be controlled using the modulation methods presented for the conventional ZSI [3], [26], [27]. In this framework, the simple boost method (SBC) [3] is used for the examination, comparison, simulation and hardware tests. The principle of operation for the presented topologies is identical to that of the traditional ZSI, having both shoot-through and non-shoot-though states. As all the presented four topologies of DIC EB-qZSIs have the same characteristics, therefore type-1 of DIC EB-qZSI is considered as an example for analysis purpose.

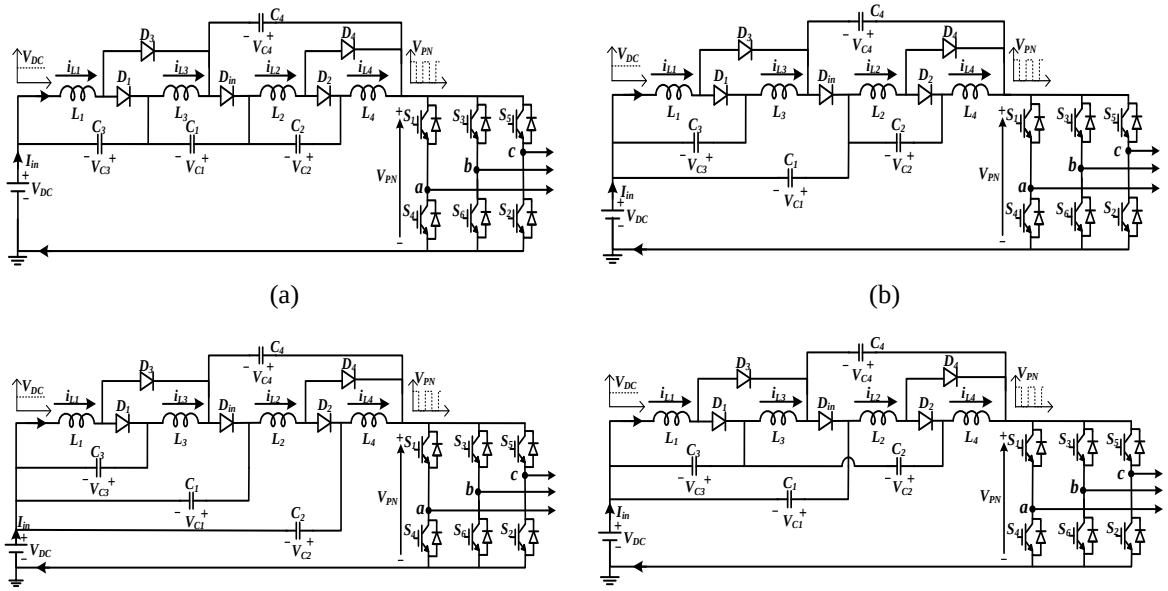


Figure 2. Illustration of proposed discontinuous input current (DIC) EB-qZSIs for (a) type-1, (b) type-2, (c) type-3, and (d) type-4

2.1. Operation and discussion in continuous conduction mode

Figure 2 (a) depicts the illustration of presented type-1 DIC EB-qZSI in which the capacitors C_1, C_2, and C_3 are connected in series to share the dc-link voltage which inturn results in the less stress across them.

– Shoot-through state:

The illustration of the presented topology for type-1 during shoot-through state is depicted in Figure 3 (a). Throughout this mode, both the switching components of either any one–phase or any two–phases or all the three–phase legs are turned-on at the same time to boost the voltage to a required level. The diodes D_{in}, D_1, and D_2 are OFF, whereas the diodes D_3 and D_4 are ON. All the inductors are charged by the input supply and the capacitors, and these inductors store the energy.

According to Kirchhoff's voltage law (KVL), the voltage across inductors and diodes can be stated as:

$$\begin{cases} V_{L1} = V_{DC} + V_{C4}; V_{L2} = V_{DC} + V_{C1} + V_{C3} \\ V_{L3} = V_{DC} + V_{C3} + V_{C4}; V_{L4} = V_{DC} + V_{C1} + V_{C2} + V_{C3} \end{cases} \quad (2)$$

$$\begin{cases} V_{Din} = -(V_{DC} + V_{C1} + V_{C3} + V_{C4}); V_{D1} = -(V_{DC} + V_{C3} + V_{C4}) \\ V_{D2} = -(V_{DC} + V_{C1} + V_{C2} + V_{C3}) \end{cases} \quad (3)$$

and the DC-link voltage across the inverter bridge, $V_{PN} = 0$.

– Non-Shoot-through state

Figure 3 (b) shows illustration of proposed topology for type-1 during non-shoot-through state. The diodes D_{in}, D_1, and D_2 are ON, while the diodes D_3 and D_4 are turned OFF. The energy stored in the inductors

and the input energy is shifted to the dc-link to increase the voltage. The capacitors are charged from the input supply and energy is stored. The resulting expressions can be found subsequently applying KVL to Figure 3 (b).

$$V_{L1} = -V_{C3}; V_{L2} = -V_{C2}; V_{L3} = -V_{C1}; V_{L4} = V_{C2} - V_{C4} \quad (4)$$

$$V_{D3} = -V_{C1};\ V_{D4} = V_{C2} - V_{C4} \quad (5)$$

After applying the volt-sec balance principle to the inductors (i.e., L_1, L_2, L_3, and L_4), the capacitor voltages can be obtained as:

$$\left\{ V_{C1} = \frac{D_0}{(1-4D_0+2D_0^2)} V_{DC};\quad V_{C2} = V_{C3} = \frac{D_0(1-D_0)}{(1-4D_0+2D_0^2)} V_{DC};\quad V_{C4} = \frac{D_0(2-D_0)}{(1-4D_0+2D_0^2)} V_{DC} \right. \quad (6)$$

The expression for the peak dc-link voltage can be written as:

$$\hat{V_{PN}} = V_{DC} + V_{C1} + V_{C3} + V_{C4} = \frac{1}{1-4D_0+2D_0^2} V_{DC} = BV_{DC} \quad (7)$$

From the terms (1) and (7), it can be detected that the boost factor, *B* of the projected configuration for type-1 is same to that of the topologies proposed in [23], [24]. In a similar way, the boost factor for the remaining three topologies can also be obatained and it will be identical as that of EB-ZSI/qZSIs. Similarly, it can be derived that the average dc-link voltage across the inverter bridge of all the four projected topologies is identical to the EB-ZSI [23]/EB-qZSIs [24] and is expressed as:

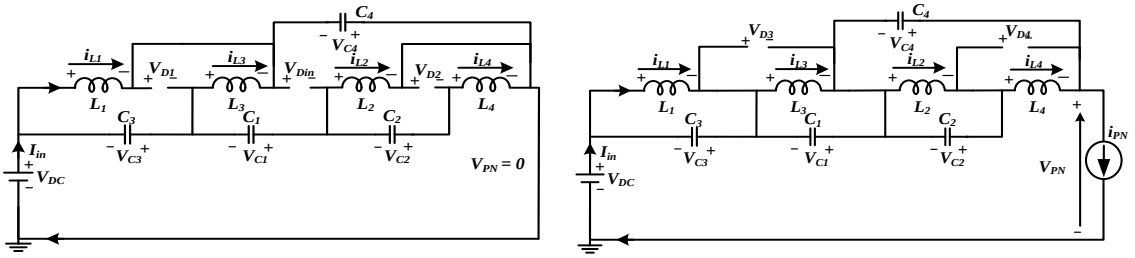
$$\tilde{V_{PN}} = \frac{1-D_0}{1-4D_0+2D_0^2} V_{DC} \quad (8)$$

The peak-phase output voltage is expressed as:

$$\hat{V_{an}} = M.\frac{\hat{V_{PN}}}{2} = M.B\frac{V_{DC}}{2} = G\frac{V_{DC}}{2} \quad (9)$$

The overall ideal voltage gain *G* of the presented network configurations in terms of modulation index *M* can be well-defined by:

$$\text{Voltage gain, } G = M.B = \frac{M}{2M^2-1} \quad (10)$$



(a) (b)

Figure 3. Illustration of type-1 DIC EB-qZSI in (a) shoot-through and (b) non-shoot-through state

2.2. Operation and discussion in continuous conduction mode

The converter may operate in DCM because of low switching frequency, light loads, and low inductance values of inductors [21], [28]. The DCM operation mode causes over-boosting of dc link and output voltage, which can lead to instabilities of the converter and must be taken in consideration while deciding components and switches. Figures 4 (a) and 4 (b) depicts the typical current and voltage waveforms of type-1 DIC EB-qZSI operating in CCM and DCM respectively.

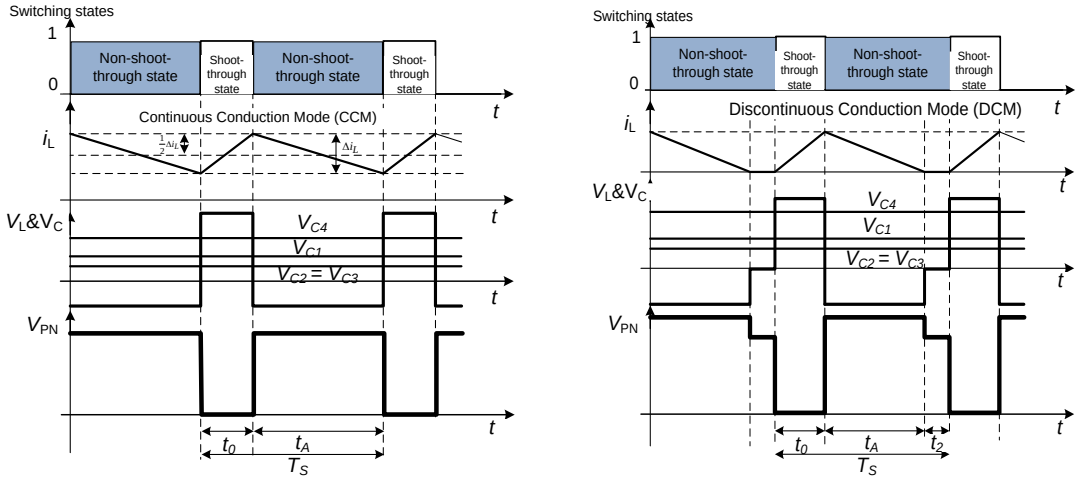


Figure 4. Typical voltage and current waveforms of type-1 DIC EB-qZSI in (a) continuous conduction and (b) discontinuous conduction modes

The functioning period of DCM consists of an active state t_A, a shoot-through state t_0 and a discontinuous conduction state t_2:

$$T_S = t_A + t_0 + t_2 \tag{11}$$

The above equation could also be represented as:

$$= \frac{t_A}{T_S} + \frac{t_0}{T_S} + \frac{t_2}{T_S} = D_A + D_0 + D_2 = 1 \tag{12}$$

where D_A-duty cycle of active state, D_0-shoot-through state, and D_2-discontinuous conduction state. Whereas the equivalent configurations of the EB-qZSI converter working in the shoot-through and active states remain the identical as in Figure 3. When the converter is in a discontinuous conduction mode (DCM) t_2, the voltages of the inductors L_1, L_2, L_3, and L_4 are equal to zero.

For a discontinuous conduction mode, in (2) and (4) could be extended as shown in:

$$V_{L1} = D_0(V_{DC} + V_{C4}) + (1 - D_2 - D_0)(-V_{C3}) = 0 \tag{13}$$

$$V_{L2} = D_0(V_{DC} + V_{C1} + V_{C3}) + (1 - D_2 - D_0)(-V_{C2}) = 0 \tag{14}$$

Similarly, for inductors L_3 and L_4, it can be expressed as:

$$V_{L3} = D_0(V_{DC} + V_{C3} + V_{C4}) + (1 - D_2 - D_0)(-V_{C1}) = 0 \tag{15}$$

$$V_{L4} = D_0(V_{DC} + V_{C1} + V_{C2} + V_{C3}) + (1 - D_2 - D_0)(V_{C2} - V_{C4}) = 0 \tag{16}$$

From the above equations, we can obtain capacitor C_3 and C_2 voltages as:

$$V_{C2,C3} = \frac{D_0}{(1-D_2-D_0)} \frac{[(1-D_0)^2 - D_2(1-D_0)]}{(2D_0^2 - 4D_0 + 1) - D_2(1-2D_0)} V_{DC} \tag{17}$$

From above two equations, it can be obtained capacitor C_4 and C_1 voltages as:

$$V_{C4} = \frac{D_0(2-D_0-D_2)}{(2D_0^2 - 4D_0 + 1) - D_2(1-2D_0)} V_{DC}; V_{C1} = \frac{D_0}{(2D_0^2 - 4D_0 + 1) - D_2(1-2D_0)} V_{DC} \tag{18}$$

The ideal DC-link voltage of DIC EB-qZSI for the DCM can be expressed as:

$$V_{PN} = \frac{(1-D_2)}{(2D_0^2-4D_0+1)-D_2(1-2D_0)} V_{DC} = B_{DCM} V_{DC} \quad (19)$$

where, B_{DCM} (i.e., boost facror during DCM) is written as:

$$B_{DCM} = \frac{(1-D_2)}{(2D_0^2-4D_0+1)-D_2(1-2D_0)} \quad (20)$$

Comparing (7) and (20) it can be specified that the changeover from CCM to DCM rises the boost factor. This is so called over boost effect, which can lead to unbalanced operation and damage of elements. It can also be detected that, at D_2=0; the boost factor expressed in (20) is same as (7). Similarly, the capacitor voltages expressed in (17)-(19) are same as (6) at D_2 = 0.

3. PARAMETER DESIGN OF Z-NETWORK

Normally, the design of Z-network elemenys primarily depends upon the component current and voltage stresses which are summarized in Table 1. Similarly, in this section type-1 DIC EB-qZSI is taken as an illustration to exemplify the components design. As enlightened in section 2, in shoot-through state, the capacitors charge the inductors, and it is also detected that the inductor voltages (V_{L1}=V_{L2} and V_{L3}=V_{L4}) are same for all proposed topologies and the arrangements proposed in [23], [24].

Table 1. Parameter comparison of proposed topologies

Parameters		EB-ZSI [23]	EB-qZSI [24]	Continuous input current (CIC) Figure 1 (a) [25]	Continuous input current (CIC) Figure 1 (b) [25]	Family of proposed configurations of EB-qZSIs Discontinuous input current (DIC) configurations Figure 2 (a)	Figure 2 (b)	Figure 2 (c)	Figure 2 (d)
Boost Factor/ Switch Stress		$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$	$\frac{1}{1-4D_0+2D_0^2}$
Capacitors Stress	$\frac{V_{C1}}{V_{DC}}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{D_0}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
	$\frac{V_{C2}}{V_{DC}}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{(1-D_0)^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0(3-5D_0+2D_0^2)}{(1-D_0)(1-4D_0+2D_0^2)}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
	$\frac{V_{C3}}{V_{DC}}$	$\frac{(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{1-3D_0+D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{D_0(1-D_0)}{1-4D_0+2D_0^2}$
	$\frac{V_{C4}}{V_{DC}}$	$\frac{(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$	$\frac{2D_0-D_0^2}{1-4D_0+2D_0^2}$
Diodes Stress	$\frac{V_{Din}}{V_{DC}}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$	$\frac{-1}{1-4D_0+2D_0^2}$
	$\frac{V_{D1,D2}}{V_{DC}}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$	$\frac{-(1-D_0)}{1-4D_0+2D_0^2}$
	$\frac{V_{D3,D4}}{V_{DC}}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$	$\frac{-D_0}{1-4D_0+2D_0^2}$
Inductor Currents		$i_{L1,L2} = \frac{(1-D_0)}{1-4D_0+2D_0^2} I_{PN}$, $i_{L3,L4} = \frac{(1-D_0)^2}{1-4D_0+2D_0^2} I_{PN}$				$i_{L1,L2} = \frac{(1-D_0)}{1-4D_0+2D_0^2} I_{PN}$, $i_{L3,L4} = \frac{(1-D_0)^2}{1-4D_0+2D_0^2} I_{PN}$			
Input Current		$2i_{L3} - I_{PN}$	i_{L1}	i_{L1}	i_{L3}	I_{PN}	I_{PN}	I_{PN}	I_{PN}
Voltage Gain, *G*		$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$	$\frac{M}{2M^2-1}$

Consequently, the inductors of the projected DIC configurations of EB-qZSIs can be calculated by:

$$L_{1,2} = \frac{D_0(1-D_0)^2}{f_s \Delta i_{L1,L2} k_{sh}(1-4D_0+2D_0^2)} V_{DC}; \qquad L_{3,4} = \frac{D_0(1-D_0)}{f_s \Delta i_{L3,L4} k_{sh}(1-4D_0+2D_0^2)} V_{DC} \quad (21)$$

similarly, the capacitors of type-1 DIC EB-qZSI can be designed as:

$$C_{1,4} = \frac{D_0(2-3D_0+D_0^2)}{f_s \Delta V_{C1,C4} k_{sh}(1-4D_0+2D_0^2)} I_{PN};\ C_2 = \frac{D_0(1-D_0)^2}{f_s \Delta V_{C2} k_{sh}(1-4D_0+2D_0^2)} I_{PN};\ C_3 = \frac{D_0(3-5D_0+2D_0^2)}{f_s \Delta V_{C3} k_{sh}(1-4D_0+2D_0^2)} I_{PN} \quad (22)$$

where f_s - the switching frequency, k_{sh} - the no. of shoot-through states over a period, T, and Δ - denotes the inductor current and capacitor voltage ripples. From above equations, it can also be observed that the components (capacitors, inductors) ratings can be reduced with increase in switching frequency.

For a lossless system, the input and output power of the converter must be in balance (i.e., $P_{in} = P_0$),

$$\begin{cases} P_{in} = V_{DC} i_{in} \\ P_0 = 3V_{an} i_{an} \cos \Phi \end{cases} \quad (23)$$

where, P_{in} – input power and P_0 – is the output power. In order to operate the inverter in CCM, the minimum inductor current (I_{Li_min}) should be greater than zero. The average inductor current should be equal to the peak value of the phase current (I_{an}). Exactly, it is written as:

$$I_{Li,avg} = \left(I_{Li} - \frac{1}{2} \Delta i_{Li}\right) \geq I_{an} \quad (24)$$

substituting the (21) and (23) in above expression,

$$I_{Li,avg} = \left(\frac{3V_{an} i_{an} \cos \Phi}{V_{DC}} - \frac{1}{2} \frac{D_0 V_{Li}}{i_{Li} L_i k_0 f_s}\right) \geq I_{an} \quad (25)$$

$$I_{Li,avg} == \left(\frac{3V_{an} \cos \Phi}{V_{DC}}\right) \geq \left(\frac{1}{2} \frac{D_0 V_{Li}}{I_{an} i_{Li} L_i k_0 f_s}\right) \quad (26)$$

after generalization of the (27), the critical inductances L_{Ci} of the inductor L_i is gained as:

$$L_{Ci} \geq \frac{D_0 V_{Li} V_{DC} Z_{an}}{2V_{an} i_{Li} k_0 f_s} \left(\frac{1}{3V_{an} \cos \Phi}\right) \quad (27)$$

where load impedance per phase, $Z_{an} = R_L + jX_L$, and R_L - resistive load per phase, X_L - inductive load per phase, $\cos ø$ – load power factor, and f_s – switching frequency.

4. ASSESSMENT OF THE PROPOSED DIC EB-qZSI TOPOLOGIES

In this segment, the projected four configurations are related with supplementary Z-source networks, such as the SL-ZSI [6], EB-ZSI [23], and the EB-qZSIs [24], [25]. The expressions of boost factor, components voltage, current stresses, and the input current are derived and are summarized in Table 1. The diodes voltage of the projected configurations and the EB-ZSI/EB-qZSIs is equal and is fewer than the SL-ZSI. Likewise, for comparison purpose, the number of components used, start-up current, and the sharing of common ground are briefed in Table 2. The assessments are accomplished on their boost abilities and components stresses.

Table 2. Comarison of novel topologies with other existing Z-source networks

S. No	Topology		Common Ground	Continuous Input Current	Start-up Current	Components			
						L	C	D	S
1	EB-ZSI [23]		No	No	Yes	4	4	5	6
2	EB-qZSI [24]		Yes	Yes	No	4	4	5	6
3	Figure 1 (a) [25]		Yes	Yes	No	4	4	5	6
4	Figure 1 (b) [25]		Yes	Yes	No	4	4	5	6
5	Proposed	Figure 2 (a)	Yes	Yes*	No	4	4	5	6
6	novel four	Figure 2 (b)	Yes	Yes*	No	4	4	5	6
7	configurations	Figure 2 (c)	Yes	Yes*	No	4	4	5	6
8		Figure 2 (d)	Yes	Yes*	No	4	4	5	6

4.1. Boost factor and switch stress assessment

Figure 5 portrays the assessment of boost factor and stress across the power switches for the traditional ZSI, SL-ZSI, EB-ZSI, EB-qZSIs, and the projected configurations. As shown in Figure 5 (a), for

the similar duty ratio D_0, the boost factor of the projected configurations is identical as to that of the EB-ZSI/ EB-qZSIs and is stronger than the ZSI and SL-ZSI. Correspondingly, the plot of switch stress versus voltage gain G for the projected configurations and the ZSI, SL-ZSI, EB-ZSI, and EB-qZSIs are shown in Figure 5 (b). From this figure it is detected that the stress across the switch in the projected configurations are same as that of the EB-ZSI/EB-qZSIs and is less when compared to ZSI, and SL-ZSI. Hence, lesser rating active devices can be used which decreases the cost.

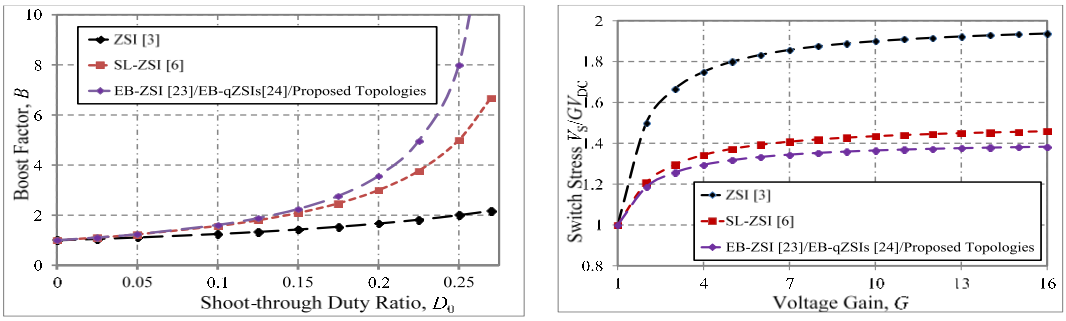


Figure 5. Evaluation of (a) boost factor and (b) switch stress

4.2. Comparison of capacitor stress

As compared in Table 1, Figure 6 shows a conspiracy of the capacitor's stress versus voltage gain for all the four projected configurations, SL-ZSI, EB-ZSI, and the EB-qZSIs. It is observed from Figure 6 (a) and Figure 6 (b), that the stress across capacitor C_1 and capacitor C_2 is less in the proposed topologies. Figure 6 (c) shows that stress across the capacitor C_3 is same in the proposed topologies as that of EB-qZSIs [24]. From this illustrattion, it can be detected that the total stress across the capacitors is less in the projected configurations when compared to other configurations. Furthermore, it is also detected that the capacitor's stress and starting inrush current in case of type-1 DIC EB-qZSI is less when compared to other three proposed configurations.

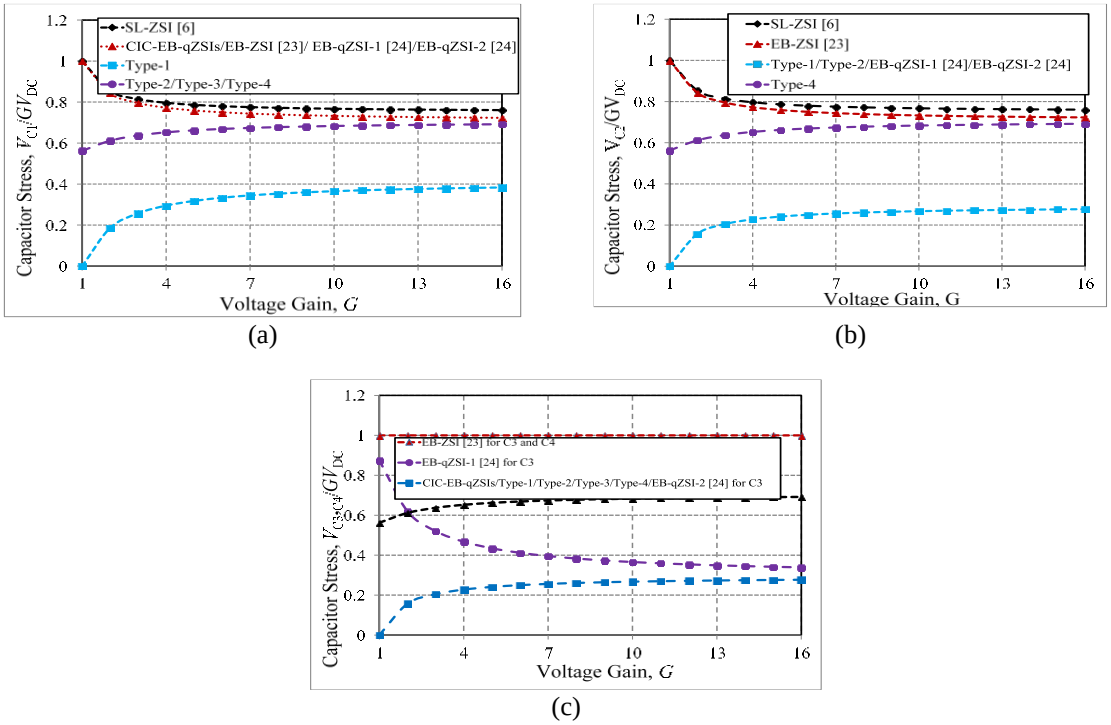


Figure 6. Proposed topologies capacitor stress comparison with other topologies (a) capacitor C_1 stress comparison, (b) capacitor C_2 stress comparison, and (c) capacitor C_3 and C_4 stress comparison

5. DISCUSSION ON SIMULATION AND EXPERIMENTAL RESULTS

To authenticate the hypothetical investigation discussed in section 3, the simulation and experimental test is performed. In order to harvest 110 Vrms as the output voltage, the projected converter is operated with simple boost control technique [3] at V_{DC} = 60 V, D_0 = 0.24112, M = 0.75888, with $L_{1,2,3,4}$ = 1 mH, $C_{1,2,3,4}$ = 1000 µF, load per phase is R_l = 40 Ω, L_l = 2.5 mH, and switching frequency, f_s =10 kHz. For a given input voltage and duty ratio, all the four proposed arrangements will offer identical DC-link voltage and are obtained as 396.3 V peak theoretically. Similarly, the theoretical values of boost factor B and voltage gain G are obtained as 6.6 and 5 respectively.

5.1. Simulation results

The simulations of capacitor voltages along with input current are depicted in Figure 7 for all the four presented topologies. It is also detected from Figure 7(a) that the inrush current and capacitor stresses are less when compared to other three novel arrangments at similar boost factor. In Figure 7 (b), due to its structure the stress across C_1 is increased. The capacitor C_2 stress is increased in Figure 7 (c), but this stress is decreased to some extent in Figure 7 (d). Therefore, type-1 shown in Figure 7 (a) is taken as an example to extract other simulation results.

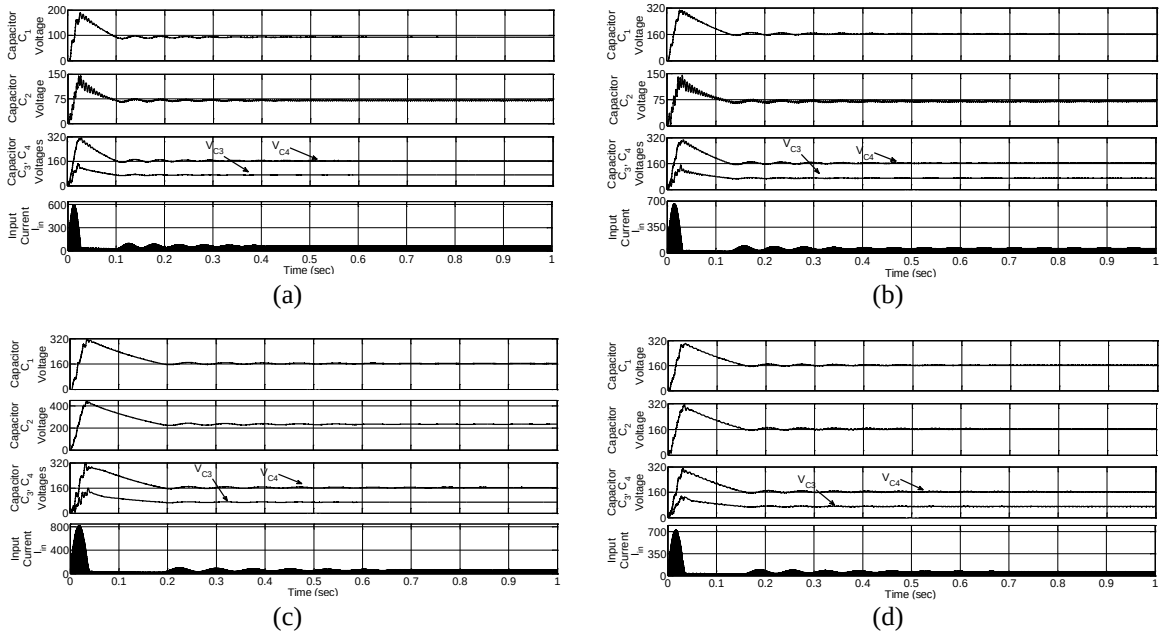


Figure 7. Simulation results of voltage across the capacitors (top) and input current (bottom) for (a) type-1, (b) type -2, (c) type -3, and (d) type -4

Figure 8 (a) displays the input voltage V_{DC} and diode (D_1/D_2, D_3/D_4, and D_{in}) voltages. In shoot-through state, D_3 and D_4 are conducting; consequently, the voltage across them is zero. Likewise, during non-shoot-through, the diode D_{in}, D_1, and D_2 are conducting state; therefore, the voltage across them is also zero. The steady-state peak DC-link voltage, and currents through inductor, diode D_{in}, and DC-link repectively are shown in Figure 8 (b). The dc-link voltage is zero in shoot-through state due to short across the inverter bridge and is peak value of about 395 V in non-shoot-through state. The inductor current is increasing in shoot-though state which implies that the inductors are charging, in non-shoot-though state, the current flowing through inductor is decreasing in order to discharge the inductors. As portrayed in bottom of Figure 8 (b), the dc-link current which is similar as input current and is discrete. In case of SBC, in zero-state, the current is zero and during shoot-though and active states the current is non-zero. Therefore, to avoid discontinuous in the input current, maximum boost control method can be used [25] in which all the zero states are used as shoot-through states and also increases the voltage boost.

Figure 9 (a) depicts the steady-state simulations results of ac-side output voltages (V_{ab} and V_{an}) and phase currents of the presented topology without LC filters. The AC-side line voltage, phase voltage and

phase current with LC filters of L_f = 1 mH, C_f = 20 µF at output side are shown in Figure 9 (b). It is realized from this figure that, the line and peak phase voltages are about 280 V and 160 V (i.e., 110 V rms) respectively.

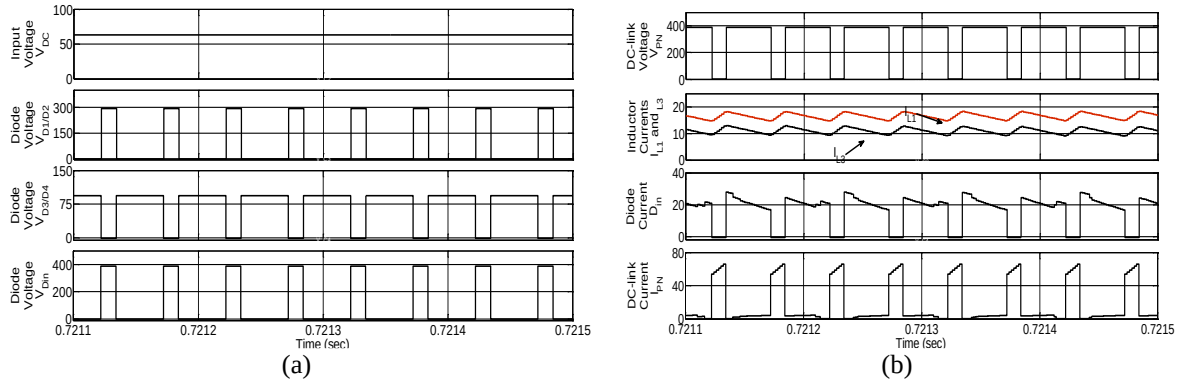


Figure 8. From top to bottom, simulation results (a) input voltage and diode voltages and (b) DC-link voltage, and inductor, diode and DC-link currents

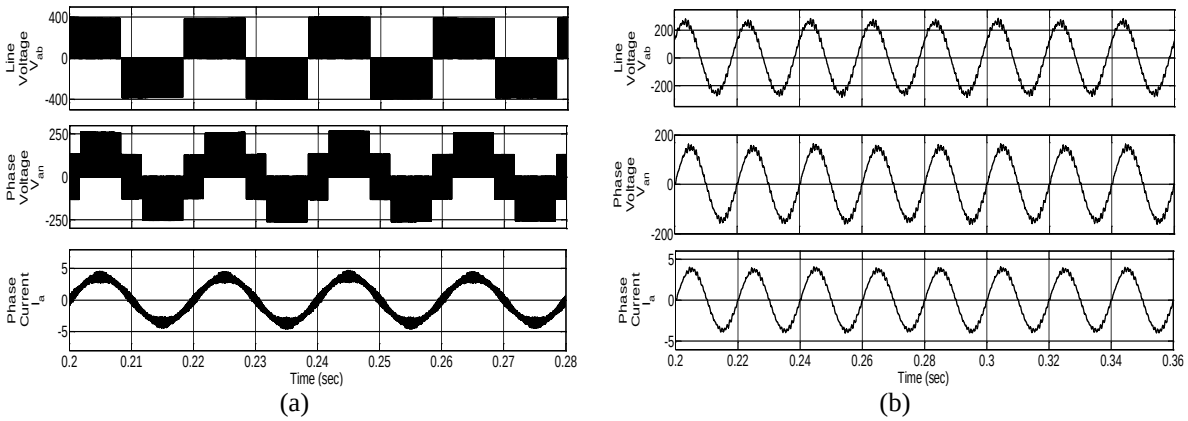
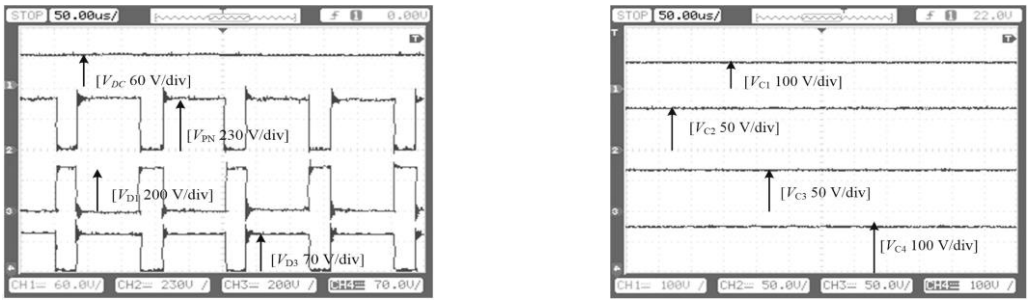


Figure 9. From top to bottom, simulation results of AC-side voltages and currents (a) without LC filter and (b) with LC filter

5.2. Experimental results

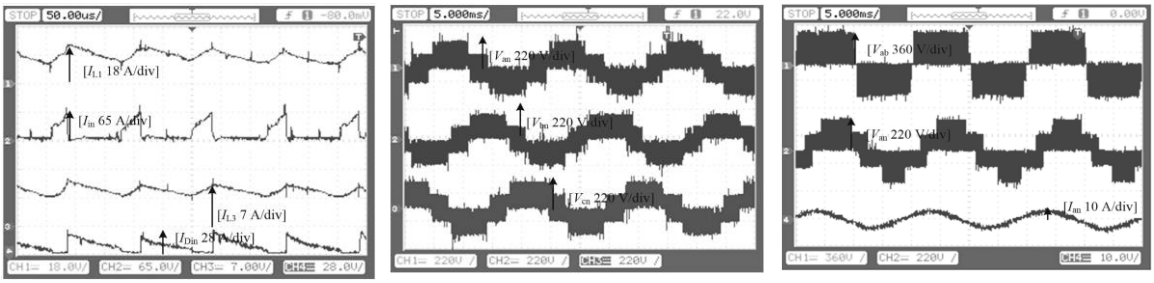
To validate the simulation results, the experimental test is conducted in the laboratory with the same parameters. The input voltage along with DC-link voltage and diode voltages are depicted in Figure 10 (a). The peak DC-link voltage and diode D_1 voltages are boosted to 382 V and 285 V respectively. The diode D_3 voltage is boosted to 89 V in non-shoot-through state and is almost zero in shoot-through state. Figure 10 (b) shows the steady-state capacitor C_1, C_2, C_3, and C_4 voltages. From these figures it is seen that due to drop across the diodes, inductors and switches; the experimental values are slightly less when compared to simulation values.

Figure 11 (a) depicts the inductor L_1 and L_3 currents along with input I_{in} and diode D_{in} currents. It is observed that the inductor currents are increasing linearly in shoot-through state and it is decreasing linearly in non-shoot-through state, which represents charging and discharging of the inductors respectively. It can be seen from this figure that the input current (same as dc-link current) is zero during zero state and it is non-zero in other states (i.e., during shoot-through state and active states). Figure 11 (b) depicts the phase voltages (i.e., V_{an}, V_{bn}, and V_{cn}) of three-phase system at M = 0.75888. The line voltage, phase voltage and the phase current are also obtained in Figure 11 (c) and it seen that the magnitude of voltages are less when compared to simulation and theoretical values.



(a) (b)

Figure 10. From top to bottom, hardware test results of (a) input, dc-link and diode voltages and (b) capacitor voltages



(a) (b) (c)

Figure 11. From top to bottom, experimental results of (a) inductor, input and diode currents, (b) ac-side voltages and (c) ac-side voltages and currents

6. CONCLUSION

This paper presents a new family of four different configurations of enhanced-boost quasi-Z-source inverters which provides discrete input current. The projected configurations provide very high voltage boost at high modulation index which results into high quality waveforms. Moreover, these configurations share common ground with input source and VSI bridge to diminish leakage current problem. In addition, the proposed topologies reduce the capacitors stress and inrush current problem. Among all these four proposed topologies, type-1 DIC EB-qZSI has more advantage, like less inrush current and less capacitor stress. The steady-state process, and the derivation of boost and capacitor voltages are given for both continuous and discontinuous conduction modes. The simulation and experimental test results have been verified with the theoretical expressions.

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