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Maximum resolution of switched capacitor converter: a graphical approach

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ABSTRACT

The efficiency of a switched capacitor converter can be represented as the ratio of the output voltage to open-circuit voltage. Switched capacitor converters with adjustable gain are designed with multiple no-load voltages to obtain higher efficiency over the voltage control range. This paper aims to realize the maximum resolution of a switched capacitor converter. A graphical representation of the output voltages formation has been proposed. The voltage composition diagram reveals a switching pattern of the multiphase operation cycle that leads to the desired output voltage. The proposed method has been applied to determine all possible output voltage levels that lead to maximum resolution. A three-capacitor converter has been controlled with the proposed scheme. The simulation results show that the output voltage follows the reference voltage closely. The converter provides 60% more output voltage steps compared to the nearest comparable design in the literature.

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1. INTRODUCTION

DC-DC converters are receiving an increased attention due to their role in numerous applications [1]–[7]. The switched capacitor converter (SCC) has the advantage of being an inductor-less design [8], [9]. Most of the power converters use inductors and the SCC is limited to low power applications with fixed voltage gain [10]–[13]. Advantages of inductor-less design include low electromagnetic interference, high power density, suitability for IC fabrication, and more tolerance to temperature rise. On the other hand, the SCC usually applies a large number of switching devices and the converter's efficiency drops considerably when the gain is regulated [14]–[17].

The output voltage of an SCC can be attenuated from the maximum no-load voltage by adjusting the switching frequency or by modulating blanking intervals [18], [19]. The nominal efficiency of the SCC is equal to the ratio of the regulated to no-load voltages ($V_o/V_{o,OC}$). This is similar to the efficiency of the circuits that use a variable resistor or linear regulator. Therefore, voltage regulation is avoided, and the SCC is generally used as a constant gain converter, except for low power circuits [20], [21].

With reasonable efficiency, many researchers have introduced SCC designs based on multiple no-load voltages. The ratio ($V_o/V_{o,OC}$) can be maximized by operating the converter to produce the minimum sufficient open circuit voltage. Changing the no-load voltage is generally achieved by modifying the switching signals according to the desired output voltage. The challenge of this approach is to maximize the number of available output voltage levels for a given number of elements [22]–[25]. To produce multiple no load voltages, some designs suggested converters with multiple unequal voltage sources [24]–[26]. This option is overlooked in this work due to the added cost of multiple sources. Other designs use low frequency switches to reconfigure

the converter circuit manually and hence adjust the converter gain. This method increases the circuit size considerably as it is usually based on implementing multiple stages and topologies. For a given gain, the active topology is determined by controlling the low frequency switches and applying a two-phase operation cycle to energize the circuit [27], [28].

A multiple-phase cycle applied to a flying capacitor SCC has been used to provide multiple no-load voltages [29]. By assigning binary ratio of the capacitor voltages, it has been shown that the *n* capacitor converter can produce 2^n-1 voltage levels. In a subsequent study, it has been shown that the capacitor voltage ratio based on Fibonacci series can add more no-load voltages [23].

Aiming to enhance the SCC's efficiency by providing the maximum number of no-load voltages, this paper introduces a graphical comprehension of the converter states. This technique is applied to a step-down, cascaded H-bridge flying capacitor converter and can be equally applied to other SCC topologies. Achieving the maximum number of no-load SCC voltages is presented as the contribution of this work. The possible gain values are identified, and the conditions required to operate the converter with a specific gain are outlined. Compared to previous studies using equivalent topology, new values of gain have been obtained which enhances the efficiency of the converter over the operation range. The paper is organized as shown in: section 2 presents a theoretical background, Section 3 presents the simulation verification and a comparison to other studies. Section 4 discusses the redundant states incident and formulates states selection optimization guidelines and section 5 presents the conclusion.

2. GENERAL SCC AND STABILITY CONDITIONS

An SCC uses capacitors and switches to perform the voltage conversion function. In basic SCC, known as the charge pump, the switching cycle is divided into two phases: the charging phase and the delivery phase. With *N* capacitors, the series/parallel connections lead to conversion ratio of *N* and 1/*N* for the step up and step-down modes respectively. Different series-parallel combinations lead to other conversion ratios [30].

2.1. SCC configuration and output voltage equation

This work discusses the SCC with three flying capacitors connected in series through H-bridges modules, as shown in Figure 1. Each capacitor can be connected directly, inversely, or bypassed through its H-bridge module. So, the output voltage can be represented as:

$$V_{out} = a_0 V_i + \sum_{k=1}^{3} a_k . V_{Ck}, \quad (1)$$

where a_o is the switching function of complementary switches Qo and Qo', and a_k is the gain of the *k*-th H-bridge; so:

$$a_o \epsilon \{0,1\}, a_k \epsilon \{-1,0,+1\} \quad (2)$$

As shown in (1) (a_0, a_1, a_2, and a_3) represent the control parameters, while the resultant voltages (V_{C1}, V_{C2}, V_{C3}, and V_{out}) represent the variables.

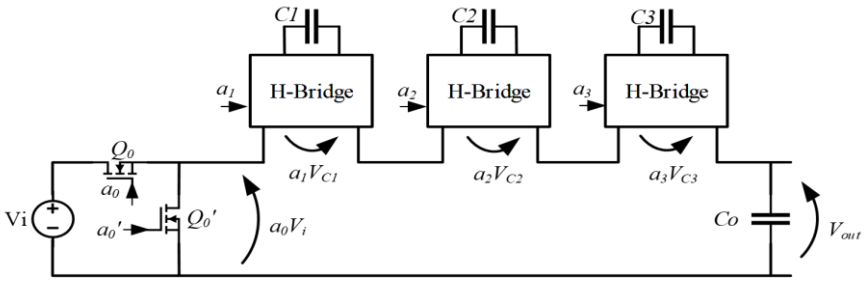

Figure 1. A general three-capacitor step-down SCC

When the switching frequency is high enough, the capacitors voltages would remain almost constant throughout the operation cycle. By dividing the switching period into *r*-intervals and imposing different set of switching variables (a_0-a_3) within each interval, the output voltage will be represented by *r* different equations. The matrix form of the resultant equations is given in (3).

$$\begin{bmatrix} a_{0,1} & a_{1,1} & a_{2,1} & a_{3,1} \\ a_{0,2} & a_{1,2} & a_{2,2} & a_{3,2} \\ & \vdots & & \\ a_{0,r} & a_{1,r} & a_{2,r} & a_{3,r} \end{bmatrix} \begin{bmatrix} V_i \\ V_{c1} \\ V_{c2} \\ V_{c3} \end{bmatrix} = \begin{bmatrix} V_{out,1} \\ V_{out,2} \\ V_{out,3} \\ \vdots \\ V_{out,r} \end{bmatrix} \quad (3)$$

2.2. Stable operation condition

To provide a given output voltage, this voltage needs to be assembled from the supply and capacitor's voltages as indicated in (1). As shown in (3), the output voltage is represented *r* times. The *r* independent and non-conflicting equations specify the output voltage and the voltages of (*r*-1) capacitors. In other words, to determine *r* unknown voltages, the set of linear equations must have a rank of *r*.

The augmented matrix corresponding to (3) is:

$$\begin{bmatrix} a_{0,1} & a_{1,1} & a_{2,1} & a_{3,1} \\ a_{0,2} & a_{1,2} & a_{2,2} & a_{3,2} \\ & \vdots & & \\ a_{0,r} & a_{1,r} & a_{2,r} & a_{3,r} \end{bmatrix} \begin{bmatrix} -V_{out} \\ -V_{out} \\ -V_{out} \\ -V_{out} \end{bmatrix} \quad (4)$$

The feasible sets of the coefficients ($a_{k,j}$: $k \in [0:3]$; $j \in [1:r]$) implies that the rank of the coefficients matrix equals the rank of the augmented matrix.

2.3. Voltage composition diagram

To specify feasible values of capacitor's voltages, consider the case of binary ratio [29] where the k^{th} capacitor voltage is given by:

$$V_{Ck}=2^{-k}V_i \quad (5)$$

Figure 2 shows a graphical representation of the possible output voltage levels corresponding to the case of the capacitors' voltages described in (5). Each stage adds, subtracts, or isolates its capacitor voltage to the voltage of the preceding stages; this is represented by the raising, declining, and horizontal arrows respectively. The resultant output voltage levels are indicated on the right side.

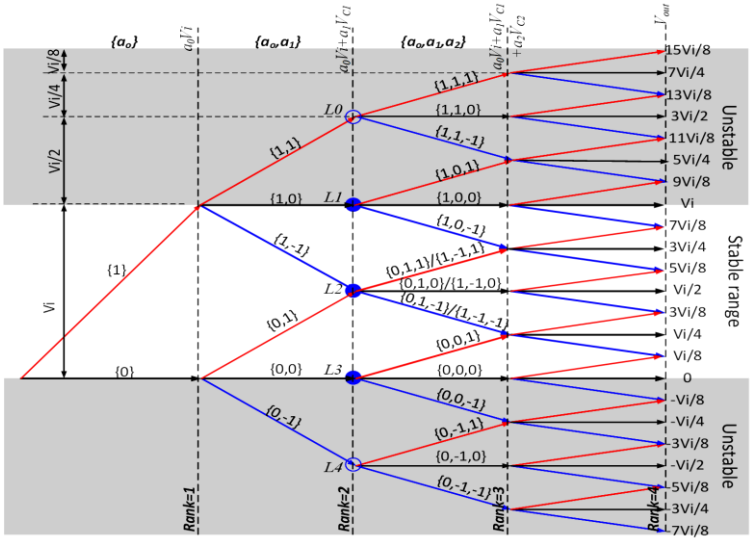

Figure 2. The voltage composition diagram of a 3-capacitor SCC

It appears from Figure 2 that the maximum output voltage is +15*Vi*/8, and the minimum output voltage is –7*Vi*/8. However, to maintain a capacitor's voltage, its average current must be zero. So, the load current must pass in opposite directions during the switching cycle. Therefore, the corresponding switching variable must have +1 besides –1 value within each switching cycle.

In Figure 2, the levels denoted by *L0* and *L4* along the vertical line ($a_0Vi+a_1V_{C1}$) are unstable. These levels are associated with one H-bridge state that leads to unidirectional connection of C1 and results in a unidirectional current with a non-zero average. However, the three levels marked as *L1*, *L2*, *L3* are stable. The stability of the levels marked as *L1* and *L3* is due to the fact the a_1=0 which implies that the capacitor C1 is isolated. As for *L2*, to maintain stability the converter must switch between the two values of a_1: +1 and –1 during the switching cycle in order to reverse the direction of the capacitor current and bring the net charge to zero. Applying the same concept to other capacitors leads to the conclusion that the stable range of the output voltage of the step-down converter is:

$$0 \leq V_{out} \leq V_i \quad (6)$$

The shaded sections in Figure 2 represent the unstable range of the output voltage. To connect the cycle equations' rank to the physical circuit, consider the SCC operation to produce an output voltage of *Vi*/2, which is the same level of point *L2* in Figure 2. The converter, then, has to switch between states (0,1, 0, 0) and (1, –1, 0, 0). In this case, C2 and C3 are isolated and do not affect the output voltage. When substituting (a_0- a_4) in (4) by (0, 1, 0, 0) and (1, –1, 0, 0) and the two variables are V_{C1} and *Vout*, the augmented matrix has a rank of 2; and solving the augmented matrix will lead to the solution: V_{C1} =*Vout* =*Vi*/2. For voltage levels, *Vi*/4 and 3*Vi*/4 (*Vi*/2±*Vi*/4), an augmented matrix of rank 3 is required to determine V_{C1}, V_{C2}, and *Vout*. The four voltage levels (*Vi*/2±*Vi*/4±*Vi*/8) require an augmented matrix of rank 4. In Figure 2, the ranks of various voltage levels are marked on the vertical lines.

2.4. Forming the coefficient matrix

This section presents the formation of the coefficient matrix using the voltage composition diagram with the capacitor's voltages given in (5). Given an output voltage level of rank (*r*), the matrix formation begins by specifying *r's* distinct paths to reach this output voltage. Each path is used to identify the converter state in one of the *r* intervals. Output voltages have ranks of either 2, 3, or 4. Figures 3 (a), 3 (b) and 3 (c) show examples of voltages with ranks 2, 3 and 4 respectively. The switching period will be divided into *r* intervals and the converter will be operated in each state for one interval. The resultant capacitors and output voltages will satisfy the simultaneous equations that have coefficients identified by the *r* paths.

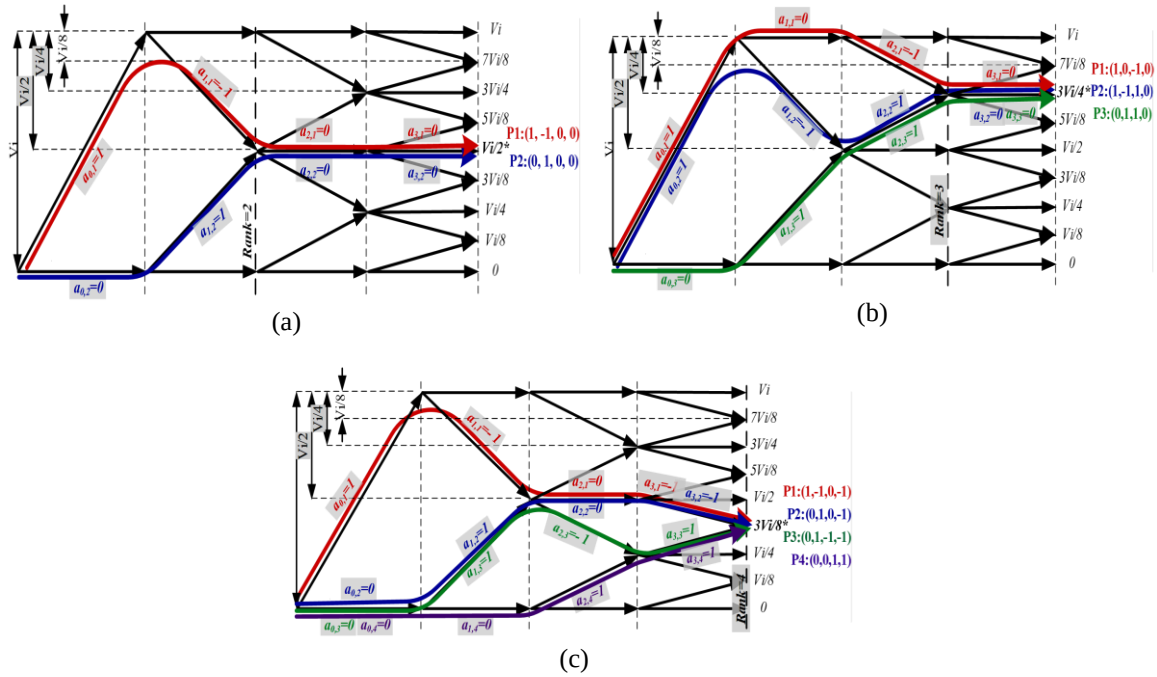

Figure 3. Coefficient matrix formation using *r* (Rank) routes to reach the output voltage, (a) rank=2, (b) rank=3, and (c) rank=4

2.5. Maximum resolution

Based on the graphical representation explained in the previous section, it can be noted that with N – capacitor converter, we can realize any nominal gain (G_{OC}) that can be represented as:

$$G_{OC} = \frac{V_{out}}{V_i} = \frac{m}{n}, m < n \leq 2^N; m, n \, \epsilon Z \quad (7)$$

For instance, the 3-capacitor converter might have any gain which can be represented as a rational number with a denominator that is less than or equal to eight, and a numerator which is less than the denominator. Assigning capacitor's voltage according to (5) provides all gains which can be represented as 2^N fractions (1/8…7/8). To realize fractions of 7, 6, and 5 we need to include the cases with minimum steps of (1/7, 1/6, and 1/5) *Vi* to the basic case described earlier that has a minimum step of (1/8) *Vi*. Notice that other larger fractions are included as multiples of smaller fractions, for instance 1/3=2/6 and so on.

For N-capacitor's converter to achieve a gain that is a multiple of $1/M$ ($2^{N-1} < M \leq 2^N$), the k-th stage capacitor voltage must adhere to:

$$\frac{V_{Ck}}{V_i} = \frac{\lceil M/2^k \rceil}{M}, \quad (8)$$

Where ⌈ ⌉stands for rounding up (or ceiling) function. For example, to have a gain of 5/7 for a 4-capacitor converter, the voltages of the four capacitors are calculated as follows:

– As (7) is less than 2^{4-1}, the gain has to be represented in terms of the 14th fraction rather than the7th fraction, i.e. G_{OC}=5/7=10/14, or M=14
– Apply (8) to all values of k (1-4) to determine the capacitors' voltages:
  k=1, gives $\frac{V_{C1}}{V_i} = \frac{\lceil 14/2 \rceil}{14} = \frac{7}{14}$;
  k=2, gives $\frac{V_{C2}}{V_i} = \frac{\lceil 14/4 \rceil}{14} = \frac{4}{14}$;
  k=3, gives $\frac{V_{C3}}{V_i} = \frac{\lceil 14/8 \rceil}{14} = \frac{2}{14}$
  k=4, gives $\frac{V_{C4}}{V_i} = \frac{\lceil 14/16 \rceil}{14} = \frac{1}{14}$

After specifying the capacitors' voltages, we can identify the r-independent representations of the output voltages by identifying r-distinct paths to the targeted output voltage using the voltage composition diagram. Figures 4 (a), 4 (b) and 4 (c) shows the voltage composition diagram of the 3-capacitor SCC with M=7, 6, and 5 respectively after applying the capacitor voltage selection criterion described in (8). It must be mentioned here that other values of gain are also possible in the presence of switch–controlled possible series/parallel connection of the capacitors [29]. This design, however, has not been taken into account in this study because is spoils the SCC modular structure and requires a large number of switches.

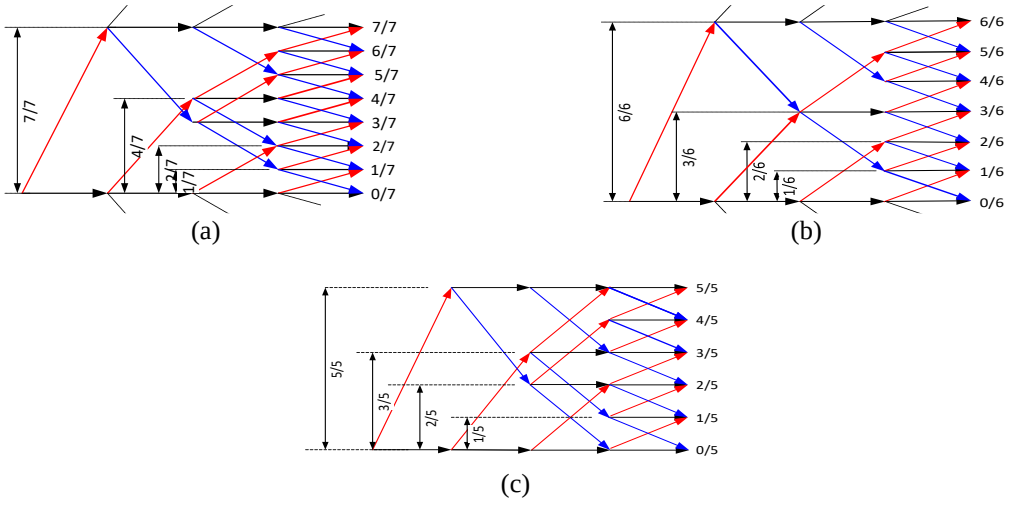

Figure 4. Voltage composition diagrams including capacitors' voltage ratios of newly identified gains, (a) gain is a fraction of 7, (b) gain is a fraction of 6, and (c) gain is a fraction of 5

2.6. Forming the switching table

The proposed procedure to define the converter state in the *r* intervals is to use the voltage composition diagram and find *r* paths to certain target gain. The *r* intervals of each possible gain ratio are listed in Table 1 ascendingly. For some gain values, however, the listed intervals are not unique, as the same gain might be realized by another $(r+1)^{th}$ state. For instance, the gain 3/5 can also be realized with state (0, 0, 1, 1) which is not indicated in the table because the number of states involved is limited to *r*. The optimum utilization of redundant states is discussed in Section 4.

Table 1. The switching states over the switching cycle for all values of the gain of the SCC

No-load gain	Rank	States
1/8	4	(0, 0, 0, 1); (0, 0, 1, -1); (0, 1, -1, -1); (1, -1, -1, -1)
1/7	4	(0, 0, 0, 1); (0, 1, -1, -1); (1, -1, -1, 0); (0, 0, 1, -1)
1/6	4	(0, 0, 0, 1); (0, 0, 1, -1); (0, 1, -1, 0); (1, -1, -1, 0)
1/5	4	(0, 0, 0, 1); (0, 0, 1, -1); (0, 1, -1, 0); (1, -1, 0, -1)
2/8	3	(0, 0, 1, 0); (0, 1, -1, 0); (1, -1, -1, 0)
2/7	4	(0, 0, 1, 0); (0, 1, -1, 0); (1, -1, 0, -1); (1, -1, -1, 1)
2/6	4	(0, 0, 1, 0); (0, 1, -1, 1); (0, 1, 0, -1); (1, -1, 0, -1)
3/8	4	(0, 0, 1, 1); (0, 1, 0, -1); (0, 1, -1, 1); (1, -1, 0, -1)
2/5	4	(0, 0, 1, 0); (0, 1, 0, -1); (1, -1, 0, 0); (1, 0, -1, -1)
3/7	4	(0, 0, 1, 1); (0, 1, 0, -1); (1, -1, 0, 0); (0, 1, -1, 1)
4/8	2	(0, 1, 0, 0); (1, -1, 0, 0)
4/7	4	(0, 1, 0, 0); (1, 0, -1, -1); (1, -1, 0, 1); (1, -1, 1, -1)
3/5	4	(0, 1, 0, 0); (1, -1, 0, 1); (1, 0, -1, 0); (1, -1, 1, -1)
5/8	4	(0, 1, 0, 1); (0, 1, 1, -1); (1, 0, -1, -1); (1, -1, 1, -1)
4/6	4	(0, 1, 0, 1); (0, 1, 1, -1); (1, 0, -1, 0); (1, -1, 0, 1)
5/7	4	(0, 1, 0, 1); (0, 1, 1, -1); (1, 0, -1, 0); (1, -1, 1, 0)
6/8	3	(0, 1, 1, 0); (1, 0, -1, 0); (1, -1, 1, 0)
4/5	4	(0, 1, 0, 1); (1, 0, 0, -1); (1, -1, 1, 0); (1, 0, -1, 1)
5/6	4	(0, 1, 1, 0); (1, 0, 0, -1); (1, -1, 1, 0); (1, 0, -1, 1)
6/7	4	(0, 1, 1, 0); (1, 0, 0, -1); (1, -1, 1, 1); (1, 0, -1, 1)
7/8	4	(0, 1, 1, 1); (1, 0, 0, -1); (1, 0, -1, 1); (1, -1 ,1 ,1)

3. SIMULATION RESULTS

The CSS circuit has been simulated using Simulink® and the converter model is shown in Figure 5. The switching table is identified using a 3-D lookup table. Other model parameters are listed in Table 2. The controller is designed to operate the converter to have a no-load gain which is right above the desired gain the desired gain. To verify all the values of gain listed in Table 1, a reference gain that changes from 0.1 to 0.86 in 21 steps is applied. The step time is 0.1 sec. The converter response over the simulation interval is shown in Figure 6. The reference and resultant output voltages are shown in Figure 6 (a); the three capacitors' voltages are shown in Figure 6 (b) and the converter's efficiency is shown in Figure 6 (c).

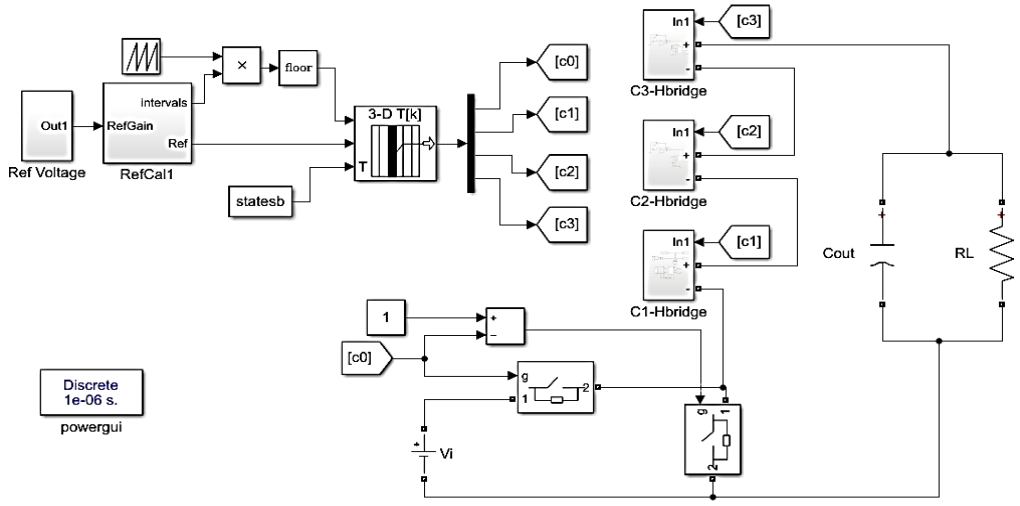

Figure 5. Simulink model of the three-capacitor SCC

Table 2. SCC Simulink model parameters

Parameter	Value (Unit)
Input voltage: Vi	100 (V)
Switching frequency: fsw	20 (kHz)
Converter Capacitors: C1, C2, C3	1 (μF)
Converter Capacitor ESR	0.01 (Ω)
Load Capacitor: Cout	100 (μF)
Load resistance: R	1000 (Ω)
Switch ON resistance	1 (mΩ)
Switch OFF resistance	100 (MΩ)

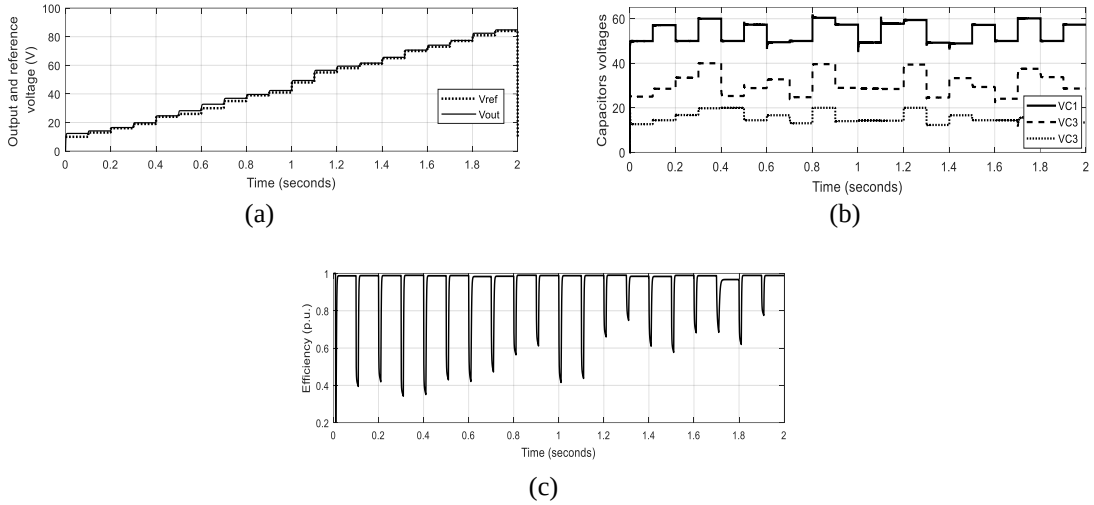

Figure 6. Simulation results of the SCC with a stepped reference voltage, (a) reference and output voltages, (b) the voltages of the three capacitors, (c) the converter efficiency

It can be noticed that the difference between the reference and the resultant output voltage is not more than 2.2 V (2.2% of maximum output voltage). In general, the converter is controlled to produce a no-load output voltage just higher than the reference voltage. As the gain increases, the difference between the actual output voltage and the no-load voltage increases due to higher load current.

Figure 6 (a) shows that the transition between subsequent output voltages is smooth and without considerable delay or overshoot. The variation of the capacitors' voltages for various values of output voltage is shown in Figure 6 (b). The change of a capacitor's voltage causes energy loss that results in a temporary efficiency drop, as shown in Figure 6 (c). The energy loss is proportional to capacitance and to the square of the voltage variation.

The three capacitors' voltages vary by changing the reference voltages to a different fraction (denominator). These voltages change to satisfy the design voltages given in (8). Figure 7 shows the values of the three capacitors voltages and the corresponding gains have been indicated. The gains with the same numerator have been marked with the same background shading. It can be seen in Figure 7 that the gains of $m/8$ have$V_{C1}=4Vi/8$, $V_{C2}=2Vi/8$, and $V_{C3}= Vi/8$. The gains of $m/7$ have $V_{C1}=4Vi/7$, $V_{C2}=2Vi/7$, and $V_{C3}= Vi/7$. The gains of $m/6$ have$V_{C1}=3Vi/6$, $V_{C2}=2Vi/6$, and $V_{C3}= Vi/6$. And the gains of $m/5$ have$V_{C1}=3Vi/5$, $V_{C2}=2Vi/5$, and $V_{C3}= Vi/5$; where m is a positive integer that is less than the denominator.

By examining the steady-state efficiency of all gains in Figure 6 (c), it can be noticed that efficiency is higher than 97.5% except for the interval 1.7-1.8 sec of the simulation time. During that interval, the efficiency is about 96.5%, which is about 2% below the average efficiency. Notice that in this interval, the nominal gain is 0.8 (4/5) while the actual output voltage is about 77 V. This phenomenon is discussed in more detail in Section 4.

Compared to the fundamental limit of the number of levels given in [30], it can be seen that the possible number of levels described in (7) is much larger and it is exponentially-related to the number of SCC capacitors. This increase is mainly due to the multiple-phase cycle compared to the two-phase cycle consider in [30]. Finally, to show the advantage of this work, Table 3 provides a brief comparison of this work to three comparable previous publications.

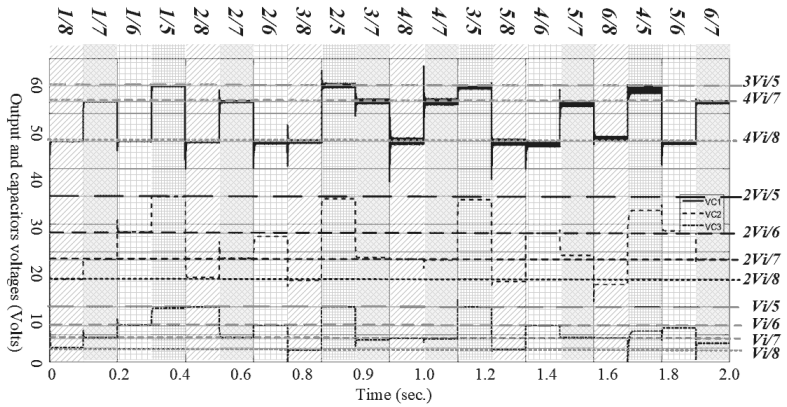

Figure 7. Comparison of the three capacitors voltages at different gains

Table 3. Comparison between the proposed converter and two references

Paper	Number of converter capacitors	Number of switches	Number of output voltage steps
[23]	3	14	13
[27]	8	12	5
[28]	8	16	7
This paper	3	14	21

4. OPERATION WITH REDUNDANT STATES

In this section, optimum states will be sought by discussing the minimum efficiency conduction experienced at gain= 4/5 in Figure 6 (c). By referring to Figure 4 (c), it can be seen that there are 5 possible paths to this gain, as shown in:

P1: (0, 1, 0, 1)
P2: (0, 1, 1, -1)
P3: (1, 0, -1, 1)
P4: (1, -1, 1, 0)
P5: (1, 0, 0, -1)

By considering four out of the five paths (P1-P5) for a switching cycle, five different sequences are identified, as listed in Table 4. Note that sequence 5 is unstable because the sign of a_1 is always positive which indicates that the capacitor C1 current is unidirectional. The step response of the other four sequences is shown in Figure 8. A 2.4% efficiency improvement has been achieved in Sequence 4, compared to Sequence 1 as shown in Figure 8. This makes the efficiency of the converter in this state slightly above the average efficiency obtained in Section 3. Figure 9 shows the output voltage step response, which illustrates that the higher efficiency sequence has a lower settling time which has improved from 10msec for Sequence 1 to 2.9 msec for Sequence 4.

In general, to optimize the selection of the states in case that there is a number of paths more than ranks, we need to:

- Minimize capacitor's discharge. Choose the sequence with the maximum number of 1's in its most left digits, i.e. the digits corresponding to (a_o). Accordingly, the shortlist of the sequence given in Table 4 has only sequences 3 and 4. It can be noted from Figure 9 that these two sequences outperform sequences 1 and 2.
- Consider the short-listed sequences after applying the first rule. To minimize the ripple of the resultant voltage, compare the sequences following the order: a_1, a_2, a_3.., and choose the sequence without consecutive similar active states (1 or -1). If there are equivalent states in this respect, move to the next switching variable.

Table 4. Switching sequences that lead to a gain of 4/5

Sequence1	Sequence2	Sequence3	Sequence4	Sequence5 (unstable)
0, 1, 1, -1	0, 1, 1, -1	0, 1, 1, -1	0, 1, 0, 1	0, 1, 1, -1
0, 1, 0, 1	0, 1, 0, 1	1, -1, 1, 0	1, -1, 1, 0	1, 0, -1, 1
1, 0, -1, 1	1, -1, 1, 0	1, 0, 0, -1	1, 0, 0, -1	0, 1, 0, 1
1, -1, 1, 0	1, 0, 0, -1	1, 0, -1, 1	1, 0, -1, 1	1, 0, 0, -1

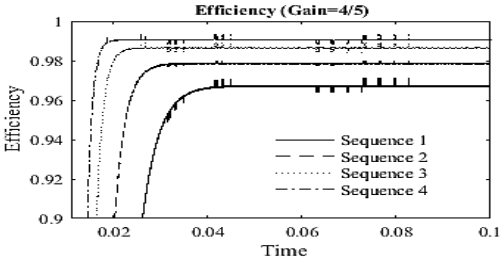

Figure 8. SCC efficiency variation during a stepped change in the gain from 0 to 4/5, for the four feasible switching sequences

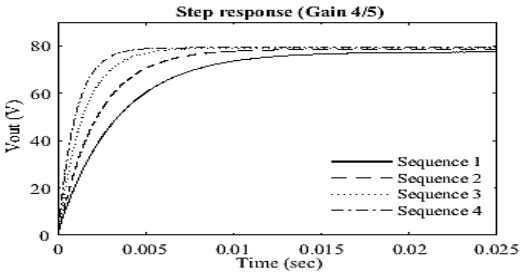

Figure 9. SCC output voltage variation during a stepped change in the gain from 0 to 4/5, for the four feasible switching sequences

5. CONCLUSION

With a multi-phase cycle operating, the SCC can provide a larger number of no-load voltages without adding elements, as compared to the two-phase cycle converters. This paper introduced the following developments to the multiphase flying capacitor SCC: i) A graphical approach to represent the capacitors and output voltages is introduced and the resultant voltage composition diagram is used to develop the switching cycle for a given open circuit gain; ii) The Maximum number of achievable voltage levels have been identified and verified; iii) The voltage ratios of the individual capacitors for all gains to realize the maximum voltage levels have been presented for any number of capacitors; vi) To optimize the use of redundancy, guidelines for states' selection have been furnished and verified by simulation.

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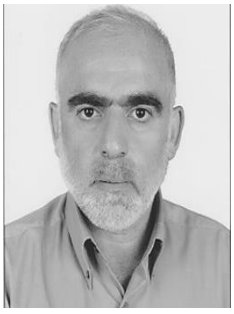

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