A new zero voltage transition interleaved flyback converter

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ABSTRACT

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Keywords:

Flyback converter Interleaved Soft switching ZCS ZVT The paper introduced a new zero voltage transition (ZVT) interleaved flyback converter which has two similar flyback converters. Two flyback converters are in parallel connection and auxiliary circuit in this converter provides ZVT condition for all of the main switches and also provides zero current switching and zero voltage zero current switching (ZVZCS) conditions for the auxiliary switch. Also, ZCS conditions are created for diodes turning off, so reverse recovery problem is solved. The auxiliary circuit in the suggested converter is modular, and by adding parallel branches to the flyback circuit, this circuit can provide soft switching conditions for all switches without significantly change. A complete analysis of the converter is provided and its operating intervals are explained. A 180 W laboratory prototype of the converter is made to approve the theoretical calculations. The experimental results show 7.7% increase in efficiency.

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1. INTRODUCTION

Recently, specifications like as low output voltage, intense power density, quick transient response and high output current have been becoming very significant for the telecommunication power supplies. To achieve the mentioned items, different types of circuit structures are presented [1], [2]. The flyback converter are widely used for low-voltage applications because of low number of elements, simple operation, isolation between input and output [3]. For increasing power density, decreasing input current ripple and providing other advantages such as power distribution, and reduced size of the magnetic elements, the interleaved structure is introduced. However, the conventional interleaved flyback converter has some disadvantages like as high switching losses and low power density. When the switching frequency increases, therefore it causes to reduction volume of the converter [4]. When the switching frequency increases, subsequently it causes difficulties like as switching losses as well as electromagnetic interferences (EMI) for the converter. To eliminate the mentioned difficulties, soft switching methods like new zero voltage transition (ZVT) and zero current transition (ZCT) are used [5]-[9].

The ZVT techniques are more appropriate because of capacitive turn-on losses of MOSFET in ZCT techniques [10]–[12]. In order to converter eliminates switching losses it can be switched softly and DC–DC converters use at too high switching frequency until the volume of the converter reduces [13]–[18]. In [19], the suggested zero voltage switching (ZVS) pulse width modulation (PWM) interleaved flyback converter has many benefits like as uncomplicated control circuit, high output current, high efficiency and low cost. But the leakage inductance in the auxiliary circuit can resonate and increase the diodes voltage stress. In [20], the ZVS condition is achieved in <u>interleaved flyback</u> converter and reverse-recovery losses in the rectifier

diodes are reduced, but the switch voltage is higher than 2Vin. A zero-voltage interleaved buck converter is offered in [21] in which there is an active switch in its auxiliary circuit structure. In suggested converter, each the semiconductor devices achieve soft switching operation but the converter has numerous auxiliary elements and the auxiliary switch has high voltage and current stresses. With two transformers in a ZVS interleaved flyback converter, the over-size problem of the transformer is eliminated and the converter efficiency is prospered. The major demerit of this converter is the dependency of soft switching condition to the load. In such a way that ZVS condition in light load is eliminated [22].

A new interleaved half-bridge flyback converter with ZCT technique in [23] is presented and the efficiency prospered and also the switching-off losses reduced. Parameter variations lead to a power imbalance problem in the proposed ZCS interleaved converter. A ZVS parallel interleaved current-double converter which reduces the current stress and the current ripple is recommended in [24]. Furthermore, on account of the coupling of the output inductors, the number of the output inductors and the output current ripple are decreased. Many numbers of magnetizing components, high conduction losses and duty cycle losses are the disadvantages of the converter. Types of non-isolated converters like as boost, buck, and buckboost are illustrated in [25], [26] in which a conventional auxiliary circuit has applied. The ZVT auxiliary circuit only uses an auxiliary switch which creates soft switching conditions for two main switches of interleaved structure. The most important problem in the suggested circuit [25] is the intense voltage stress in its auxiliary switch, which increases the RDS (on) of the auxiliary switch and as a result increases its conduction losses and converter [26] problems are that the number of auxiliary circuit components is numerous and the voltage stress on the auxiliary switch is measured also intensive.

In this study, a new auxiliary circuit for an interleaved flyback converter has presented so that it can be extended to more parallel branches and because of the low number of elements, soft switching of elements and low circulating current of the auxiliary circuit, this circuit does not inflict considerable losses on the converter. Since all converter diodes also turn off under ZCS conditions, there is no problem of reverse recovery in this converter. For this reason, the efficiency compared to previous converters has increased significantly. In part 2, the ZVT interleaved flyback converter operating analysis is provided. Design technique of the converter is proposed in part 3 and the control circuit of this converter is proposed in part 4. Experimental results of the suggested proposed ZVT interleaved flyback converter have exhibited in part 5. Part 6 compares the efficiency of the ZVT interleaved flyback converter with a conventional interleaved flyback converter.

2. CIRCUIT DESCRIPTION AND OPERATION

2.1. Circuit structure

The introduced converter has exhibited in Figure 1 which is composed of the main switches M_1 and M_2 , the output diodes D_{o1} and D_{o2} , output filter capacitor C_o , two isolating transformers which consist of primary windings L_{p1} and L_{p2} , leakage inductances L_{k1} and L_{k2} , and secondary windings L_{s1} and L_{s2} . The auxiliary circuit has an auxiliary switch M_a , auxiliary inductor L_a , auxiliary diodes D_a and D_b , and auxiliary winding L_b coupled to the main winding, a capacitor C_b , snubber diodes D_{s1} and D_{s2} , and snubber capacitor C_s . The first isolating transformer includes the primary winding L_{p1} , the secondary winding L_{s1} and the auxiliary winding L_b . The second isolating transformer includes the primary winding L_{p2} and the secondary winding L_{s2} . The turn ratio of L_{s1}/L_{p1} is $n_{s1}/n_{p1}=n$ and the turn ratio of L_{s2}/L_{p2} is $n_{s2}/n_{p2}=n$.





2.2. Operating of the suggested converter

The checking of the suggested converter can be simplified, therefore the following assumptions have presented: i) All elements design ideal; ii) The capacitor C_o has a large value, in order that the output voltage can be fixed; iii) The Capacitor C_b has a large value, in order that its voltage can be fixed and identical to V_{cb} ; and iv) Magnetizing inductances L_{m1} and L_{m2} are same and large, thus the current I_{Lm} is considered fixed: $L_{m1}=L_{m2}=L_{m}$.

To evaluate the suggested converter, the first 9 intervals of the converter are fully analyzed. The equivalent circuit of each of the 9 intervals has exhibited in Figure 2. Figure 3 indicates the key waveforms of the operating intervals. Before the interval 1: It can be presumed that the main switches M_1 and M_2 are off and diodes D_{o1} , D_{o2} and D_b are on and transmit current, and so the snubber capacitor voltage V_{Cs} is identical to $V_{in}+V_o/n$ and the capacitor voltage V_{Cb} is identical to mV_o .



Figure 2. Equivalent circuit of the operation intervals: (a) Interval $1[t_o-t_1]$, (b) Interval $2[t_1-t_2]$, (c) Interval $3[t_2-t_3]$, (d) Interval $4[t_3-t_4]$, (e) Interval $5[t_4-t_5]$, (f) Interval $6[t_5-t_6]$, (g) Interval $7[t_6-t_7]$, (h) Interval $8[t_7-t_8]$, and (i) Interval $9[t_8-t_9]$

Interval 1 [t_o - t_I]: At the beginning, the auxiliary switch M_a turns on under ZCS condition, because an auxiliary inductor L_a with the auxiliary switch M_a are in series. Because of the output diodes D_{o1} and D_{o2} conduct, the constant voltage mV_o+V_o/n is placed across L_{k1} and L_a and also across L_{k2} and L_a . Therefore, the snubber circuit diodes D_{s1} and D_{s2} start to conduct and the auxiliary switch current I_{Ma} increases linearly. Since the values of L_{k1} and L_{k2} are small, in this interval snubber capacitor voltage V_{Cs} has considered constant and identical to $V_{in}+V_o/n$, therefore the auxiliary switch current I_{Ma} is calculated from (1).

$$I_{Ma}(t) = \frac{V_0(m+\frac{1}{n})}{L_a}(t-t_0)$$
(1)

$$n = \sqrt{\frac{L_{s1}}{L_{p1}}} = \sqrt{\frac{L_{s2}}{L_{p2}}}$$
(2)

$$m = \sqrt{\frac{L_b}{L_{s1}}} \tag{3}$$

By increasing the auxiliary switch current I_{Ma} , current in output diodes D_{o1} and D_{o2} is reduced and when the auxiliary switch current I_{Ma} achieves I_{Lml} + I_{Lm2} , the output diodes D_{o1} and D_{o2} turn off with ZCS and current mode finishes. Duration of this mode is:

$$\Delta t_1 = t_1 - t_0 = \frac{2I_{Lm} L_a}{V_o(m + \frac{1}{n})}$$
(4)



Figure 3. Key waveforms of the suggested ZVT interleaved flyback converter

Interval 2 [t_1 - t_2]: The output diodes D_{o1} and D_{o2} turn off under ZCS condition as soon as the interval starts and then the snubber capacitor C_s begins to resonate with L_a and its energy has transferred to capacitor C_b . Important equations of this interval are:

$$I_{Ma}(t) = \frac{V_o(m + \frac{1}{n})}{Z_o} sin(w_o(t - t_1)) + 2I_{Lm}$$
(5)

A new zero voltage transition interleaved flyback converter (Zahra Peiravan)

$$V_{Cs}(t) = V_0 \left(m + \frac{1}{n} \right) \cos(w_0 (t - t_1)) + (V_{in} - mV_0)$$
(6)

where:

$$Z_o = \sqrt{\frac{L_a}{C_s}} \tag{7}$$

$$\omega_o = \frac{1}{\sqrt{L_a C_s}} \tag{8}$$

Because the anode voltage of D_b is less than $(V_{in}+V_o/n)/2$, the resonance stops after half a cycle and at the finale of this interval the capacitor C_s has fully discharged and this mode ends. Then, the duration of current interval can be derived:

$$\Delta t_2 = t_2 - t_1 = \pi \sqrt{L_a C_s} \tag{9}$$

Interval 3 $[t_2-t_3]$: With complete discharge of C_s , the body diodes of the main switches M_1 and M_2 (D_{b1} and D_{b2}) start to conduct under ZV. Therefore, the constant voltage V_{in} - mV_o is reversed across the auxiliary inductor L_a and the auxiliary switch current I_{Ma} reduces linearly. The main switch M_1 can turn on with zero-voltage. This interval ends by turning the body diodes of the main switches M_1 and M_2 (D_{b1} and D_{b2}) off. Whenever the auxiliary inductor current I_{La} is identical to $I_{Lm1}+I_{Lm2}$, the body diodes of the main switches M_1 and M_2 (D_{b1} and D_{b2}) off. Whenever the auxiliary inductor current I_{La} is identical to $I_{Lm1}+I_{Lm2}$, the body diodes of the main switches M_1 and the duration of this interval:

$$I_{Ma}(t) = I_{Ma}(t_2) - \frac{V_{in} - mV_o}{L_a}(t - t_2)$$
⁽¹⁰⁾

$$\Delta t_3 = t_3 - t_2 = \frac{I_{Ma}(t_2) L_a}{V_{in} - mV_o}$$
(11)

Interval 4 [t_3 - t_4]: Current transmission from the body diode of the main switch M_1 to the main switch M_1 occurs and increases linearly with the same slope and the body diodes of the main switches M_1 and M_2 (D_{b1} and D_{b2}) turn off with ZCS. While the current of the main switch M_1 achieves I_{Lm1} , finally the snubber diode D_{s1} turns off with ZCS. The main switch current I_{M1} and the time of this interval are derived from (12)-(13).

$$I_{M1}(t) = \frac{V_{in} - mV_o}{L_a}(t - t_3)$$
(12)

$$\Delta t_4 = t_4 - t_3 = \frac{I_{Lm} L_a}{V_{in} - mV_o}$$
(13)

Interval 5 $[t_4-t_5]$: This interval starts as soon as the snubber diode D_{s1} turns off and the I_{Lm2} current charges the capacitor C_s linearly. Also, current of the auxiliary switch M_a achieves zero and the auxiliary switch M_a turns off under ZVZC condition on account of the presence of capacitor Cs and the auxiliary circuit entirely exits from the converter. Also the current of the main switch M_1 is fixed and identical to I_{Lm1} .

Interval 6 [t_5 - t_6]: In this mode, while the C_s capacitor voltage achieves to $V_{in}+V_o/n$, the snubber diode D_{s2} turns off and the diode D_{o2} conducts, and the magnetizing inductance L_{m2} starts discharging to the the output. Interval 7 [t_6 - t_7]: Interval 7 occurs simultaneously as the main switch M_1 is turned off, and the magnetizing inductance L_{m1} charges the snubber capacitor C_s and the output diode D_{o1} has also turned on under ZCS condition. The equation of duration is expressed as:

$$V_{CS}(t) = \frac{I_{Lm}}{c_S}(t - t_5) + (V_{in} - mV_o)$$
(14)

$$\Delta t_6 = t_6 - t_5 = \frac{V_0(m + \frac{1}{n})C_s}{I_{Lm}}$$
(15)

Interval 8 $[t_7-t_8]$: The auxiliary diode D_b turning on occurs at the beginning of this interval. Because both of the main switches M_1 and M_2 are off, the magnetizing inductances are discharged to the output. In this mode, the resonance occurs between the leakage inductance of the transformer L_{kl} and the snubber capacitor C_s and the voltage of the main switch M_l is increased resonating. This interval ends with the complete discharge of the leakage inductance L_{kl} . Finally, the main switch voltage (V_{Ml}) and transformer leakage inductance current (I_{lkl}) expressions for this interval are as follows:

$$V_{M1}(t) = V_{in} + V_0/n + Z_1 I_{Lm} \sin(\omega_1(t - t_6))$$
(16)

$$Z_1 = \sqrt{\frac{L_{k1}}{C_s}} \tag{17}$$

$$I_{Lk1}(t) = I_{Lm} \cos(\omega_1(t - t_6))$$
(18)

Where:

$$\omega_1 = \frac{1}{\sqrt{L_{k1}c_s}} \tag{19}$$

Duration of this interval is:

$$\Delta t_7 = t_7 - t_6 = \pi/2 \sqrt{L_{k1} C_s} \tag{20}$$

Interval 9 [t₈-t₉]: by fully discharging the energy of the transformer leakage inductance L_{kl} and turning snubber circuit diode D_{sl} off under ZCS condition, this interval begins and therefore voltage across the main switch M_l decreases to a fixed amount and identical to $V_{in}+V_o/n$, and similar to a regular flyback converter in off switch mode, both magnetizing inductances are discharged to the output.

3. DESIGN METHOD

In this part, the design of the converter is discussed. The converter has prepared for 300V input voltage, 40V output voltage, and 180W output power. Switching frequency can be selected at 100kHz. The turn ratio of L_b/L_{s1} should be selected in such a way that the anode voltage of D_b is less than $(V_{in}+V_o/n)/2$. If L_b turns is defined as n_b and L_{s1} turns as n_{s1} and L_{s2} turns as n_{s2} , then:

$$V_{A(Db)} = V_{in} - V_{cb} = V_{in} - mV_o$$
(21)

The snubber capacitor C_s is selected like a turn-off snubber capacitor according to (22) and (23) [27].

$$C_s > C_{Smin} = \frac{I_{SW} \cdot t_f}{2 \cdot V_{SW}} \tag{22}$$

$$C_b = \frac{100I_{Lm}D_{Ma}}{mV_o f} \tag{23}$$

It can be presumed that the switch current fall time is indicated by abbreviation t_j , I_{sw} is the switch current before the switch is turned off and V_{sw} is the switch voltage after the switch is turned off. To prove soft switching in practice, the snubber capacitor C_s should be much greater than C_{Smin} . To prove the snubber capacitor C_s discharge, the amount of C_b should be greater than C_s . L_a is designed like a turn-on snubber. For appropriate selection of L_a , there is a relationship between M_a maximum current and D_{max} which can be indicated by:

$$D_{max} = \frac{T - \frac{2I_{Lm}L_a}{V_o(m + \frac{1}{n})} - \pi \sqrt{L_a C_s}}{T}$$
(24)

 L_b should be much greater than L_a . The maximum current and voltage of auxiliary switch M_a are obtained as follows:

$$I_{Ma\ max} = \frac{V_o(m + \frac{1}{n})}{Z_o} + I_{Lm}$$
(25)

$$V_{Ma\ max} = V_o(m + \frac{1}{n}) + \sqrt{\frac{L_a}{C_s}} I_{Lm}$$
⁽²⁶⁾

4. CONTROL CIRCUIT

The closed loop system digital control circuit of the suggested converter is exhibited in Figure 4. A SPARTAN-6 FPGA is selected as the PI digital controller hardware. The output voltage feedback is directed to the analog-to-digital converter (ADC), and then the output of the ADC converter is appraised with the reference voltage (V_{ref}). The error voltage (V_{error}) is directed to the PI digital controller which produces the

necessary control signal. Then this signal is entered to the digital pulse width modulation (DPWM) generator to create the switching gate signals necessary for the three converter switches.



Figure 4. The suggested interleaved flyback converter with implemented digital control circuit

5. EXPERIMENTAL RESULTS

A new ZVT interleaved flyback converter has demonstrated. The picture of the tested converter has exhibited in Figure 5. The design values and components of the converter are exhibited in Table 1. In the Figure 6(a), gating signals waveforms of main switches and auxiliary switch is displayed. The ZV conditions for the main switches are illustrated in Figures 6(b) and 6(c). At the turn on instant of the main switches, their currents are negative and the body diodes are conducting, therefore the main switches can turn on under ZV. The ZCS condition for the auxiliary switch is illustrated in Figure 6(d). The auxiliary switch current increases with the slope, thus the auxiliary switch can turn on with ZCS. The auxiliary switch can turn off with ZVZCS technique. The output diodes are also soft switched as shown in Figures 6(e) and 6(f). The output diodes can turn on and off with ZCS. The operation of this converter is justified by the experimental results.



Figure 5. Picture of the implemented ZVT interleaved flyback converter

Table 1. Design values and components of the suggested converter				
Parameter	Value	Parameter	Value	
Output power (P_o)	180W	Leakage inductances (L_{k1} and L_{k2})	4 μΗ	
Input voltage (V_{in})	300V	Auxiliary inductor (L_a)	5μΗ	
Output voltage (V_o)	40V	Output filter capacitor (C_o)	100µF	
Main switches switching frequency (f_{sw})	100kHz	Filter capacitor (C_b)	10µF	
Load resistance (R_o)	10Ω	Snubber capacitor (C_s)	2.7 nF	
MOSFET power switches (M)	IRFP460B	Turn ratio (n)	0.4	
Power diodes	MUR860	Turn ratio (m)	4	



Figure 6. Experimental waveforms: (a) The measured gaiting signals of the switches M₁ (top), M₂ (middle), M_a (bottom) (voltage: 10 V/div; time: 2.5 µs/div), (b) The measured current (top) and voltage (bottom) of the main switch M₁ (voltage: 200 V/div; current: 2 A/div; time: 1 µs/div), (c) The measured current (top) and voltage (bottom) of the main switch M₂ (voltage: 400 V/div; current: 2 A/div; time: 1 µs/div), (d) The measured current (top) and voltage (bottom) of the auxiliary switch M_a (voltage: 400 V/div; current: 4 A/div; time: 1 µs/div), (e) The measured current (top) and voltage (bottom) of the diode D_{o1} (voltage: 80 V/div; current: 2 A/div; time: 1 µs/div), and (f) The measured current (top) and voltage(bottom) of the diode D_{o2} (voltage: 100 V/div; current: 5 A/div; time: 1 µs/div)

6. EFFICIENCY

Figure 7 shows the suggested ZVT interleaved flyback converter efficiency diagram and as well as the hard switching interleaved converter efficiency diagram. According to Figure 7, both efficiencies are designed for 180 W. The efficiency has measured at 5 various loads and when compared to the hard switching interleaved converter, the efficiency has increased by 7.7%. In Table 2, the losses of the suggested ZVT interleaved flyback converter with a hard switching interleaved flyback sample have compared. In the presented Table, the rise and fall times of the converter switches currents are indicated by abbreviations t_r and t_f , respectively. Also, t_{rr} can be considered as reverse recovery time of the diodes. In addition, C_{out} can define as the switches output capacitance, R_{ds} is supposed equivalent to the switches on state resistance, I_{ave} can be considered as an average current of output and auxiliary diodes, V_F can also be considered as a forward voltage of diodes, and f_{sw} is switching frequency. Furthermore, all semiconductor elements can turn on and off with soft switching technique, accordingly switching losses have significantly declined.



Figure 7. Evaluated efficiency of the suggested ZVT interleaved flyback converter versus conventional hard switching interleaved flyback converter

Table 2. Calculation of losses in hard switching interleaved flyback converter and the suggested ZVT interleaved flyback converter

Kinds of loss	Formula	Hard switching interleaved flyback converter	Suggested converter
Switching loss in M_1	$1/2 V_{sw1} I_{sw1} f_{sw}(t_r + t_f + t_{rr})$	$1/2 \times 400 \times 2.1 \times 40 \times 10^{3} (31 + 56 + 437) \times 10^{-9}$	N.A
Parasitic capacitance loss in M_1	$1/2 C_{out} V_{sw1}^2 f_{sw}$	$1/2 \times 131 \times 10^{-12} \times 400^{2} \times 40 \times 10^{3}$	N.A
Conduction loss in M_I	$R_{ds} I^2_{RMS-M1}$	$0.25 \times (1.65)^2$	$0.25 \times (1.6)^2$
Switching loss in M_2	$1/2 V_{sw2} I_{sw2} f_{sw}(t_r + t_f + t_{rr})$	$1/2 \times 400 \times 2.1 \times 40 \times 10^{3} (31 + 56 + 437) \times 10^{-9}$	N.A
Parasitic capacitance loss in M_2	$1/2 C_{out} V_{sw2}^2 f_{sw}$	$1/2 \times 131 \times 10^{-12} \times 400^2 \times 40 \times 10^3$	N.A
Conduction loss in M_2	$R_{ds} I^2_{RMS-M2}$	$0.25 \times (1.5)^2$	$0.25 \times (1.12)^2$
Switching loss in M_a	$1/2 V_{swa} I_{swa} f_{sw}(t_r+t_f+t_{rr})$	-	N.A
Parasitic capacitance loss in M_a	$1/2 C_{out} V_{swa}^2 f_{sw}$	-	N.A
Conduction loss in M_a	$R_{ds}I^2_{RMS-Ma}$	-	$0.25 \times (2.6)^2$
Conduction loss in diode D_{ol}	V _F I _{avg-Do1}	1.5 ×2.3	1.5×0.8
Conduction loss in diode D_{o2}	V _F I _{avg-Do2}	1.5 ×2.3	1.5×3.4
Conduction loss in diode D_{sI}	V _F I _{avg-Ds1}	_	1.5×0.4
Conduction loss in diode D_{s2}	$V_F I_{avg-Ds2}$	_	1.5 ×0.3
Conduction loss in diode D_a	$V_F I_{avg-Da}$	_	1.5×0.8
Conduction loss in diode D_b	$V_F I_{avg-Db}$	_	1.5×1
Conduction losses of magnetizing	$R_{Lm1} I^2_{Lm1}$	$23.68 \times 10^{-3} \times (0.6)^2$	$23.68 \times 10^{-3} \times (0.8)^2$
inductance L_{m1}			
Conduction losses of magnetizing	$R_{Lm2} I^2_{Lm2}$	$23.68 \times 10^{-3} \times (0.6)^2$	$23.68 \times 10^{-3} \times (0.66)^2$
inductance L_{m2}			
Total loss		26.59 W	12.71 W

7. CONCLUSION

This paper presents a new interleaved flyback converter with a modular auxiliary circuit to produce soft switching conditions for all semiconductor devices. The main switches of the converter operate under ZVT and the auxiliary switch turns off under ZVZC conditions. On the other hand, the input current ripple of the

converter is much less than the regular flyback converter due to its interleaved structure. Because of the a few numbers of components, and low circulating current in the auxiliary circuit, this circuit does not inflict considerable losses on the converter. The practical results of the suggested converter exhibit a 7.7% increment in efficiency at full load versus the hard switching counterpart.

REFERENCES

- M. Z. Hossain, N. A. Rahim, and J. a/l. Selvaraj Jeyraj, "Recent progress and development on power DC-DC converter topology, control, design and applications: A review," *Renewable and Sustainable Energy Reviews*, vol. 81, pp. 205-230, 2018, doi: 10.1016/j.rser.2017.07.017.
- [2] S. A. Gorji, H. G. Sahebi, M. Ektesabi, and A. B. Rad, "Topologies and control schemes of bidirectional DC–DC power converters: An overview," *IEEE Access*, vol. 7, pp. 117997-118019, 2019, doi: 10.1109/ACCESS.2019.2937239.
- [3] M. Delshad, N. A. Madiseh, and M. R. Amini, "Implementation of soft-switching bidirectional flyback converter without auxiliary switch," *IET Power Electronics*, vol. 6, no. 9, pp. 1884-1891, Nov. 2013, doi: 10.1049/iet-pel.2012.0472.
- [4] B. Akhlaghi and H. Farzanehfard, "Soft switching interleaved high step-up converter with multifunction coupled inductors," *IEEE Journal of Emerging and Selected Topics in Industrial Electronics*, vol. 2, no. 1, pp. 13-20, Jan. 2021, doi: 10.1109/JESTIE.2020.3033542.
- [5] A-H. M. Dobi, M. R. Sahid, and T. Sutikno, "Overview of soft-switching DC-DC converters," International Journal of Power Electronics and Drive Systems, vol. 9, pp. 957-967, 2018, doi: 10.11591/ijpeds.v9.i4.pp2006-2018.
- [6] T. Shamsi, M. Delshad, E. Adib, and M. R. Yazdani, "A new simple-structure passive lossless snubber for DC-DC boost converters," *IEEE Transactions on Industrial Electronics*, vol. 68, no. 3, pp. 2207-2214, March. 2021, doi: 10.1109/TIE.2020.2973906.
- [7] E. Gerami, M. Delshad, M. R. Amini, and M. R. Yazdani, "A new family of non-isolated PWM DC-DC converter with soft switching," *IET Power Electronics*, vol. 12, no. 2, pp. 237-244, Feb. 2019, doi: 10.1049/iet-pel.2018.5351.
- [8] N. Anandh, A. Sharma, S. Julius Fusic, and H. Ramesh," An improved zero-voltage zero-current transition boost converter employing l-c-s resonant network," *International Journal of Power Electronics and Drive Systems*, vol. 11, pp. 1844-1856, Dec. 2020, doi: 10.11591/ijpeds.v11.i4.pp1844-1856.
- [9] P. Vu, M. L. Nguyen, and V. P. Pham, "ZVS based on dead-time analysis of three port half bridge converters," *International Journal of Power Electronics and Drive Systems*, vol. 11, pp. 1936-1944, 2020, doi: 10.11591/ijpeds.v11.i4.pp1936-1944.
- [10] Y. Hsieh, T. Hsueh, and H. Yen, "An interleaved boost converter with zero-voltage transition," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 973-978, April. 2009, doi: 10.1109/TPEL.2008.2010397.
- [11] W. Li and X. He, "ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion," *IET Electric Power Applications*, vol. 1, no. 2, pp. 284-290, March. 2007, doi: 10.1049/iet-epa:20060239.
- [12] B. Akhlaghi and H. Farzanehfard, "Efficient ZVT cell for interleaved DC-DC converters," *IET Power Electronics*, vol. 13, pp. 1925-1933, 2020, doi: 10.1049/iet-pel.2019.1102.
- [13] E. Adib and H. Farzanehfard, "Family of zero current zero voltage transition PWM converters," *IET Power Electronics*, vol. 1, no. 2, pp. 214-223, July. 2008, doi: 10.1049/iet-pel:20070225.
- [14] E. Adib and H. Farzanehfard, "Family of zero-current transition PWM converters," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 8, pp. 3055-3063, Aug. 2008, doi: 10.1109/TIE.2008.922597.
- [15] E. Adib and H. Farzanehfard, "Family of soft-switching PWM converters with current sharing in switches," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 979-984, April. 2009, doi: 10.1109/TPEL.2008.2008022.
- [16] I. Aksoy, H. Bodur, and A. F. Bakan, "A new ZVT-ZCT-PWM DC-DC converter," IEEE Transactions on Power Electronics, vol. 25, no. 8, pp. 2093-2105, Aug. 2010, doi: 10.1109/TPEL.2010.2043266.
- [17] E. Adib and H. Farzanehfard, "Zero-voltage transition current-fed full-bridge PWM converter," *IEEE Transactions on Power Electronics*, vol. 24, no. 4, pp. 1041-1047, April. 2009, doi: 10.1109/TPEL.2008.2011553.
- [18] G. Yao, A. Chen, and X. He, "Soft switching circuit for interleaved boost converters," *IEEE Transactions on Power Electronics*, vol. 22, no. 1, pp. 80-86, Jan. 2007, doi: 10.1109/TPEL.2006.886649.
- [19] J. Zhao, H. Zhao, and F. Dai, "A novel ZVS PWM interleaved flyback converter," IEEE Conference on Industrial Electronics and Applications, May 2007, pp. 337-341, doi: 10.1109/ICIEA.2007.4318426.
- [20] Y. Hsieh, M. Chen, and H. Cheng, "An interleaved flyback converter featured with zero-voltage transition," *IEEE Transactions on Power Electronics*, vol. 26, no. 1, pp. 79-84, Jan. 2011, doi: 10.1109/TPEL.2010.2051817.
- [21] M. Esteki, E. Adib, H. Farzanehfard, and S. A. Arshadi, "Auxiliary circuit for zero-voltage-transition interleaved pulse-width modulation buck converter," *IET Power Electronics*, vol. 9, no. 3, pp. 568-575, March 2016, doi: 10.1049/iet-pel.2014.0687.
 [22] A. Thangavelu, V. Senthilkumar, and D. Parvathyshankar, "Zero voltage switching-pulse width modulation technique-based
- [22] A. Thangavelu, V. Senthilkumar, and D. Parvathyshankar, "Zero voltage switching-pulse width modulation technique-based interleaved fyback converter for remote power solutions," *IET Power Electronics*, vol. 9, no. 7, pp. 1381-1390, Jun 2016, doi: 10.1049/iet-pel.2015.0365.
- [23] T. Liang, M. Cheng, W. Huang, and W. Tseng, "Interleaved half-bridge flyback converter with zero-current switching," *IEEE Transactions on Power Electronics*, vol. 34, no. 4, pp. 3370-3383, April 2019, doi: 10.1109/TPEL.2018.2852332.
- [24] Y. Chen, R. Jiang, and R. Liang, "Analysis and design of zero-voltage-switching parallel interleaved current-doubler converters with coupled output inductors," *IET Power Electronics*, vol. 5, no. 4, pp. 467-476, April 2012, doi: 10.1049/iet-pel.2010.0163.
- [25] B. Akhlaghi and H. Farzanehfard, "Family of ZVT interleaved converters with low number of components," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 11, pp. 8565-8573, Nov. 2018, doi: 10.1109/TIE.2018.2808915.
- [26] B. Akhlaghi, M. Esteki, and H. Farzanehfard, "Family of zero voltage transition interleaved converters with low voltage and current stress," *IET Power Electronics*, vol. 11, no. 12, pp. 1886-1893, Oct. 2018, doi: 10.1049/iet-pel.2017.0656.
- [27] W. Mcmurray, "Selection of snubbers and clamps to optimize the design of transistor switching converters," *IEEE Transactions on Industry Applications*, pp. 513-523, 1980, doi: 10.1109/TIA.1980.4503823.

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