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Modified proportional integral controller for single ended primary inductance converter

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ABSTRACT

The article highlights and optimizes a controller for the single ended primary inductance converter (SEPIC) direct current-direct current (DC-DC) converter. The SEPIC converter adjusts a range of dc input voltages and delivers a constant and stable output voltage. Three different models of the SEPIC converter are presented in order to derive its transfer function. Being a 4^{th} order, an approximation method for the reduction of this transfer function to 2^{nd} and 1^{st} order is implemented. Two methods for controlling the converter are presented, the first one is based on guessing techniques and the second explains the design steps of the controller based on the internal model control (IMC). Furthermore, an improvement on the IMC controller is proposed and results were shown and discussed. IMC is based on integrating the "process model" in the control operation of the actual system. By using an approximation of the original transfer function of the system, it is expected that the IMC control will be able to achieve the desired results. Control schemes of the SEPIC will be presented and results will be shown. The response of the controller was tested with mathematical models for batteries and supercapacitors in MATLAB, as non-ideal DC-sources, and results were presented.

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1. INTRODUCTION

It is well known that the switched mode direct current-direct current (DC-DC) converters are used as an efficient way to a regulate a changing DC input voltage thus maintaining a stable DC output voltage. These switched mode power supplies (SMPS) are far efficient than the linear power supplies and they are capable to deliver a higher power density. Relying on solid-state switches such as transistors (mainly metal–oxide–semiconductor field-effect transistors (MOSFET) and insulated-gate bipolar transistor (IGBT)) and diodes and on energy storage components (capacitors and inductors), electrical energy is transferred between the ports of the converter and filtered at its output. Nowadays the application of the SMPS's conquer a wide area from embedded systems to industrial power applications, renewable energy complexes as well as in distributed generation, and smart electrical networks. In general, they are used in most of the technological fields that require very good voltage regulation and reduced losses. To increase the energy efficiency of the enterprises of mineral resource complexes for example, it is essential to construct a power supply system capable of supporting their technical process. Having said that, it is necessary to take into account a number of features inherent in these enterprises, i.e., the possibility to operate remotely from centralized power systems, where the local operational objects are dispersed, for example, those intended for geological exploration, geodetic and other types of work carried out to search, discover and prepare mineral deposits [1]–[6]. Moreover, with

the integration of renewable energy sources and the widespread adoption of the concept of distributed generation, integrating different types of energy sources into one system is becoming more common and profitable in many places. For example, within the framework of the smart grids and energy markets program of the Lappeenranta University of Technology, a project is being developed for a power supply system for rural settlements. The project substantiates the feasibility of replacing overhead alternating current (AC) lines of medium (1 kV) and low (0.4 kV) low voltage direct current (LVDC) voltage development with LVDC cable underground networks (±0.75 kV) [7]. Abramovich and Sychev [1], Abramovich [2] in consider the use of uninterruptible power supply (UPS) systems for mining enterprises on the basis of combining them with alternative and renewable energy sources and multi-step automatic reserve transition systems in order to guarantee a continuous energy supply for mining enterprises consumers. To achieve this task, SMPS's will play an important role in regulating the variations and fluctuations of power delivered by the renewable resources. Belsky *et al*. [5] considered the problem of leveling the load profiles by supplying the grid with energy stored in batteries and supercapacitors through boost and buck-boost converters.

Figure 1 shows a general block diagram of an autonomous power supply system LVDC having different types of power sources and storage devices. One of the main elements that contribute in the establishment of an autonomous power source are energy storage devices (batteries, supercapacitor modules) and DC/DC converters. Since different types of power sources operate in parallel on a unified DC bus system, it is necessary to take into account the presence of equalization currents between the multiple installed sources due to ripples from rectified AC voltages (for example, hydro or wind power sources). Accounting for the variability and change in the input voltage level (photovoltaic (PV) panels and wind generators), will require a well and suited regulation and stabilization of output DC voltage. Therefore, a reasonable choice of DC/DC converters for autonomous power supply applications and the determination of their parameters and the values of their components is an urgent task. Moreover, it is worth to note that due to the switching action implemented in SMPS these converters require a management of the connect/disconnect process. Such management, if achieved precisely, will allow for various types of applications from active filtering implementation to power factor correction and maximum power point tracking (MPPT) control, power shading, and many others. Hence the necessity also to understand the dynamics of DC/DC converters and use them to apply a firm control system.

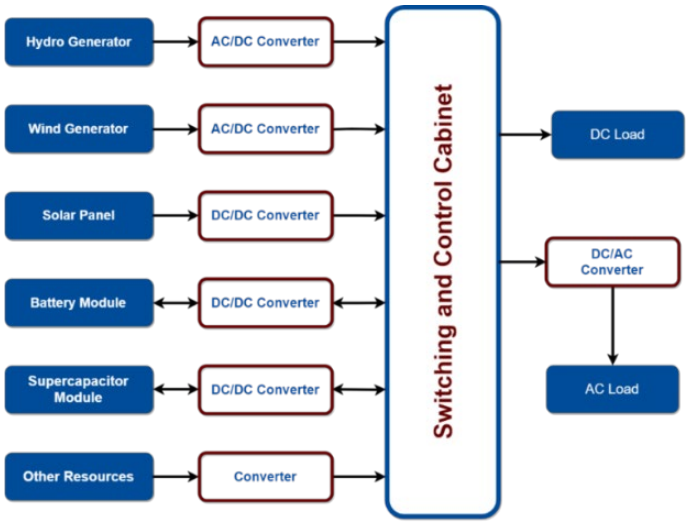


Figure 1. Block diagram of an autonomous power supply system LVDC

The DC/DC power conversion application can be implemented by various circuit topologies [8]. Among them are the basic and most commonly used converters: buck, boost, Cuk, Zeta, and single ended primary inductance converter (SEPIC) converters. Various types of bridgeless converter topologies are discussed in [9]–[29], most of which are based on boost converter configurations. Their main advantage is their low cost. However, they have the following disadvantages [30]: i) lack of isolation of input-output and ii) high ripple current.

The main feature of Cuk, Zeta, and SEPIC converters is that they can operate in both boost and buck mode. The results of comparison of the indicated converters are given in [31]. It is shown that the Cuk converter has a higher level of impulse noise and the duration of the transient process. The characteristics of SEPIC and

Zeta are shown to be almost identical. However, it should be noted that the capacitor filter used for the SEPIC converter was 80 µF, while the capacitor used in the Zeta converter was 120 µF. This suggests that the use of a larger capacitor can improve the quality of the output voltage when used with a SEPIC converter. At the same time, the polarity of the output voltage does not change in the SEPIC converter, which is an advantage over its analogs and provides a beneficial effect when using the microprocessor control of the converter. Converters based on various SEPIC topologies have been discussed and their ability to overcome the above boost converter problems has been shown in [30]–[41]. The analysis and comparison of the operation of various DC/DC converters in a wide power range in [31] showed that by using a SEPIC converter, lower voltage ripple and overshoot values can be obtained. Another advantage of SEPIC is its ability to provide input/output isolation [42].

Among the advantages of the SEPIC converter is its useful application when the operating voltage of the input battery can be higher or lower than the desired regulated output voltage. This feature allowed it to gain popularity among DC storage-powered systems, where the action of boosting or bucking the output voltage is related to the charge level of the storage equipment (ex: battery or supercapacitor). Based on that SEPIC Figure 2 holds many advantages compared to the other classical converters. The complete operation of the converter relies on regulating the output voltage by controlling the duty cycle of the transistor Q_1. However, the transfer function of this converter is of 4th order, besides its operation is characterized by a nonlinear property as all switched mode converters, which introduce difficulty in controlling it.

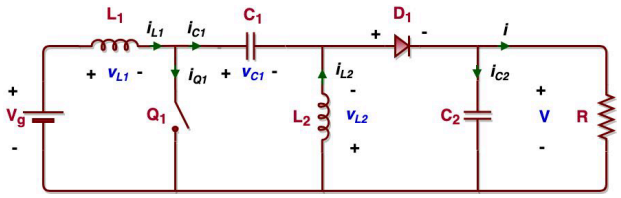


Figure 2. SEPIC converter schematic

Proportional–integral (PI) and proportional–integral–derivative (PID) controllers are well known among the DC/DC digital converters. Such controllers are easily planned for SMPS's. The parameters of such controllers are calculated by applying the approximated or averaged small signal model technique. Our PI controller will be derived from the internal model control method that allows to predict its proportional and integral terms.

PI controller are among linear control techniques that necessitate a decent knowledge of the "plant" under control and a presize tuning to guarantee the achievement of the desired stable results. Therefore, realizing a large-signal stability generally requires "a reduction of the useful bandwidth which affects the converter performances" [42]. As a consequence, the application of the control technique to high order DC/DC converters, e.g., SEPIC topologies, should take into account the critical design of control parameters and the difficulties of stabilization or maneuver. As we will see for example the approximation of the original transfer function should ensure a reliable response of the actual system and no arbitrary approximation shall be implemented.

The availability of a zero in the right half plane of the open loop transfer function of SEPIC converter may lead to some stability problems. Many papers discussed this problem among them the works presented in [6], [43]–[50]. To solve this issue, different control techniques have been proposed among them internal model control (IMC) [49], [50]. IMC is based on integrating the "process model" in the control operation of the actual process/plant. The main idea behind it considers that an ideal control can be attained if the control system comprises a representation of the system (process) under control. We propose that by using an approximation of the original transfer function of this system, it is expected that the reduced transfer function can still represents some of the system's characteristics and dynamics. This reduced order transfer function will be used by the IMC based PI controller to derive its parameters.

2. RESEARCH METHOD

The main idea of the proposed research method is to modify the design of the IMC-based PI controller of a SEPIC converter by integrating a reduced order transfer function representing some of the dynamics of its intial transfer function. To accomplish this task, the following steps shall be implemented: i) Design the SEPIC converter by identifying its main elements according to the required application; ii) Derive its small signal model from the averaged large signal and steady state models; iii) Implement a PI

controller for the converter using the conventional PI controller techniques and the IMC-based PI controller theory; iv) Detect and analyze the performance of the derived controllers; v) Propose a reduced order model of the internal model using the Padé approximation technique and use it to control the converter; vi) Compare the results by analyzing the performance of the original internal model and the reduced order models using bode plot, root locus, and step response methods; vii) Enhance the controller scheme by integrating within its structure the steady state duty cycle; and viii) Test the final result by applying non-ideal voltage sources (battery and supercapacitor) at the input of the converter.

2.1. Control objectives

In this article, two kinds of control have been developed based on PI controller. The first one uses the conventional guessing method to derive the controller parameters. The second one is based on the IMC technique which results in a controller similar in shape to the PI, but uses the circuit known information and tries to mimic the actual system model. In the end an improvement in the control scheme is presented based on achieving a large-signal controller output. The control process applied to the SEPIC converter shall be able to guarantee a stable low impulse output voltage.

2.2. Converter model topology

SEPIC is designed by adding the capacitor C_1 to a boost converter topology between the inductor L_1 and the diode D_1. This capacitor obviously provides isolation between the input side and the output of the converter; thus, it blocks any direct current path. Since, the anode of D_1 must be connected to a defined potential [42], D_1 is pulled to ground via inductor L_2. The switch Q_1 (a MOSFET or an IGBT transistor) controls the energy transfer between the converter ports. Based on the state of Q_1 (open or closed) two circuit schemes are shown in Figures 3(a) and 3(b). Accordingly, we will derive three models for the SEPIC converter [51]: i) The averaged large signal model, ii) The steady state, or the DC-signal model, and iii) The averaged small signal model. The derivation of these models helps us estimating how the converter works, and therefore enables us to decide how to control it.

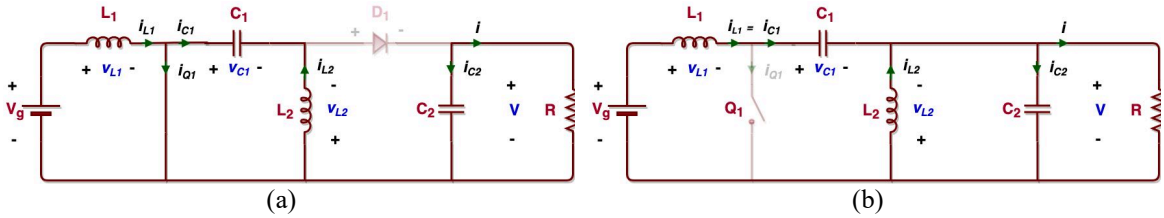


Figure 3. SEPIC analysis (a) -1st subinterval and (b) -2nd subinterval

By applying the method of small ripple approximation, it is possible to design the parameters of the converter by assuming the ripple on the inductors' current ($\Delta i_{L1}, \Delta i_{L2}$) to be no more than 15% and the capacitors' voltage ripple ($\Delta v_{C1}, \Delta v_{C2}$) to be 1%. The ripple limitation in the current of the inductors and the voltage of the capacitors in the SEPIC converter and the choice of the converter switching frequency ($\frac{1}{T}$) are essential for obtaining convenient voltage output and for limiting the size of the components of the converter. So, having decided on the amount of acceptable ripple in these components, the inductance, and capacitance of L_1, L_2, C_1, and C_2 respectively can be determined as:

$$L_1 = \frac{V_g DT}{2\Delta i_{L1}} \quad (1)$$

$$L_2 = \frac{V_g DT}{2\Delta i_{L1}} \quad (2)$$

$$C_1 = \left(\frac{D}{1-D}\right)^2 \frac{V_g T}{2R\Delta v_{C1}} \quad (3)$$

$$C_2 = \left(\frac{D}{1-D}\right)^2 \frac{V_g T}{2R\Delta v_{C2}} \quad (4)$$

where, "D" is the steady state duty cycle for which the semi-conductor switch "Q_1" is ON and the diode "D_1" is OFF within a specific period "T".

2.3. Converter models

As stated earlier, we will be deriving 3 models of the converter, the derivation of these models will help us assessing the relationship between the different variables, and gives us a clear view on how would be the control scheme. We will start in getting the large signal model, which is the general model of the converter. Then we will split it into small signal and steady state models. But first for the sake of simplicity let us consider the following conventions:

$$\dot{v}_1 = \frac{dv_{C1}}{dt}, \dot{v}_2 = \frac{dv_{C2}}{dt}, \dot{i}_1 = \frac{di_{L1}}{dt}, \dot{i}_2 = \frac{di_{L2}}{dt} \tag{5}$$

$$v_2 = v = Output\ Voltage \tag{6}$$

$$d = D + \hat{d} \tag{7}$$

$$v_g = V_g + \widehat{v_g} \tag{8}$$

$$v_1 = V_1 + \widehat{v_1} \tag{9}$$

$$v_2 = V_2 + \widehat{v_2} \tag{10}$$

$$i_1 = I_1 + \widehat{i_1} \tag{11}$$

$$i_2 = I_2 + \widehat{i_2} \tag{12}$$

where "$\hat{h}$" represents the small part of the signal.

2.3.1. Averaged large signal model

Considering the initial scheme of the SEPIC converter Figure 2, and its subinterval analysis Figures 3(a) and 3(b) we notice the following:

– Subinterval 1 ($0 \le t \le dT$):

$$\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 \\ 0 & \frac{-1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{\boldsymbol{A_1}} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{B_1}} (v_g) \tag{13}$$

From (28) we have:

$$(v) = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{\boldsymbol{C_1}} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \underbrace{[0]}_{\boldsymbol{D_1}} (v_g) \tag{14}$$

– Subinterval 2 ($dT \le t \le T$):

$$\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1}{L_1} & \frac{-1}{L_1} \\ 0 & 0 & 0 & \frac{-1}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{1}{C_2} & \frac{1}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{\boldsymbol{A_2}} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{B_2}} (v_g) \tag{15}$$

From (28) we have:

$$(v) = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{\boldsymbol{C_2}} \begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix} + \underbrace{[0]}_{\boldsymbol{D_2}} (v_g) \tag{16}$$

To obtain the averaged large signal model we add the above matrices in the form:

$$\mathrm{A} = A_1 d + A_2(1-d) \tag{17}$$

$$B = B_1 d + B_2(1-d) \tag{18}$$

$$C = C_1 d + C_2(1-d) \tag{19}$$

$$C = C_1 d + C_2(1-d) \tag{20}$$

And we get the following state space model representation:

$$\underbrace{\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1(1-d)}{L_1} & \frac{-1(1-d)}{L_1} \\ 0 & 0 & \frac{d}{L_2} & \frac{-1(1-d)}{L_2} \\ \frac{1-d}{C_1} & \frac{-d}{C_1} & 0 & 0 \\ \frac{1-d}{C_2} & \frac{1-d}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B} \underbrace{(v_g)}_{U} \tag{21}$$

$$\underbrace{(v)}_{Y} = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{C} \underbrace{\begin{bmatrix} i_1 \\ i_2 \\ v_1 \\ v_2 \end{bmatrix}}_{X} + \underbrace{[0]}_{D} \underbrace{(v_g)}_{U} \tag{22}$$

2.3.2. Steady state model

It is worth to note that the above time varying matrices, depend on "d" and they represent a nonlinear model that is hard to control. For this reason, it is of good benefit to linearize them. Therefore, we will perform the perturbation on the signal using (7) to (12), split the matrices, remove the steady state part and linearize the model considering the part "$\hat{d}$" as another input. That is if we desire to control the converter, we will be counting on the small signal "$\hat{d}$". At steady state, we consider all the component to be DC-values, and thus constant and unchanging, which makes all the derivatives equal to zero. Hence:

$$\underbrace{\begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{v}_1 \\ \dot{v}_2 \end{bmatrix}}_{\dot{X}} = \tag{23}$$

$$d = D, v_g = V_g, v_1 = V_1, v_2 = V_2, i_1 = I_1, i_2 = I_2 \tag{24}$$

Thus:

$$\underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\dot{X}} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1(1-D)}{L_1} & \frac{-1(1-D)}{L_1} \\ 0 & 0 & \frac{D}{L_2} & \frac{-1(1-D)}{L_2} \\ \frac{1-D}{C_1} & \frac{-D}{C_1} & 0 & 0 \\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{A} \underbrace{\begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix}}_{X} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B} \underbrace{(V_g)}_{U} \tag{25}$$

$$\underbrace{(V)}_{Y} = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{C} \underbrace{\begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix}}_{X} + \underbrace{[0]}_{D} \underbrace{(V_g)}_{U} = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{C} \underbrace{\begin{bmatrix} I_1 \\ I_2 \\ V_1 \\ V_2 \end{bmatrix}}_{X} \tag{26}$$

And the steady state model can be expressed in the following formulas:

$$0 = A * X + B * U \implies X = -A^{-1} * B * U \tag{27}$$

$$Y = C * X + D * U = C * X = -C * A^{-1} * B * U \tag{28}$$

In (28) represents the solution of the steady state model, and it can be written in the form of:

$$\underbrace{(V)}_{\boldsymbol{Y}} = -\underbrace{[0 \quad 0 \quad 0 \quad 1]}_{\boldsymbol{C}} \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1(1-D)}{L_1} & \frac{-1(1-D)}{L_1} \\ 0 & 0 & \frac{D}{L_2} & \frac{-1(1-D)}{L_2} \\ \frac{1-D}{C_1} & \frac{-D}{C_1} & 0 & 0 \\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}^{-1}}_{\boldsymbol{A}} \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{B}} \underbrace{(V_g)}_{\boldsymbol{U}} \tag{29}$$

2.3.3. Deriving the small signal model

Going back to the averaged large signal model and inserting (7) → (12) into (21), (22), we end up with the following relationships:

$$\underbrace{\begin{bmatrix} I_1 + \dot{\hat{\imath}_1} \\ I_2 + \hat{\imath_2} \\ V_1 + \hat{v_1} \\ V_2 + \hat{v_2} \end{bmatrix}}_{\boldsymbol{X}+\dot{\hat{\boldsymbol{x}}}} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1(1-D-\hat{d})}{L_1} & \frac{-1(1-D-\hat{d})}{L_1} \\ 0 & 0 & \frac{D+\hat{d}}{L_2} & \frac{-1(1-D-\hat{d})}{L_2} \\ \frac{1-D-\hat{d}}{C_1} & \frac{-D-\hat{d}}{C_1} & 0 & 0 \\ \frac{1-D-\hat{d}}{C_2} & \frac{1-D-\hat{d}}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{\boldsymbol{A}+\hat{\boldsymbol{a}}} \underbrace{\begin{bmatrix} I_1 + \hat{\imath_1} \\ I_2 + \hat{\imath_2} \\ V_1 + \hat{v_1} \\ V_2 + \hat{v_2} \end{bmatrix}}_{\boldsymbol{X}+\hat{\boldsymbol{x}}} + \underbrace{\begin{bmatrix} \frac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{\boldsymbol{B}} \underbrace{\left(V_g + \hat{v_g}\right)}_{\boldsymbol{U}+\hat{\boldsymbol{u}}} \tag{30}$$

$$\underbrace{(V + \hat{v})}_{\boldsymbol{Y}} = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{\boldsymbol{C}} \underbrace{\begin{bmatrix} I_1 + \hat{\imath_1} \\ I_2 + \hat{\imath_2} \\ V_1 + \hat{v_1} \\ V_2 + \hat{v_2} \end{bmatrix}}_{\boldsymbol{X}+\hat{\boldsymbol{x}}} + \underbrace{[0]}_{\boldsymbol{D}} \underbrace{\left(V_g + \hat{v_g}\right)}_{\boldsymbol{U}} \tag{31}$$

Hence, every variable is now represented in terms of its steady state term and small signal term.

Note that: $X + \dot{\hat{x}} = \dot{\hat{x}} = \begin{bmatrix} I_1 + \dot{\hat{\imath}_1} \\ I_2 + \hat{\imath_2} \\ V_1 + \hat{v_1} \\ V_2 + \hat{v_2} \end{bmatrix} = \begin{bmatrix} \dot{\hat{\imath}_1} \\ \hat{\imath_2} \\ \hat{v_1} \\ \hat{v_2} \end{bmatrix}$

On the other hand, we have from (27) $0 = A * X + B * U$. Assuming that all the multiplications of small signal entities to be very small (i.e.: $\hat{m} \times \hat{n} = 0$), we can neglect them. Splitting the matrices based on the above assumptions and conclusions, we can easily obtain the following small signal model written in terms of $\hat{d}$ and $\hat{v}_g$.

$$\underbrace{\begin{bmatrix} \dot{\hat{\imath}_1} \\ \hat{\imath_2} \\ \hat{v_1} \\ \hat{v_2} \end{bmatrix}}_{\dot{\hat{\boldsymbol{x}}}} = \underbrace{\begin{bmatrix} 0 & 0 & \frac{-1(1-D)}{L_1} & \frac{-1(1-D)}{L_1} \\ 0 & 0 & \frac{D}{L_2} & \frac{-1(1-D)}{L_2} \\ \frac{1-D}{C_1} & \frac{-D}{C_1} & 0 & 0 \\ \frac{1-D}{C_2} & \frac{1-D}{C_2} & 0 & \frac{-1}{RC_2} \end{bmatrix}}_{\boldsymbol{A}} \underbrace{\begin{bmatrix} \hat{\imath_1} \\ \hat{\imath_2} \\ \hat{v_1} \\ \hat{v_2} \end{bmatrix}}_{\hat{\boldsymbol{x}}} + \underbrace{\begin{bmatrix} \frac{V_1+V_2}{L_1} & \frac{1}{L_1} \\ \frac{V_1+V_2}{L_2} & 0 \\ \frac{-I_1-I_2}{C_1} & 0 \\ \frac{-I_1-I_2}{C_2} & 0 \end{bmatrix}}_{\boldsymbol{B_{dv}}} \underbrace{\begin{bmatrix} \hat{d} \\ \hat{v_g} \end{bmatrix}}_{\boldsymbol{U_{dv}}} \tag{32}$$

$$\underbrace{(\hat{v})}_{\boldsymbol{Y}} = \underbrace{[0 \quad 0 \quad 0 \quad 1]}_{\boldsymbol{C}} \underbrace{\begin{bmatrix} \hat{\imath_1} \\ \hat{\imath_2} \\ \hat{v_1} \\ \hat{v_2} \end{bmatrix}}_{\hat{\boldsymbol{x}}} + \underbrace{[0]}_{\boldsymbol{D}} \underbrace{\left(\hat{v_g}\right)}_{\boldsymbol{U}} \tag{33}$$

Deriving the state space equation of the small signal model, we can now study the behavior of the system at the transient time:

$$\begin{cases} \dot{x} = Ax + Bu \\ y = Cx + Du \end{cases} \tag{34}$$

Converting the above system into Laplace form:

$$\begin{cases} sX(s) = A.X(s) + B.U(s) \\ Y(s) = C.X(s) + D.U(s) \end{cases} \quad (35)$$

$$\begin{cases} X(s) = [sI - A]^{-1}.B.U(s) \\ Y(s) = C.[sI - A]^{-1}.B.U(s) + DU(s) \end{cases} \quad (36)$$

Having set our relationships, we can now derive the open loop transfer function of the output voltage $\hat{v}$ of the converter with respect to the duty cycle $\hat{d}$:

$$\frac{\hat{v}}{\hat{d}} = C.[sI - A]^{-1}.B_d \quad (37)$$

Where:

$$B_d = \begin{bmatrix} \frac{V_1+V_2}{L_1} \\ \frac{V_1+V_2}{L_2} \\ \frac{-I_1-I_2}{C_1} \\ \frac{-I_1-I_2}{C_2} \end{bmatrix} \quad (38)$$

Since we are considering the voltage source of the converter to be a storage module (battery modules/supercapacitor modules) the converter shall have a bidirectional power flow capability, in order to charge these modules. There are lot of ways to convert the system to a bidirectional way, the simplest among them is to replace the transistor Q_1 and the diode D_1 by IGBT's with anti-parallel diode to allow the current to flow when needed in both directions. An implementation block for the converter in MATLAB/Simulink is shown in Figure 4.

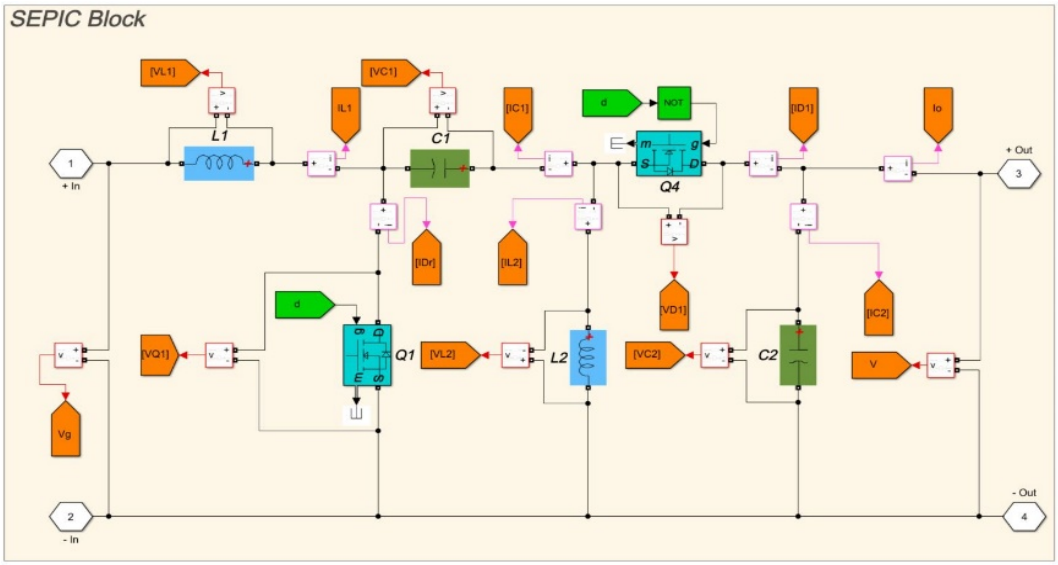


Figure 4. Bidirectional SEPIC converter

2.4. Single ended primary inductance converter simulation

Once the open loop transfer function is derived, we can start analyzing the system response. The considered system consists mainly of a set of batteries and/or supercapacitors feeding a separate converter with 500 volts DC. The role of the SEPIC converter is to boost the input voltage to 800 volts and thus maintain the DC-link bus supplying a maximum load of 120 kW. The design assumptions of the converter took into account these factors and led to the following design basis parameters as per Table 1.

The duty cycle D is calculated using the following relationship:

$$V = \frac{D}{1-D} V_g \quad (39)$$

With the assistance of computer simulation in MATLAB, the above parameter values and the derived equations are used to obtain the open loop transfer function of the output voltage $\hat{v}$ of the converter with respect to the duty cycle $\hat{d}$ as well as the transfer function of the output voltage of the converter with respect to the input voltage:

$$\frac{\hat{v}}{\hat{d}}(s) = \frac{-1.352*10^6\ s^3+1.318*10^{10}\ s^2-5.273*10^{12}\ s+5.141*10^{16}}{s^4+650\ s^3+7.8*10^6\ s^2+2.535*10^9\ s+1.521*10^{13}} \quad (40)$$

$$\frac{\hat{v}}{\hat{v}_g}(s) = \frac{6.24*10^6\ (s^2+3.9*10^6)}{(s^2+650\ s+3.9*10^6)\ (s^2+1.705\ *10^{-12}\ s+3.9*10^6)} \quad (41)$$

We can see that the obtained transfer function is of 4th order. It bodes plot diagram is shown in Figure 5. Analyzing the zeros and poles of this equation shows that it has 4 poles and 3 zeros. Among the zeros, one is located in the right half side of the s-plane, therefore the bode diagram analysis is not enough in this case to assess the stability of the transfer function. This is why we will use also the root locus analysis Figure 6, that describes how the poles and zeros are being distributed.

Table 1. Design parameters

Design Parameters	Value
Switching Frequency	20 KHz
Input Voltage	500 V
Output Voltage	800 V
Load Resistance (@ 120 kW)	5.333 Ω
Steady-State duty cycle D	0.6154
Δi_{L1}	15% of I_{L1}
Δi_{L2}	15% of I_{L2}
L_1	0.2136 mH
L_2	0.3419 mH
Δv_{C1}	1% of V_{C1}
Δv_{C2}	1% of V_{C2}
C_1	0.4615 mF
C_2	0.2884 mF

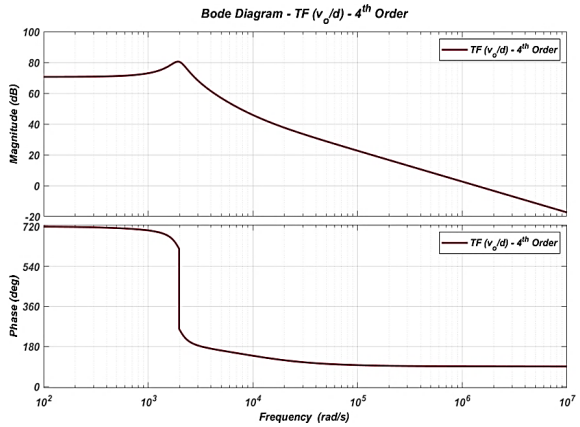


Figure 5. Bode plot diagram of the converter transfer function

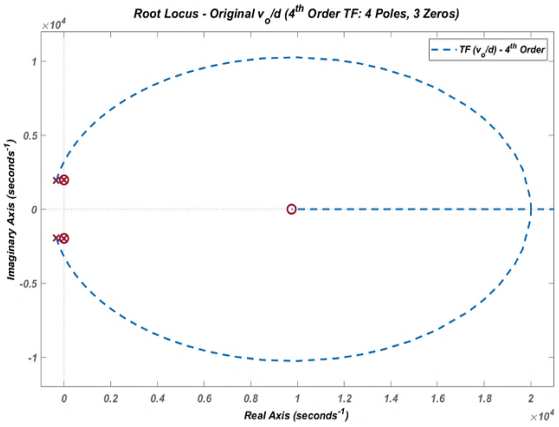


Figure 6. Root locus plot of the converter transfer function

2.5. Order reduction and Padé approximation

The derived transfer function represents a complete description of the control-to-output dynamics of the system. However, since it is hard to control it, we will try to minimize its order using Padé approximation for single input single output (SISO) transfer functions. By reducing the order from 4th degree into 2nd order and 1st order, we can use the results to derive the proportional and integral parameter of the PI controller. The transfer function approximations are shown below:

Padé approximation to 2nd order equation:

$$\frac{\hat{v}}{\hat{d}}(s) = \frac{-1.352*10^6\ (s-9750)}{s^2+650\ s+3.9*10^6} \quad (42)$$

Padé approximation to 1st order equation:

$$\frac{\hat{v}}{\hat{d}}(s) = \frac{1.255*10^7}{s+3714} \quad (43)$$

A bode diagram analysis is done to verify the approximation feasibility in Figures 7 and 8, and the root locus of the approximated transfer functions are also plotted in Figure 9. For clarity, the body plots of all the derived transfer functions are sketched together in Figure 10. A step response is also plotted for the 3 variants of the transfer function in order to show stability at steady state, and the results are shown in Figure 11. It is clear that all the functions are stable at steady state, where the original transfer function shows a decaying oscillation that we will be dealing with after implementing our controller.

All the open loop transfer functions reach stability within a short period of time. The original transfer function and the reduced one to 2nd order have a positive pole, at the contrary from the reduced transfer function to 1st order. Since we are going to use the IMC control method, we will check the response of the PI controller based on both 1st and 2nd order transfer functions.

2.5.1. The pulse width modulator

The main job of the PWM is to convert the input control signal to a set of pulses with a controlled duty cycle. These pulses will turn ON and OFF the semi-conductor switch and the output voltage is generated. There are many types of PWM techniques, the most famous among them is applied here, and it is based on comparing the input control signal with a periodic waveform (sawtooth waveform). When the input control signal is higher than the sawtooth signal, the PWM block will trigger the semi-conductor. When the input is lower than the comparator signal, the semiconductor is turned OFF. By this operation, the duty cycle is dynamically calculated during each period based on the output of the controller and will have $\hat{d}$ with a value of $\frac{T_{ON}}{T}$, "T" being the period of the comparator.

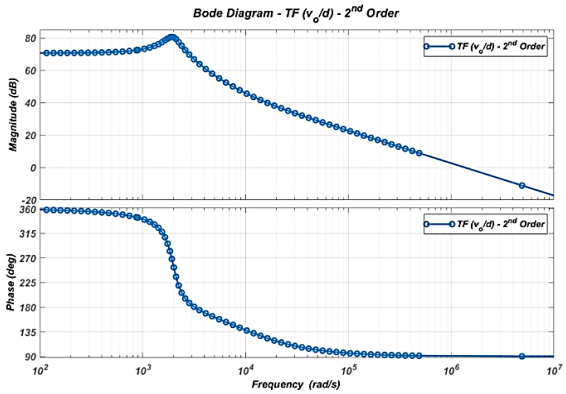


Figure 7. Bode plot diagram of the converter transfer function with 2nd order

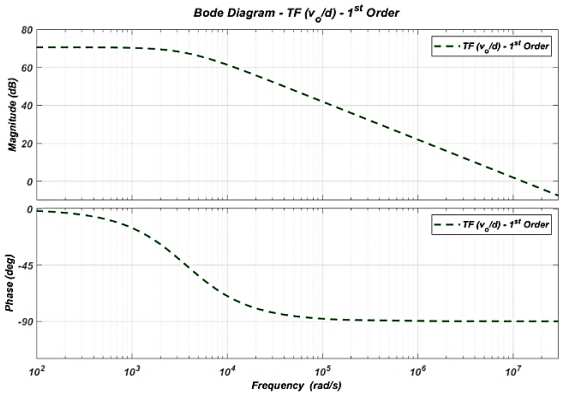


Figure 8. Bode plot diagram of the converter transfer function with 1st order

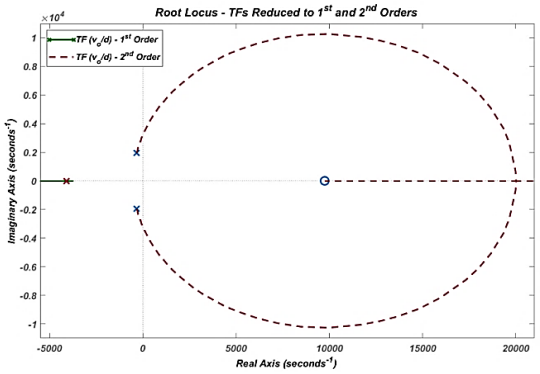


Figure 9. Combined root locus plot for 1st and 2nd order reduced transfer functions

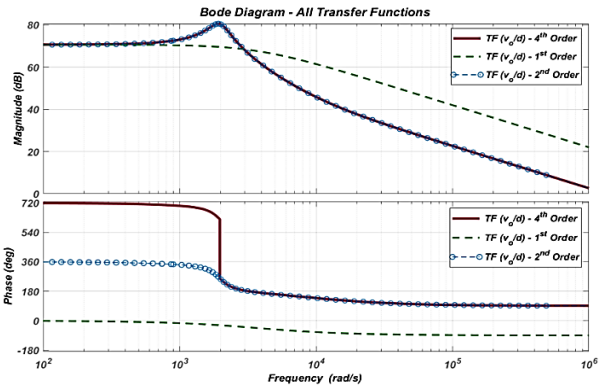


Figure 10. Bode plot diagrams of the converter main transfer function and its reduced orders

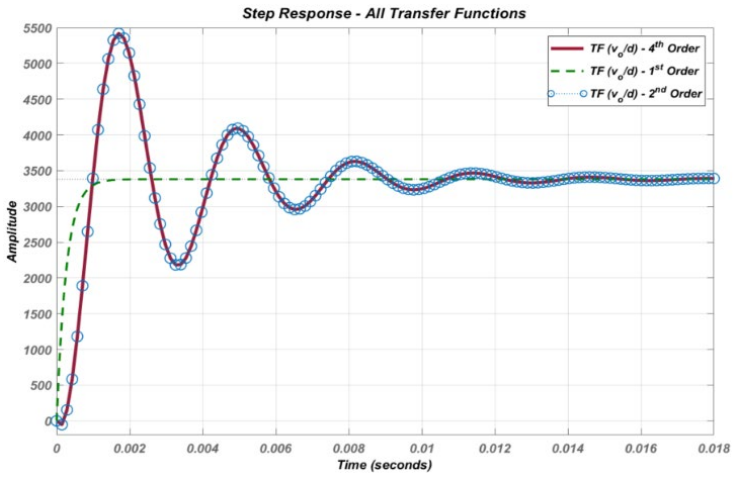


Figure 11. Step responses of the transfer function and its reduced orders

3. RESULTS AND DISCUSSION

The controller design will follow the form shown in Figure 12, we will be presenting two ways of deriving the parameters of the controller. The first way is using the conventional method for deducting the proportional and integral parameters of the PI controller. The second method is considering the available dynamics and parameters of the converter, with the help of the Internal Model Control method. Both methods are effective, however as we will see the IMC is more scientific since it is based on imitating the converter transfer function.

There are many different ways to deduce the parameters of a PI controller. For this purpose, a model has been constructed in MATLAB/Simulink. The values of k_p and k_i, mentioned in Table 2, were fed into the system and its response to a step input signal was tested under the 4th order SEPIC transfer function. The result is shown in the first part of Figure 13.

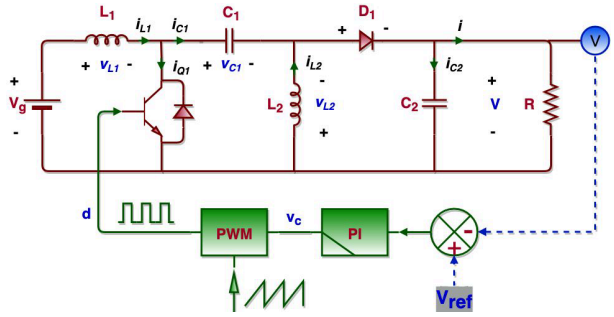


Figure 12. Controller of SEPIC converter

Table 2. PI controller parameters

PI Controller Parameters	
k_p	k_i
0.00001	0.05

The second part of Figure 13 shows the output voltage of the converter (constructed in Simulink according to the data presented in Table 1) with respect to an input reference of 800 volts. It is clear how the output voltage aligns itself with the reference value with a riste time of 14 ms and 27.5 ms for the transfer function output and the converter output respectively. The voltage ripple of the output capacitor C2 in Figure 14 shows that the PI controller regulates the output within the design requirements (±1% of the reference value). This will ensure that the voltage supplied by the batteries or the super capacitor will be boosted to 800 volts ±1%.

Details about the IMC controller are explained in [49], the parameters are calculated using the following equations for a one degree of freedom controller and considering the transfer function reduced to 1st order [52]:

$$k_p = \frac{\tau_r}{\tau_{sepic} k_{sepic}} = 7.9654 * 10^{-6} \quad (44)$$

$$k_i = \frac{k_p}{\tau_r} = 0.0296 \quad (45)$$

where, τ_r is the transfer function rising time, k_{sepic} is the transfer function gain and τ_{sepic} the low pass filter time constant which affects the response speed of the closed loop system. Similar analysis is shown in the following figures and at the contrary from what was predicted, the IMC control method did not provide better rising time 0.047 seconds. In fact, the choice of τ_{sepic}, between robustness and response speed, will affect the rising time. The controller works well but the rising time can still be improved. We also implied the IMC controller rules the transfer function reduced to 2nd order transfer function (42: which is closer to the original transfer function form) and as it is predicted the new IMC controller provides better rising time 0.037 seconds and less oscillations, and therefore better control for the following parameters:

$$k_p = \frac{2\zeta\tau_r}{\tau_{sepic} k_{sepic}} = 6.3212 * 10^{-6} \quad (46)$$

$$k_i = \frac{k_p}{2\zeta\tau_r} = 0.038 \quad (47)$$

where, τ_r is the transfer function rising time, k_{sepic} is the transfer function gain, ζ is the damping ratio and τ_{sepic} being the low pass filter time constant. The resulting output voltage is shown in Figure 15.

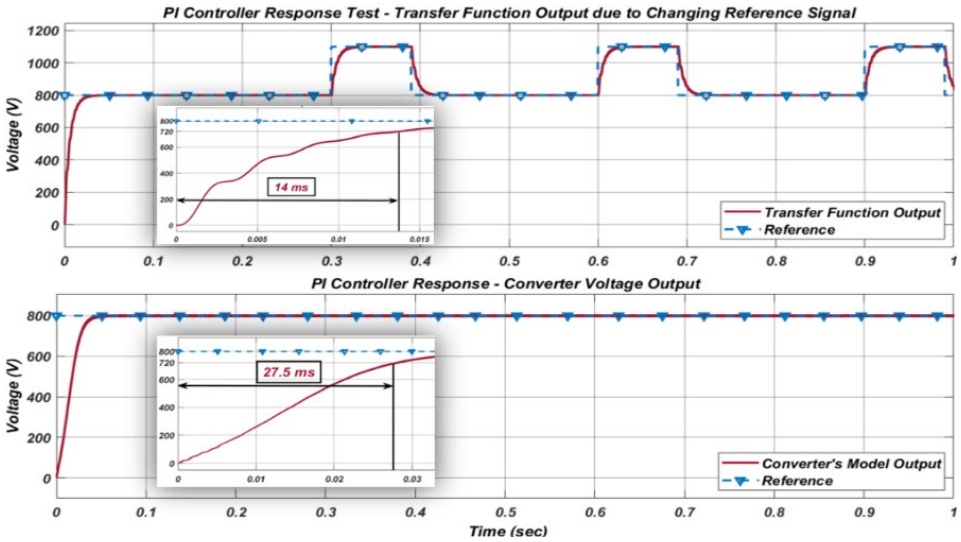


Figure 13. PI controller response and voltage output

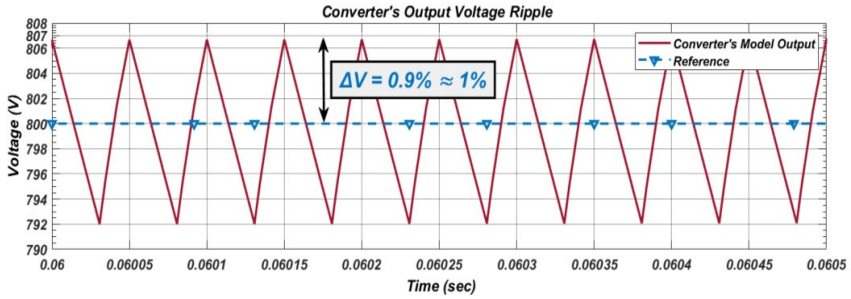


Figure 14. Output voltage ripple using a PI controller

Since we designed our transfer function using the small signal analysis, the output of the PI controller is the small signal duty cycle $\hat{d}$, therefore if we feed the PWM with the large signal "d" (7), we will expect a

faster response. For this purpose, we will add the steady state part of the duty cycle "D" to the input signal of the PWM as shown in the Figure 16 and its implementation in MATLAB/Simulink is presented in Figure 17. The output response of the improved controller is shown to be far better than the previous method providing a rising time around 0.6 ms Figure 18.

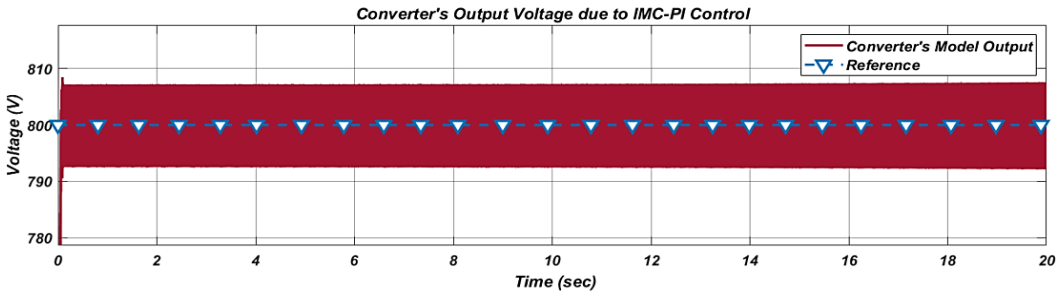


Figure 15. Output voltage response using IMC control

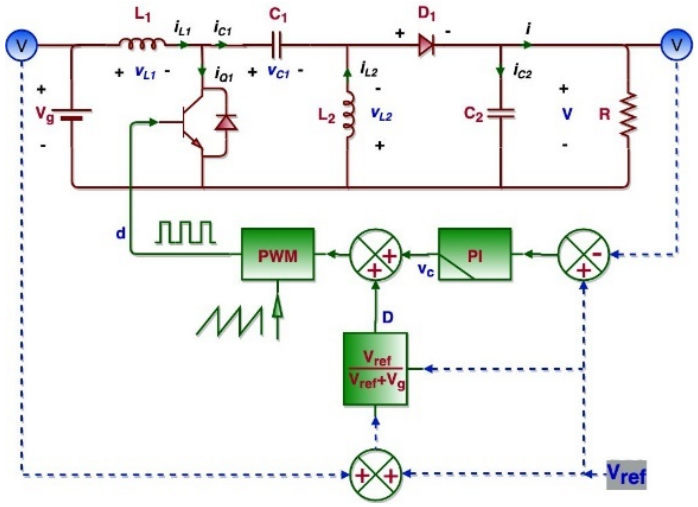


Figure 16. Improved controller scheme

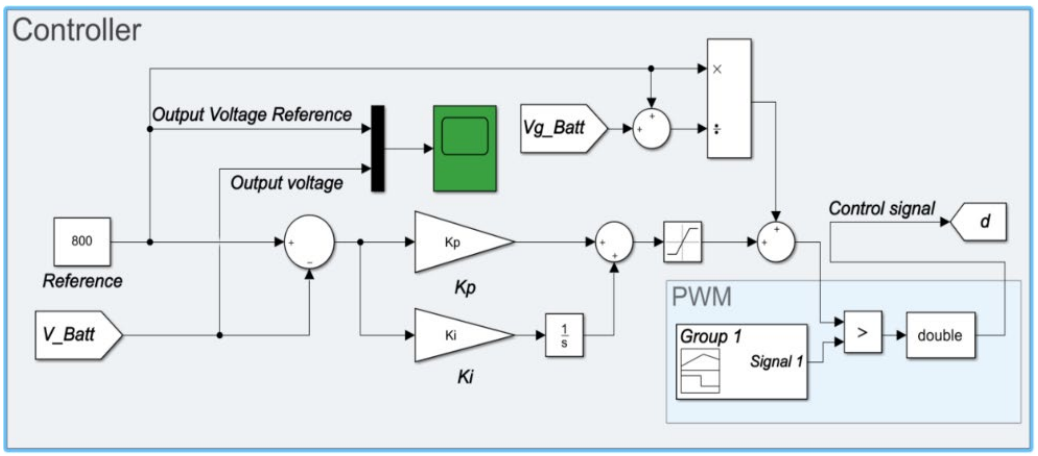


Figure 17. SEPIC controller block in MATLAB/Simulink

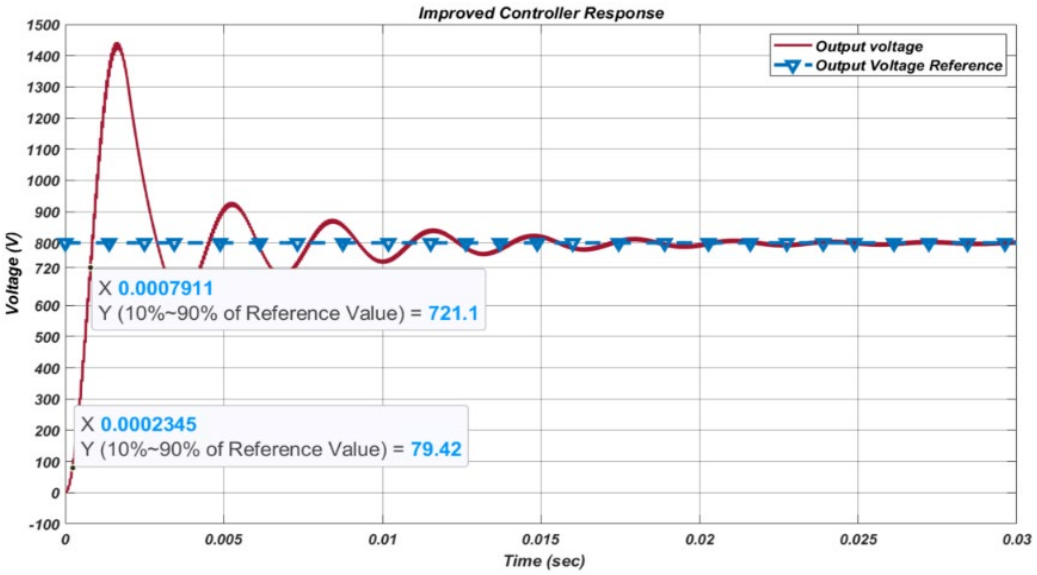


Figure 18. Response of the improved controller

The steady state duty cycle "D" is derived from (48) and V is replaced with V_{ref}:

$$D = \frac{V_{ref}}{V_{ref}+V_g} \tag{48}$$

Hence the input to the PWM is:

$$d = \hat{d} + \frac{V_{ref}}{V_{ref}+V_g} \tag{49}$$

And the response of the controller is shown below.

All the previous analysis was conducted by supplying the converter by an ideal DC-source V_g; therefore, it is good to test its response when it is supplied by a non-ideal DC-source like a battery and supercapacitor. The battery model used from MATLAB/Simulink, imitates the behavior of a Li-ion battery, and it has been utilized to test the response of the converter. For this matter, the following data of the battery, in Table 3, has been considered.

The response due to the input of a battery as a DC-source showed very minor oscillations that were not present when we used an ideal source, especially at the transient time, however the ripple in the output voltage Figures 19(a) and 19(b) was conserved, which proves the right design of the converter. On the other hand, the transient response showed to be very satisfactory as seen in Figure 20 with a rising time of almost 0.55 ms. On the other hand, the supercapacitor (SC) used in the simulation imitates the Stern model behavior. The parameters used for the supercapacitor are presented in Table 4. The response of the supercapacitor showed similar results to the battery. A combined plot for 2 converter outputs, one powered by a battery set, the other by a supercapacitor set, is shown in Figure 21 and Figure 22.

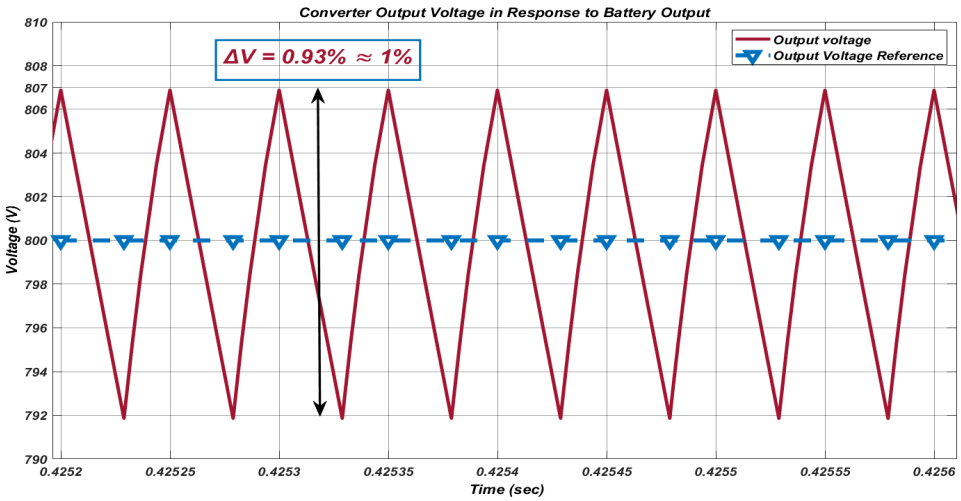
It is worth to note that the higher the initial voltage (i.e. the SOC) of the battery or the supercapacitor, the faster their response will be. On Figure 23, a plot shows the response of a fully charged supercapacitor and a battery with an SOC of 85%. We can notice the change in the battery's response due to such change.

Table 3. Battery parameters

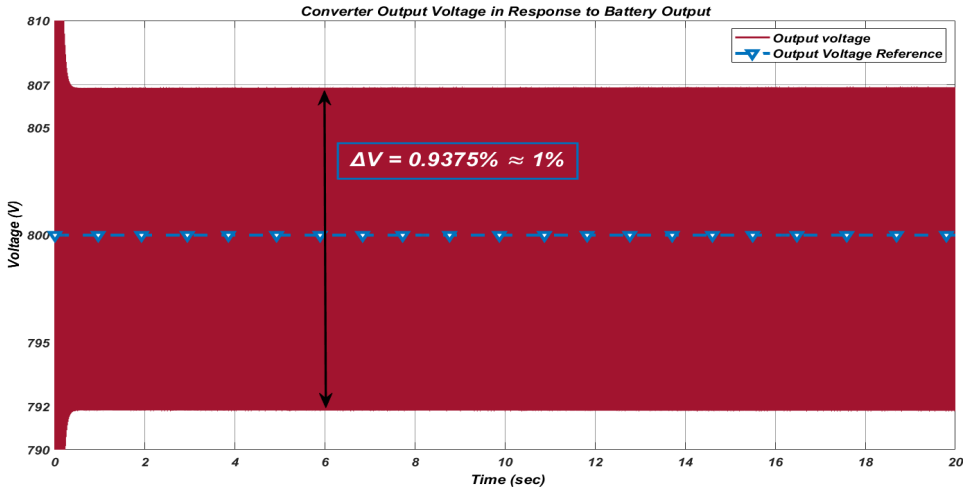
Battery Parameters	
Nominal Voltage (V)	3.3
Rated Capacity (Ah)	2.05
Initial State of Charge (SOC) (%)	100
Battery Response Time (s)	0.1
Number of Batteries in Series	152
Number of Batteries in Parallel	30

Table 4. Supercapacitor parameters

Supercapacitor Parameters	
Nominal Voltage (V)	2.7
Rated Capacitance (F)	3500
Equivalent Series Resistance (m Ohms)	8.9
Initial Voltage (V)	585.9
Number of Supercapacitors in Series	185
Number of Supercapacitors in Parallel	30
SOC (%)	100
Operating Temperature (ºC)	25



(a)



(b)

Figure 19. Output voltage response to the battery input (a) voltage ripple identification and (b) response over all the simulation time

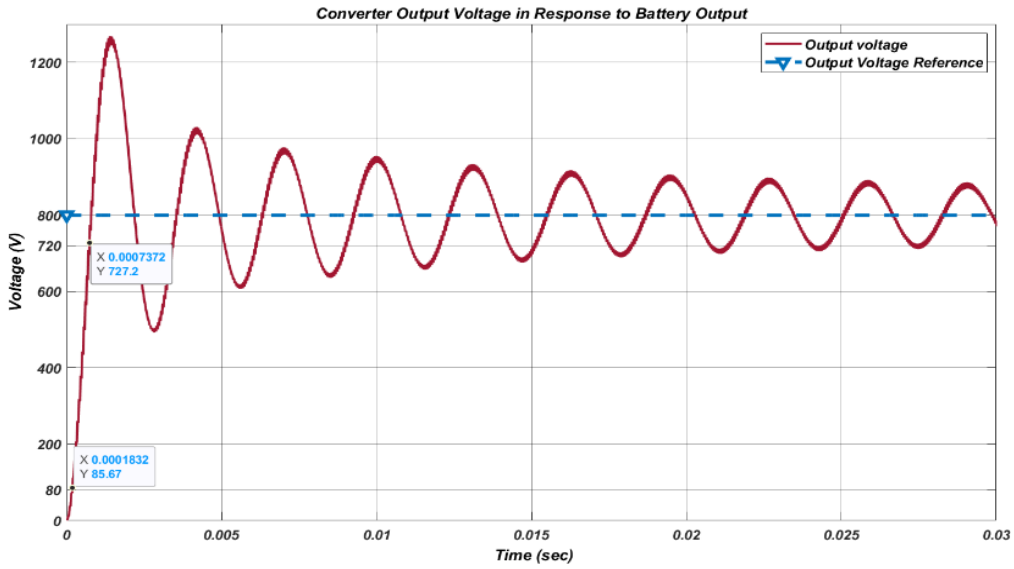


Figure 20. Transient response of converter supplied by battery

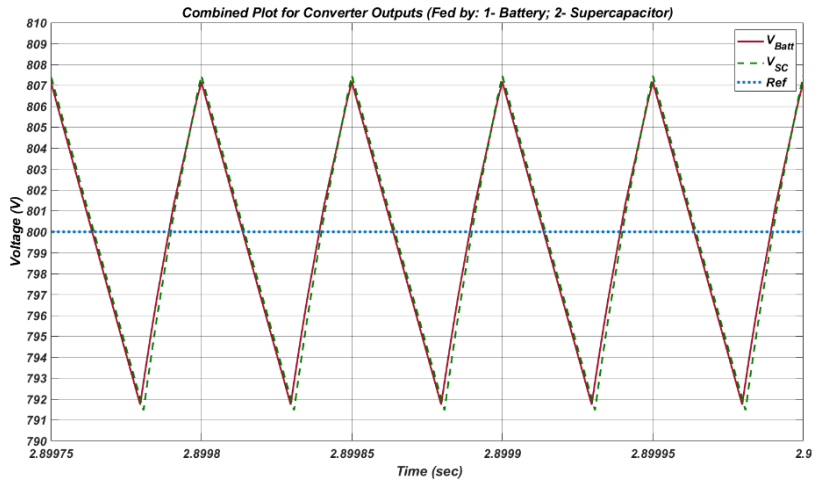


Figure 21. Two converters' outputs: one powered by battery module, the other by supercapacitor module

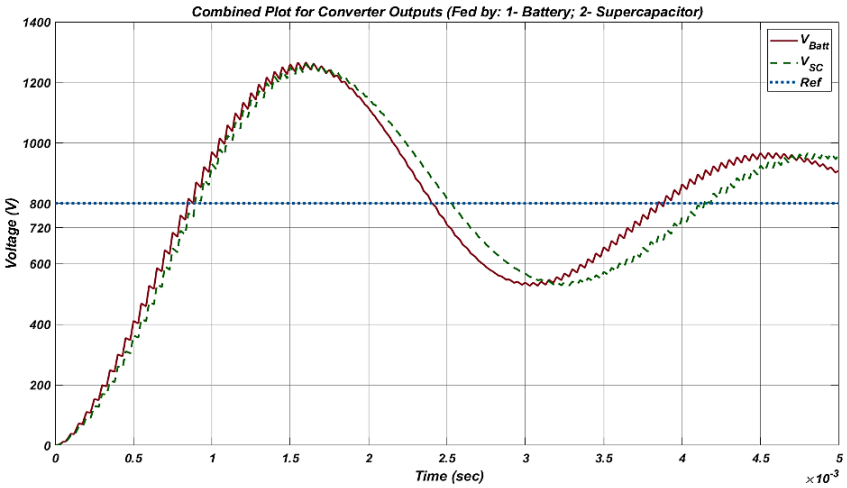


Figure 22. Transient response of two converters outputs: one powered by battery module, the other by supercapacitor module

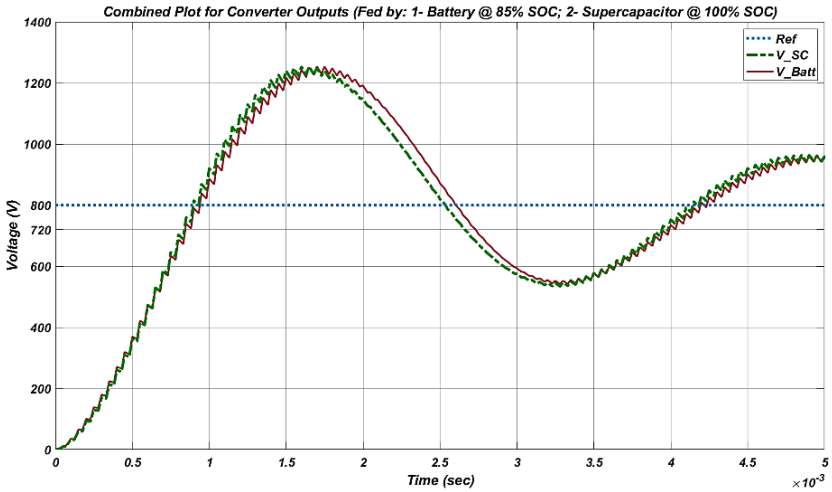


Figure 23. Response of two converters outputs: one powered by battery module, the other by supercapacitor module having a lower SOC%

4. CONCLUSION

The analysis of DC/DC converters has been carried out. It is substantiated that for autonomous power supply systems including energy storage devices (batteries, supercapacitor modules), it is advisable to use a SEPIC converter. The parameters of the elements of the SEPIC converter have been developed in addition to its three mathematical models. The dynamic characteristics of the small signal model has been derived and used to build a PI controller for the converter. Reduced order models of the original transfer function of the controller have been derived and used to achieve a successful simulation for the control operation. The simulation results show the response of the converter and justify the use of the IMC-based PI controller method by using a reduced order model. The obtained simulation results show the applicability of the proposed solution with autonomous power supply sources fed by batteries or supercapacitors. For converters with high order transfer function, implementing a control based on internal model control method is a complex process. However, with the help of Padé approximation, reducing the order of the converter's transfer function, still can save some characteristics of the dynamics of the system, yet makes the control process easier for implementation. SEPIC converters can be used not only in autonomous power supply systems with energy storage (batteries and supercapacitor modules), but also in power factor correction systems, as well as for photovoltaic power plants and wind turbines.

5. FUTURE CONSIDERATION

Further studies on SEPIC will include analysis to make the design integrable into real components taking into account the real values of the converter components and their parasitic resistances. Seeking other control techniques for the SEPIC and its complement converters will also be a subject for future consideration.

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