Novel multi-device unified powerquality conditioner for powerquality improvement

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Article Info

ABSTRACT

This paper describes the customizable multi-device unified power-quality conditioner (MD-UPQC) is designed especially for multi-feeder distribution networks. The proposed MD-UPQC can exchange the power between the multi-feeders and proficiently mitigates all voltage-current associated power-quality problems, make sure to maintain balanced power-flow to consumers. At recent days, various manufacturers recommend the provision of multilevel inverters in mid-range customized compensation devices with desirable control schemes. In distinct, the 5-level diode-clamped multi-level inverter (DCMLI) is best suited for MD-UPQC over traditional 3-level voltage source inverter (VSI) topology for attaining enhanced features. In this paper, MD-UPQC has been proposed with three 5-level DCMLI modules interfaced as back-to-back with a common direct current (DC) capacitor. The simplified phase-dispositional modulation technique is easily assembled with proposed universal voltage-current reference controller for significant functioning of DCMLI-MDUPQC device. The operation and performance of proposed model and its control scheme is evaluated with MATLAB/Simulink computational tool, simulation results are presented.
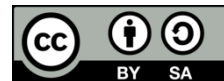
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1. INTRODUCTION

The power-quality (PQ) in multi-feeder distribution networks has been crucially proliferated, affecting the loads connected at common feeding point of distribution network due to several deviations and distortions [1]. The increased use of non-linear power-electronic converters, short-circuits, switching of massive loads and electric motors takes-place in secondary distribution networks are the frequent examples causing the PQ distortions [2]. It initiates the injection of harmonic currents, reactive-power extraction, load unbalancing, and poor power-factor. Moreover, the effect of voltage-quality initiates the voltage harmonics, voltage sag-swells, voltage unbalance and voltage deviations which imply the power-pollution at common-feeding point of distribution network [3]. These critical loads are connected to a network with unfortunate PQ then customized flexible alternate current transmission system (FACTS) devices should be introduced to compensate these deficits [4], [5].

The multi-feeder customized FACTS devices are categorized as many groups based on definite PQ problems and its affects such as interline dynamic-voltage restorer [6], interline power-flow controller [7], and interline-unified power-quality controller [8], so on. Particularly, multi-device unified power-quality conditioner (MD-UPQC) is designed especially for PQ enrichment in multi-feeder distribution systems. It can exchange power between multi-feeders and proficiently mitigates both voltage-current associated PQ problems and make

sure to maintain quality power in multi-feeder distribution systems. The structure of the MD-UPQC device in multi-feeder distribution network is most likely presented in [9]; substantially it is designed with multiple voltage source inverters (VSIs) connected as back-to-back form like series-shunt, shunt-shunt and shunt-series manner between the feeders through common DC-link point.

Mukassir *et al*. proposed the novel design of multi-converter UPQC for PQ improvement in multi-feeder distribution network using multiple VSIs as shunt-series form connected through an equal DC capacitor in [10]. Rao and Rao [11] explored the multi-feeder universal compensation device for mitigating of both load voltage and source current related PQ problems. Moreover, it provides power transfer between the feeders during sudden interruptions by using multi-feeder unified power-quality controller is developed through multi-VSIs devices in [11]. Yadav *et al*. [12] explored the new trend multi-converter UPQC in multi-bus distribution network for PQ conditioning for maintaining load current and supply voltage as balanced nature. The MC-UPQC is developed with the help of shunt-series connected VSIs through common DC-point capacitor in [12].

The major problems highlighted in traditional three-level VSIs in customized-compensation is proposed in [10]–[12] have limited developments due to common-mode voltage and reverse voltage blocking capability of switches. Also, its di/dt and dv/dt introduces the more electro-magnetic interference (EMI) loss to entire system. To overcome limitations in traditional three-level VSIs by introducing multilevel inverter (MLI) technology. It is the most relevant technology employed for high-power medium-voltage distribution system, also used in electric-vehicle (EVs), distribution generation (DGs), variable speed drives (VSDs) applications [13].

Multilevel inverters are grown, explored and recommended at high rate in recent past, it is even under development and research on MLI based customized FACTS devices. A multilevel inverter produce AC staircase output voltage which is close to the sinusoidal wave-shape by using various switching devices connected to the input DC source. The well-recognized MLI topologies are cascaded H-bridge MLI, flying-capacitor MLI and diode-clamped MLI topologies [14]–[16]. Among these, the single DC sourced diode-clamped multilevel inverter (DC-MLI) is best suited and incorporated in MD-UPQC device. It is operated through multi-carrier based pulse-width modulation (MCB-PWM) technique with significant control objective [17].

The symmetrical instantaneous control theory (SICT) [18], instantaneous real-power control theory (IRP) [19], and synchronous reference control theory (ID-IQ) [20] are prominent control objectives explored in [21]. The above control objectives are fated-out due to complex dual-transformations, more mathematical analysis and high delayed signals. The major objective of this work is proposing a new universal voltage-current reference (UVCR) control objective for generation of reference current/voltage signals to DCMLI-MDUPQC device. The proposed UVCR control scheme has been developed with simple mathematical functions, no need of any transformations, low delay and produce fundamental switching frequency in reference voltage and current sequence. The operation of DCMLI-MDUPQC device with proposed UVCR control objective is designed and verified through MATLAB/Simulink computational tool, Simulink results are described in detail.

2.   PROPOSED DCMLI-MDUPQC METHOD

The schematic model of 5-level DCMLI structure is depicted in Figure 1. In distinct, the proposed 5-level diode-clamped multi-level inverter (DCMLI) is best suited over traditional 3-level VSI topology for PQ enhancement [22]. The proposed MD-UPQC is designed with three 5-level DCMLI modules interfaced as back-to-back with a common DC capacitor. It includes, MLI-1, MLI-2 are integrated as shunt-series to feeder-2 and MLI-3 is integrated as series to feeder-1 via 1:1 linear design transformers and filter units. The incorporation of DCMLI in MD-UPQC device is good opportunity for getting enhanced compensation features over the traditional VSI device, and technically accepted for any compensation structure [23]–[25].

It consists, 2(N-1) switches named as upper and lower unit in a single-phase defined as S_{1a}/S_{1a}'; S_{2a}/S_{2a}'; S_{3a}/S_{3a}'; S_{4a}/S_{4a}', for appropriate current flow (N-1)*(N-2) clamping diodes are required defined as D_{1a}/D_{1a}'; D_{2a}/D_{2a}'; D_{3a}/D_{3a}', respectively. Mostly, (N-1) DC capacitors are required defined as C_{1a}, C_{2a}, in upper unit and C_{3a}, C_{4a} in lower unit connected to a neutral point (N_{ca}) to maintain common DC voltage as $V_{dc.L}$. The schematic model of proposed DCMLI-MDUPQC is depicted in Figure 2. The synthetization of various switching actions produce the 5-level output voltage at load terminals to drive the MD-UPQC with voltage levels of $V_{dca}/4$; $V_{dca}/2$; $0V_{dca}$; $-V_{dca}/4$ and $-V_{dca}/2$, respectively. The switching arrangement of 5-level DCMLI structure is represented in Table 1. This switching action shows, "1" represents the conducted switches and "0" represents the non-conducted switches in a 5-level DCMLI switching arrangement.
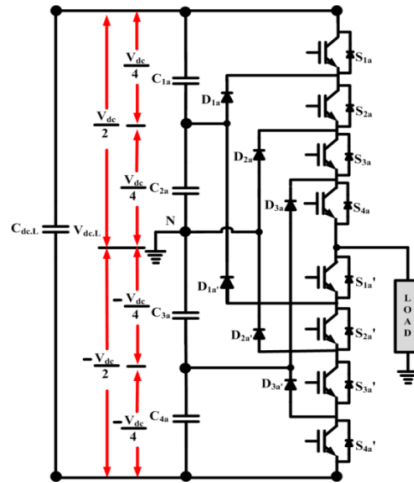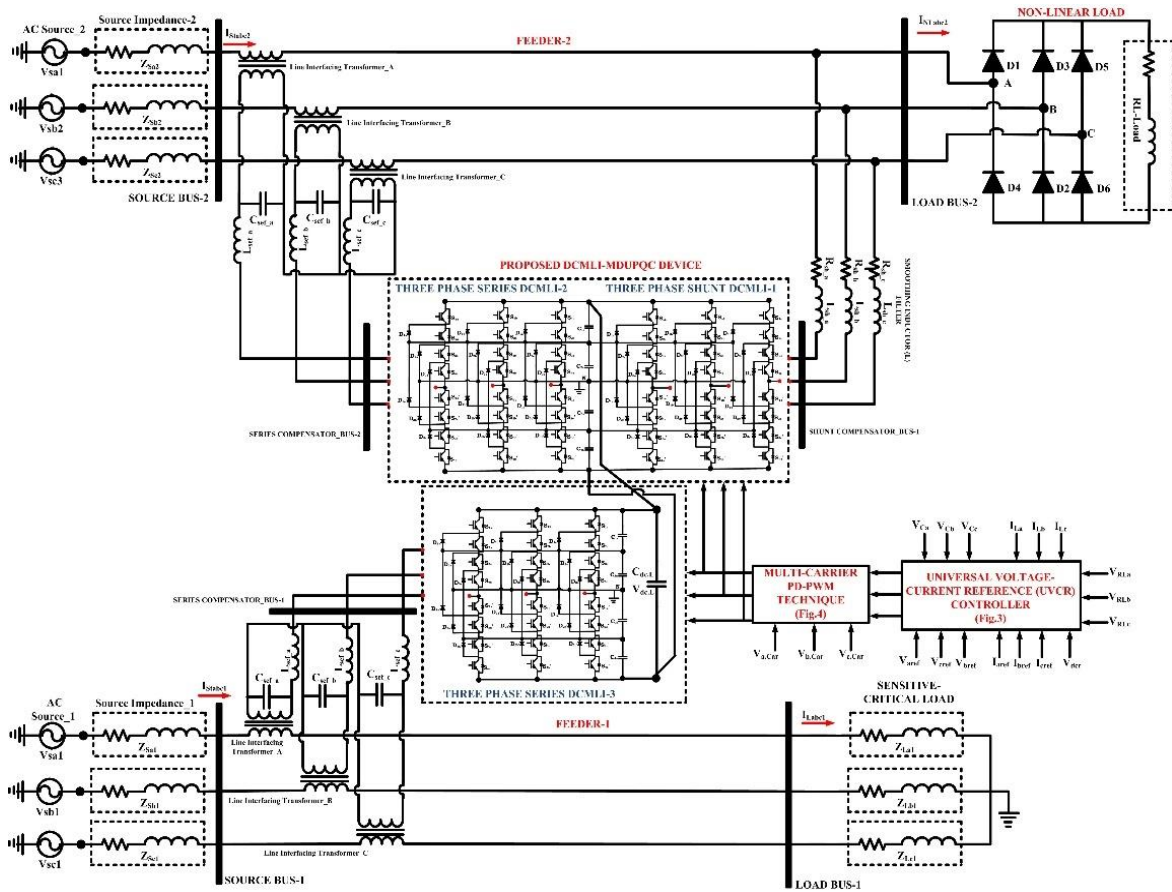
Figure 1. Model of 5-level DCMLI structure

Figure 2. Schematic model of proposed DCMLI-MDUPQC

Table 1. Switching arrangement of 5-level DCMLI structure

DCMLI Voltage (Vo)	Switching Arrangement							
	S_{1a}	S_{2a}	S_{3a}	S_{4a}	S_{1a}'	S_{2a}'	S_{3a}'	S_{4a}'
$V_{dca}/4$	0	1	1	1	1	0	0	0
$V_{dca}/2$	1	1	1	1	0	0	0	0
$0\ V_{dca}$	0	0	1	1	1	1	0	0
$-V_{dca}/4$	0	0	0	1	1	1	1	0
$-V_{dca}/2$	0	0	0	0	1	1	1	1

3.   PROPOSED UVCR CONTROLLER

The switching action of DCMLI of MD-UPQC device is controlled by using suitable switching states with extraction of reference voltage-current signals via proposed UVCR control scheme. The proposed UVCR scheme doesn't requires any phase transformation techniques and producing the reference signals with a low computational delay over the classical abc-dq transform extraction schemes. It delivers reference signals by sensing load voltage which develops unit-vector signals through pre-synchronize angle (θ_s) received from discrete phase-lock loop (D-PLL). Schematic model of proposed UVCR control scheme for DCMLI based MDUPQC device is depicted in Figure 3. The unit-vector module composes the non-complex vector signals which are described in (1) & (2) as, the sensed load voltage is represented as (1).

$$V_{L.a} = V_{st.a} \, sin\theta s$$
$$V_{L.b} = V_{st.b} \, sin\left(\theta s - {}^{2\pi}/_3\right)$$
$$V_{L.c} = V_{st.c} \, sin\left(\theta s + {}^{2\pi}/_3\right) \qquad (1)$$

The non-complex unit-vector signal is represented as (2).

$$V_{st.abc} = \left\{\frac{2}{3}\left(V_{L.a}^2 + V_{L.b}^2 + V_{L.c}^2\right)\right\}^{1/2} \qquad (2)$$

The extracted non-complex vector signals are defined as in-phase quadrature components represented as (3).

$$UV_{st.a} = \frac{V_{L.a}}{V_{st.abc}} = sin\theta s$$
$$UV_{st.b} = \frac{V_{L.b}}{V_{st.abc}} = sin\left(\theta s - {}^{2\pi}/_3\right)$$
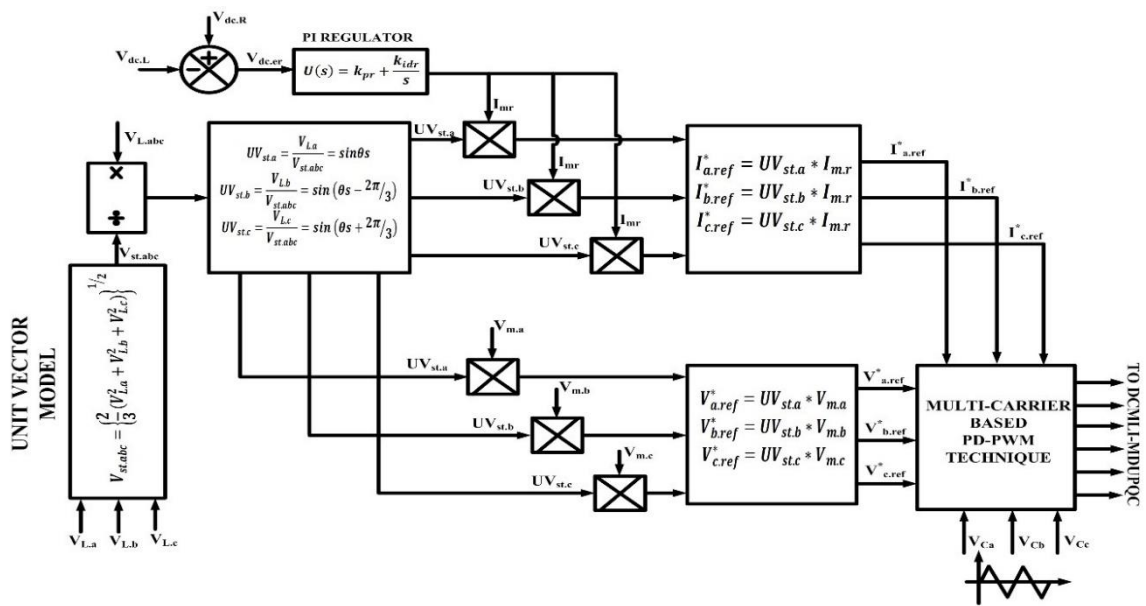$$UV_{st.c} = \frac{V_{L.c}}{V_{st.abc}} = sin\left(\theta s + {}^{2\pi}/_3\right) \qquad (3)$$

Figure 3. Schematic model of proposed UVCR control scheme for DCMLI based MDUPQC device

The extracted non-complex vector signals ($UV_{st.abc}$) is propagated with measured voltage signal ($V_{m.abc}$) for extracting reference voltage signal ($V_{abc.ref}^*$) to series MLI-2 and series MLI-3 of DCMLI of MD-UPQC device is described as (4).

$$V_{a.ref}^* = UV_{st.a} * V_{m.a}$$
$$V_{b.ref}^* = UV_{st.b} * V_{m.b}$$
$$V_{c.ref}^* = UV_{st.c} * V_{m.c} \qquad (4)$$

The extracted non-complex vector signals ($UV_{st.abc}$) is propagated with measured current signal ($I_{m.r}$) for extracting reference current signal ($I^*_{abc.ref}$) to shunt MLI-1 of DCMLI of MD-UPQC device is described as (5).

$$I^*_{a.ref} = UV_{st.a} * I_{m.r}$$
$$I^*_{b.ref} = UV_{st.b} * I_{m.r}$$
$$I^*_{c.ref} = UV_{st.c} * I_{m.r} \tag{5}$$

The reference current signal ($I_{m.r}$) is received from feed-forward DC voltage controller which reduces the loss components and eliminate the circulation currents in input DC capacitors of DCMLI. Also, it maintains DC voltage as constant by comparing the measured DC voltage ($V_{dc.L}$) and reference DC voltage ($V_{dc.R}$) and creates error signals. These error signals are counteracted with proportional-integral (PI) regulator and establish the active reference current signals described as (6) and (7).

$$V_{dc.er} = V^*_{dc.R} - V_{dc.L} \tag{6}$$

$$I_{m.r} = K_{pr} * \left(V_{dc.er(k)} - V_{dc.er(k-1)}\right) + K_{ir} * \left(V_{dc.er(k)}\right) \tag{7}$$

The proposed UVCR control scheme extracts reference voltage-current signals and the actual signals are propagated with multi-carrier based pulse-width modulation (MCB-PWM) technique for generation of feasible switching pattern to DCMLI-MDUPQC device. Several MCB-PWM techniques are available for MLI structures and classification is relied on shifting of carrier position such as phase-opposition disposition (POD), phase-disposition (PD) and alternate phase-opposition disposition (APOD), respectively. The PD technique is considered here and N-1 carriers are required for generation of N number of voltage levels; 4 carriers are required for generation of 5-level output voltage. The representation of multi-carrier based phase-disposition pulse-width modulation (PD-PWM) technique is depicted in Figure 4.
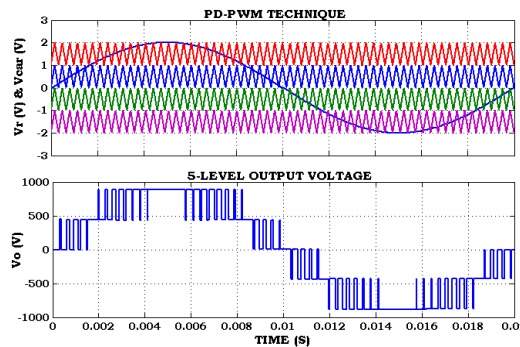

Figure 4. Multi-carrier based PD-PWM technique

4.   RESULTS & DISCUSSION

The operation of proposed model and control scheme are discussed, the performance of proposed DCMLI-MDUPQC structure is evaluated with MATLAB/Simulink computational tool and simulation results are presented. The system parameters and their values of proposed UVCR controlled DCMLI-MDUPQC device is considered in [18] and represented in Table 2.

Table 2. Proposed system parameters and values

S. No	Parameters	Values	
		Feeder-2	Feeder-1
1	Source Terminal Voltage (V_{rms})	V_{sf1}- V_{sf2}-415Vrms, 50Hz	
2	Load Specifications	Non-Linear PE Load in Feeder-2 $V_{L.2}$=415Vrms, 50Hz, R_{L1}=30 Ω, L_{L1}-20 mH	Sensitive Load in Feeder-1 $V_{L.1}$=415Vrms, 50 Hz $P_{Load.1}$=10KW, $Q_{Load.1}$=5KVar
3	Feeder Impedance	R_{sf}=0.15Ω, L_{sf}-0.9mH	
4	1:1 Line Connected Transformer	415V, 5KVA, Linear type, 10% of Leakage Reactance	
5	Carrier Switching Frequency	Fc-3050Hz, MI-1	
6	Shunt-MLI Line Compensated Filter	$R_{sh.2}$= 0.001 Ω, $L_{sh.2}$-10 mH	
7	Series-MLI Line Compensated Filter	$L_{se.12}$- 3mH, $C_{se.12}$-100μF	
8	Common DC-Link Capacitor	$C_{dc.L}$ =1500μF, $V_{dc.L}$= 880V	

4.1. Compensation of voltage and current associated PQ problems in feeder-2 using proposed UVCR controlled DCMLI-MDUPQC Device

The simulation results of proposed UVCR controlled shunt MLI-1 of DCMLI-MDUPQC device in feeder-2 for compensation of harmonic currents is depicted in Figures 5 (a)-(d). The three-phase multi-feeder distribution network is used to drive the non-linear diode-bridge rectifier load with a source terminal voltage of 415 Vrms, 50 Hz supply. The critical non-linear diode-bridge load creates the harmonic distortions in source current proliferates the other loads connected at common point. These harmonic currents affecting the functioning of other loads and produces high losses, more heat and damaging the feeder specifications is shown in Figure 5 (a). These harmonic currents are mitigated by employing shunt MLI-1 of MD-UPQC operated as in-phase current compensation principle. Also, it regulates the load reactive power, source power factor, and load balancing, maintaining the system specifications as linear, sinusoidal and balanced nature in feeder-2. The total harmonic distortion (THD) value of source terminal current in feeder-2 is measured as 1.47% is shown in Figure 5 (b), it is complying with IEEE standards and the THD of non-linear rectifier load current in feeder-2 is measured as 30.19% is shown in Figure 5 (c). Moreover, the source current seems as in-phase with thesource terminal voltage which shows the unity power factor in feeder-2 is shown in Figure 5 (d).
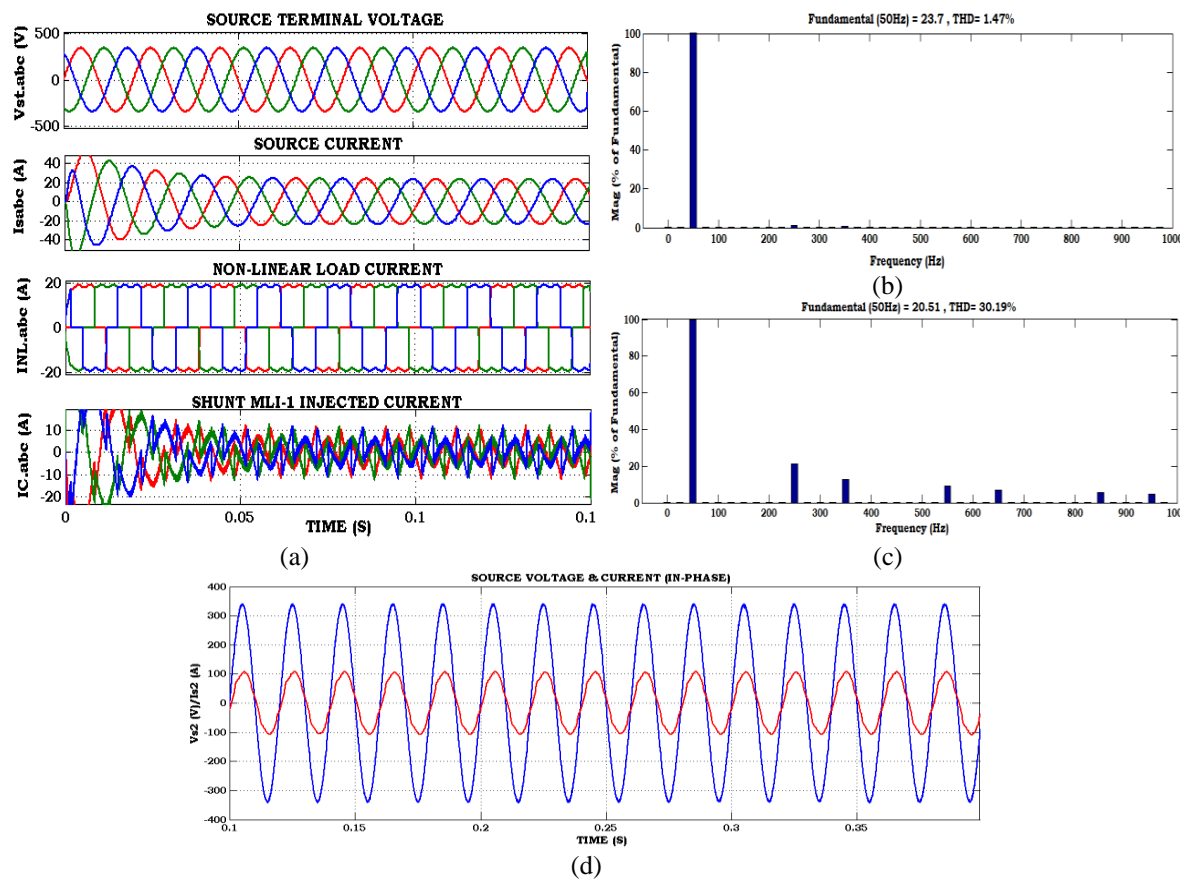

Figure 5. Simulation results shows (a) proposed UVCR controlled shunt MLI-1 of DCMLI-MDUPQC device in feeder-2, (b) THD of source current in feeder-2, (c) THD of non-linear PE load current in feeder-2 and (d) source current in-phase with source voltage

The simulation results of proposed UVCR controlled series MLI-2 of DCMLI-MDUPQC device infeeder-2 for compensation of voltage harmonics, voltage sags-swells, is depicted in Figures 6 (a)-(c). During pre-sag condition source terminal voltage is retained as constant, then voltage-sag is occurred at a time instant of 0.15 sec <t<0.25 sec and the value of source terminal voltage is decreased to 170V. But the load voltage is unaffected and retained as constant of 340V, due to presence of series MLI-2 in feeder-2. It compensates voltage sag problem and inject required voltage as 170V to drive the non-linear load as balanced nature. During pre-swell condition source terminal voltage is retained as constant, then voltage-swell is occurred at a time instant of 0.35 sec <t<0.45 sec and the value of source terminal voltage is

increased to 510 V. But the load voltage is unaffected and retained as constant of 340 V, due to presence of series MLI-2 in feeder-2. It compensates voltage swell problem and extracts required voltage as 170 V to drive the non-linear load as balanced nature. The terminal voltage consists of non-sinusoidal voltage harmonics occurred between 0.5 sec <t<0.6 sec, affecting the common-point or consumer end-point.

These harmonic voltages affecting the functioning of other loads and produces high losses, more heat and damaging the feeder specifications. These harmonic voltages are mitigated by employing series MLI-2 of MD-UPQC operated as in-phase voltage compensation principle. Also, it regulates the load reactive power, source power factor, and load balancing, maintaining the system specifications as linear, sinusoidal and balanced nature in feeder-2 is shown in Figure 6 (a). The THD value of non-linear load voltage in feeder-2 is measured as 0.5%is shown in Figure 6 (b), it is complying with IEEE standards and the THD value of source terminal voltage in feeder-2 during voltage harmonics is measured as 20.62% is shown in Figure 6 (c).
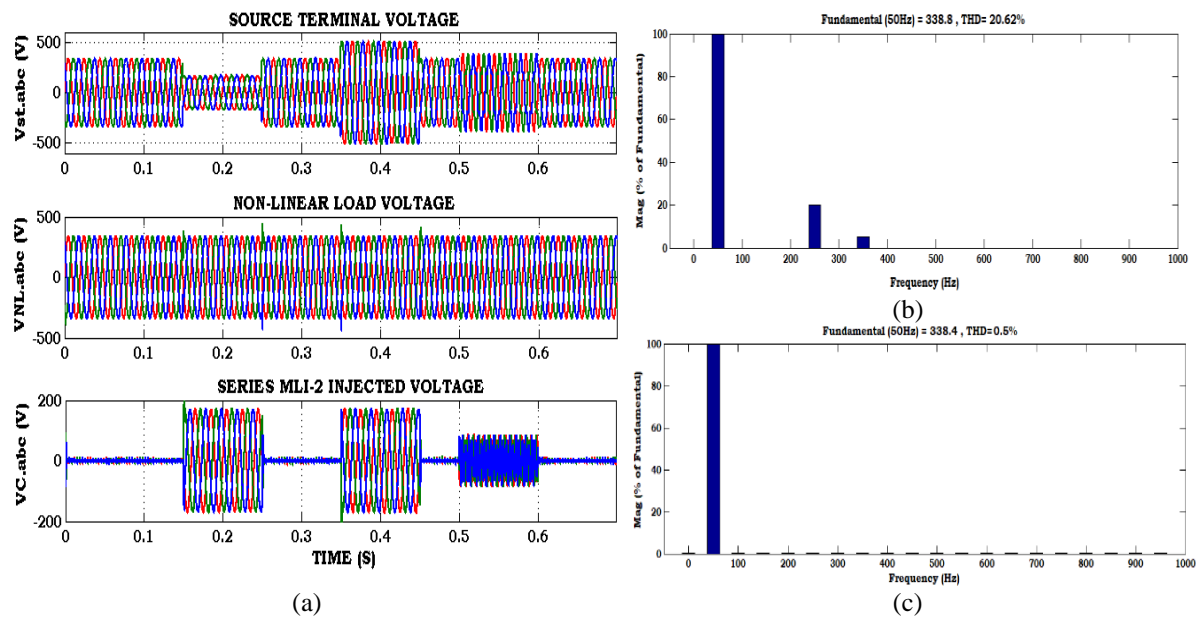

Figure 6. Simulation results shows (a) proposed UVCR controlled series MLI-2 of DCMLI-MDUPQC device in Feeder-2, (b) THD of critical non-linear load voltage, and (c) THD of source terminal voltage

The proposed series MLI-2 of MD-UPQC compensates all voltage problems and maintains load voltage as sinusoidal and fundamental nature to drive the non-linear load as balanced condition. The THD comparison of source & load voltages in feeder-2 of traditional 3-level VSI & proposed 5-level DCMLI based MD-UPQC device is illustrated in Table 3. The THD comparison of source & load currents in feeder-2 of traditional 3-level VSI & proposed 5-level DCMLI based MD-UPQC device is illustrated in Table 4. The active and reactive powers of source, injected compensator and critical load of DCMLI-MDUPQC Device in Feeder-2 are depicted in Figure 7. The calculated power values of source, compensator and load in Feeder-2 of proposed 5-level DCMLI-MD UPQC device under voltage associated PQ problems is illustrated in Table 5.

Table 3. THD comparison of source & load voltages in feeder-2 of traditional 3-level VSI &proposed 5-level DCMLI based MD-UPQC device

THD (%)	Source Voltage			Load Voltage			Output Voltage		
	a	b	c	a	b	c	a	b	c
Traditional 3-Level VSI Based MD-UPQC [10]	20.62%	20.62%	20.62%	1.72%	1.63%	1.71%	91.7%	89.03%	90.3%
Proposed 5-Level DCMLI Based MD-UPQC	20.62%	20.62%	20.62%	0.89%	0.91%	0.83%	27.5%	27.3%	27.3%

Table 4. THD comparison of source & load currents in feeder-2 of traditional 3-level VSI & proposed 5-level DCMLI based MD-UPQC device

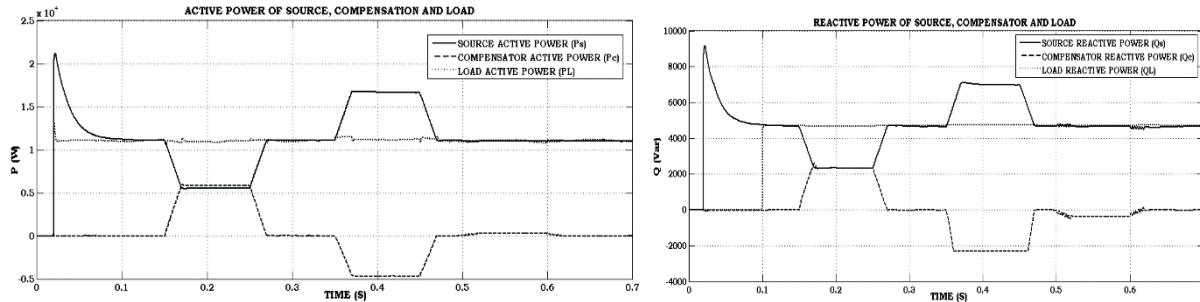| THD (%)	Source Current			Load Current		
	a	b	c	a	b	c
Traditional 3-Level VSI Based MD-UPQC [10]	5.12%	5.09%	5.48%	30.14%	30.04%	30.06%
Proposed 5-Level DCMLI Based MD-UPQC	1.47%	1.60%	1.58%	30.19%	29.97%	30.11%

Figure 7. Active and reactive powers of source, injected compensator, critical load of DCMLI-MDUPQC device in feeder-2

Table 5. Power calculation of source, compensator and load values in feeder-2 of proposed 5-level DCMLI Based MD-UPQC device under voltage associated PQ problems

Power	Pre-Condition			Voltage-Sag			Voltage-Swell		
	Source	Inject	Load	Source	Inject	Load	Source	Extract	Load
Active Power (W)	11.1 KW	0 KW	11.05 KW	5.5 KW	5.55 KW	11.05 KW	15.95 KW	4.9 KW	11.05 KW
Reactive Power (Var)	4.7 KVar	0 KVar	4.7 KVar	2.4 KVar	2.3 KVar	4.7 KVar	7 KVar	2.3 KVar	4.7 KVar

4.2. Compensation of voltage associated PQ problems in feeder-1 using proposed UVCR controlled DCMLI-MDUPQC device

The simulation results of proposed UVCR controlled series MLI-3 of DCMLI-MDUPQC device in feeder-1 for compensation of voltage harmonics, voltage sags-swells, and voltage deviations is depicted in Figures 8 (a)-(c). The terminal voltage consists of non-sinusoidal voltage harmonics, voltage-sag-swells and voltage deviation, affecting the common-point or consumer end-point. During pre-sag condition source terminal voltage is retained as constant, then voltage-sag is occurred at a time instant of 0.2 sec <t<0.3 sec and the value of source terminal voltage is decreased to 170V. But the load voltage is unaffected and retained as constant of 340V, due to presence of series MLI-3 in feeder-1. It compensates voltage sag problem and inject required voltage as 170V to drive the non-linear load as balanced nature. During pre-swell condition source terminal voltage is retained as constant, then voltage-swell is occurred at a time instant of 0.4 sec <t<0.5 sec and the value of source terminal voltage is increased to 510V. But the load voltage is unaffected and retained as constant of 340V, due to presence of series MLI-3 in feeder-1. It compensates voltage swell problem and extracts required voltage as 170V to drive the non-linear load as balanced nature.

During harmonic condition at a time instant of 0.6 sec <t<0.7 sec, series MLI-3 in feeder-1 of MD-UPQC counteracts the 5th and 7th harmonic and injects the required voltage as in-phase compensation strategy and maintains harmonic-free, sinusoidal and fundamental with a value of 340V is shown in Figure 8 (a). The THD value of sensitive load voltage in feeder-1 is measured as 0.89% is shown in Figure 8 (b) it is complying with IEEE standards and the THD value of source terminal voltage in feeder-1 during voltage harmonics is measured as 20.62% is shown in Figure 8 (c). The proposed series MLI-3 of MD-UPQC compensates all voltage problems and maintains load voltage as sinusoidal and fundamental nature to drive the sensitive load as balanced condition. During pre-voltage deviation condition source terminal voltage is retained as constant, then voltage-deviations is occurred at a time instant of 0.75 sec <t<0.85 sec and the value of source terminal voltage is decreased to 0V. But the load voltage is unaffected and retained as constant of 340V, due to presence of series MLI-3 in feeder-1. It compensates voltage deviations problem and inject required voltage as 340V to drive the sensitive load as balanced nature. The THD comparison of source, load voltage and VSI output voltages in both feeder-1 and feeder-2 of traditional 3-level VSI & proposed 5-level DCMLI based MD-UPQC device is illustrated in Table 6.
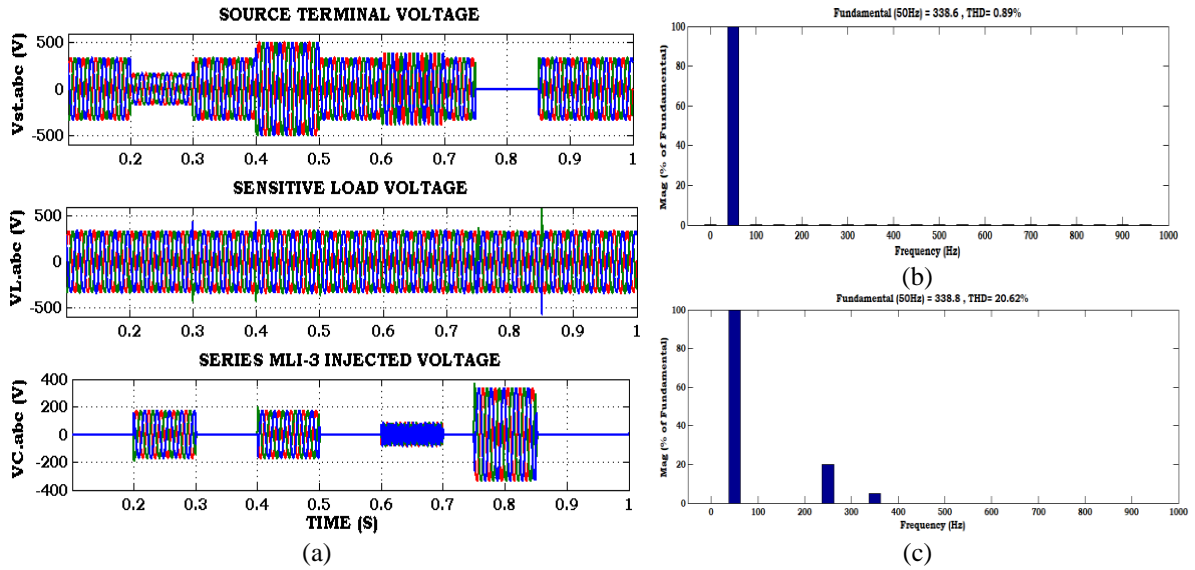
Figure 8. Simulation results shows (a) proposed UVCR controlled series MLI-3 of DCMLI-MDUPQC device in feeder-1, (b) critical non-linear load voltage in feeder-1 THD values of source terminal voltage, and (c) THD of source terminal voltage

Table 6. THD comparison of source & load values in feeder-1 of traditional 3-level VSI &proposed 5-level DCMLI based MD-UPQC device

THD (%)	Source Voltage			Load Voltage			VSI Output Voltage		
	a	b	c	a	b	c	a	b	c
Traditional 3-Level VSI Based MD-UPQC [10]	20.62%	20.62%	20.62%	1.84%	1.75%	1.89%	91.7%	89.03%	90.3%
Proposed 5-Level DCMLI Based MD-UPQC	20.62%	20.62%	20.62%	0.5%	0.61%	0.58%	27.5%	27.3%	27.3%

The power calculation of source, compensator and load values in feeder-1 of proposed 5-Level DCMLI based MD-UPQC is illustrated in Table 7. The required active, reactive power of feeder-1 is retained as constant by using MD-UPQC device to drive the sensitive load; the voltage across capacitor is retained as constant of 1760 V through voltage controller as depicted in Figure 9.

Table 7. Power calculation of source, compensator and load values in feeder-1 of proposed 5-level DCMLI based MD-UPQC device under voltage associated PQ problems

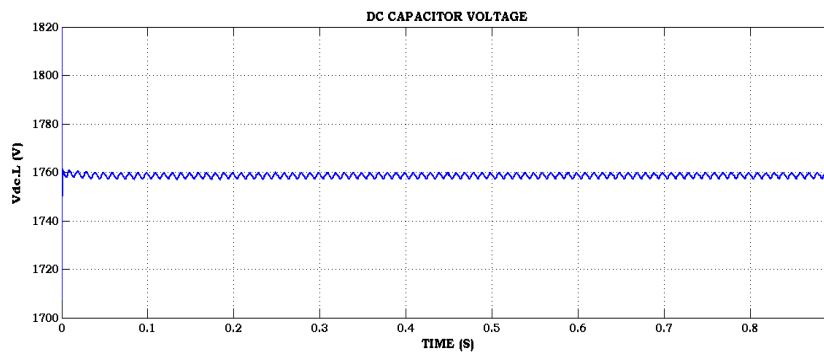| Power	Pre-Condition			Voltage-Sag			Voltage-Swell			Voltage Deviations		
	Source	Inject	Load	Source	Inject	Load	Source	Extract	Load	Source	Inject	Load
Active Power (W)	10 KW	0 KW	10 KW	5 KW	5 KW	10 KW	15 KW	5 KW	10 KW	0 KW	10 KW	10 KW
Reactive Power (Var)	5 KVar	0 KVar	5 KVar	2.5 KVar	2.5 KVar	5 KVar	7.5 KVar	2.5 KVar	5 KVar	0 KVar	5 KVar	5 KVar

Figure 9. Voltage across common DC capacitor

5. CONCLUSION

The capability of proposed DCMLI topology of MD-UPQC relies on ability of maximum injected current and voltages during particular PQ problem and the required power that can be delivered to load during the both voltage and current associated PQ problems. The proposed 5-level DCMLI topology reduces the common-mode voltage, reverse-voltage blocking capability, low dv/dt and di/dt stress, low EMI loss and maximizing the compensation efficiency, etc. Likewise, the proposed UVCR control scheme reduces the complex dual-transformations and mathematical analysis, high delayed signals for generation of reference current/voltage signals to drive the 5-level DCMLI-MDUPQC device. The performance evaluation of proposed UVCR controlled 5-level DCMLI-MDUPQC topology is verified through MATLAB/Simulink computational tool and simulation results are presented complying with IEEE-519 standards to attain good compensation features. The further work can be carried on reduced-switch multilevel inverter of MD-UPQC device for getting good compensation features with fewer switching elements.

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