

# NPN Sziklai pair small-signal amplifier for high gain low noise submicron voltage recorder

Sachchida Nand Shukla, Syed Shamroz Arshad, Geetika Srivastava

Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University, Uttar Pradesh, India

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## ABSTRACT

Small signal-to-noise ratio (SNR) and multiple noise sources, coupled with very weak signal amplitudes of bio signals make brain-computer interface (BCI) application studies a challenging task. The front-end recorder amplifiers receive very-weak signal (few  $\mu\text{V}$ ) from high impedance electrodes and for efficient processing of such weak and low frequency ( $<1$  kHz) signals a high gain amplifier with very low operating voltage and low total harmonic distortion (THD) is required. Existing amplifiers suffer from problem of high non-linearity and low common mode rejection. A good sense amplifier at predeceasing stage can solve this problem. Utilizing very high amplification factor of Sziklai Pair, this paper proposes two circuit topologies of common-emitter and common-collector negative-positive-negative (NPN) Sziklai Pair small signal amplifiers suitable for use in preamplifier stages of such signal acquisition circuit. Present study provides broad-spectrum of analysis of these amplifiers covering effect of additional biasing resistance  $R_A$ , variation of 'ideal forward maximum beta'  $\beta$ , temperature dependency, noise sensitivity and phase variation. The tunable capability of first topology makes it a suitable candidate in wide variety of other applications. The first amplifier operates on very low input voltage range ( $0.1 \mu\text{V}$ - $6 \text{ mV}$ ) whereas the second amplifier works on  $100 \mu\text{V}$ - $11 \text{ mV}$  range of input voltage.

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## Corresponding Author:

Geetika Srivastava

Department of Physics and Electronics, Dr. Ram Manohar Lohia Avadh University

Hawai Patti, Allahabad Road, Ayodhya-224001, Uttar Pradesh, India

Email: geetika\_gkp@rediffmail.com

## 1. INTRODUCTION

Low frequency small signal voltage measurement in submicron region ( $<1 \mu\text{m}$ ) is a challenging task especially with noisy, non-stationary sources such as bio-signals. Correct measurement with very high gain, high sensitivity amplifiers is the key to reliable results [1]. There is a practical limit to gain of available semiconductor devices for amplifier design and it forces use of multi stage design for high gain. Multistage amplifiers not only occupy large area but also suffer from low noise immunity and high harmonic distortion. Various attempts have been made in past to increase device gain such as use of Darlington pair and Sziklai pair in place of bipolar-junction-transistor (BJT). Sziklai offer lower turn on voltage but its performance depends greatly on matched parameters of used pair of transistors. There is not much reported work available on circuit arrangement and amplifier based on these device configurations [2].

This paper deals with novel arrangement of negative-positive-negative (NPN) Sziklai pair amplifier with varying biasing arrangement and matched BJT pair combination under common-emitter (CE) and common-collector (CC) configurations [3]. CE amplifiers are most common fundamental amplifying circuit that produces undistorted output as long as the small-signal base-emitter voltage ( $v_{be}$ ) is less than thermal

voltage ( $V_T$ ) [4]. Emitter resistance  $R_E$  provides negative feedback which enhances current gain and reduces distortions in the amplified output with  $180^\circ$  phase shift [5]. Conventionally, CE amplifiers have wide application in audio amplifiers, basic switch for logic circuits, general analog amplifiers, speakers, microcontrollers and DC motors due to moderate voltage and current gain with moderate input and output impedances [6]. The CC amplifiers produces nearly unit voltage gain, high current gain. Its output emitter voltage follows input base voltage, and the input impedance is much higher than output impedance [7]. CC amplifier is frequently employed as a voltage buffer and used for impedance matching [8]. CC amplifiers have relatively better frequency response and less distortion in comparison to CE and Common-Base (CB) amplifiers [9].

Sziklai pair, named after its Hungarian inventor George Sziklai, works as high gain amplifier similar to Darlington pair but it requires only half turn-ON base-emitter voltage ( $V_{BE}=0.625$  volt) than Darlington pair ( $V_{BE}=1.36$  Volts) [10]. A major advantage associated with Sziklai pair small-signal amplifiers is that it has better response at higher frequencies than Darlington pair small-signal amplifiers [11]. At higher frequencies the matched Sziklai pair device current gain is  $\beta^2$  whereas for unmatched Sziklai pair it is  $\beta_1 \times \beta_2$  [12]. The lower quiescent current makes Sziklai pair thermally stable than Darlington pair and also shows better linearity [13]. This paper covers detailed analysis of NPN Sziklai pair small-signal amplifiers under CE and CC configurations with matched pair of BJTs. Two circuit topologies proposed in this paper overcome the narrow bandwidth problem of PNP Sziklai pair small-signal amplifier and also removes the poor response problem of conventional Darlington pair small-signal pair amplifier at higher frequencies [14].

## 2. CIRCUIT DESCRIPTION AND RESEARCH METHOD

Two circuit topologies, proposed in this paper, are the circuit models of NPN Sziklai pair small-signal amplifier. Circuit-1 amplifier under the CE configuration is shown in Figure 1 (a) and circuit-2 amplifier under the CC configuration is shown in Figure 1 (b). The Sziklai pair CE amplifier uses matched pair of user defined simulation program with integrated circuit emphasis (SPICE) model of NPN transistor QN ( $\beta=250$ ) and PNP transistor QP ( $\beta=250$ ) with  $R_S=1\ \Omega$ ,  $R_1=81\ \text{K}\Omega$ ,  $R_2=47\ \text{K}\Omega$ ,  $R_C=9\ \text{K}\Omega$ ,  $R_E=5\ \Omega$ ,  $R_L=800\ \Omega$ ,  $C_1=10\ \mu\text{F}$ ,  $C_2=10\ \mu\text{F}$ ,  $C_E=100\ \mu\text{F}$ ,  $V_{CC}=+25\ \text{V}$ . The second configuration of Sziklai pair CC amplifier user defined SPICE model of NPN transistor QN ( $\beta=50$ ) and PNP transistor ( $\beta=50$ ) with components  $R_S=1\ \Omega$ ,  $R_1=50\ \text{M}\Omega$ ,  $R_2=50\ \text{M}\Omega$ ,  $R_E=19\ \text{K}\Omega$ ,  $R_L=10\ \text{K}\Omega$ ,  $C_1=0.1\ \mu\text{F}$ ,  $C_L=10\ \mu\text{F}$  and  $V_{CC}=+25\ \text{V}$ .

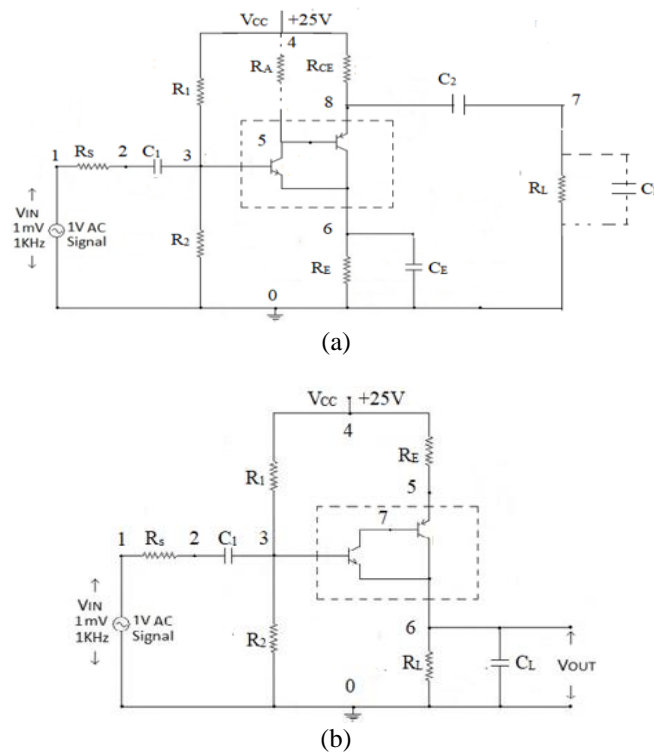


Figure 1. Sziklai pair small-signal amplifier for (a) CE-configuration and (b) CC-configuration

As the designed amplifier circuits use NPN-type transistor at driver position and PNP-type transistor at follower position, hence it is termed as NPN-type Sziklai pair small-signal amplifier. Device structure of the CE amplifier operates with base voltage 9.1789 V at node 3 and 8.8499 V at node 5 whereas for CC amplifier it works with base voltage 6.6306 V at node 3 and 12.8820 V volt at node 7. Table 1 and Table 2 lists all the simulation parameters used in modeling of transistors and the operating point.

Table 1. Simulation parameters

Simulation Parameters	Under Sziklai CE-mode		Under Sziklai CC-Mode	
	QN1 (NPN BJT)	QP1 (PNP BJT)	QN2 (NPN BJT)	QP2 (PNP BJT)
IS (p-n saturation current)	100.00E-18	100.00E-18	200.00E-18	200.00E-18
BF (Ideal maximum forward beta)	250	250	50	50
NF (Forward current emission coefficient)	1	1	1	1
BR (Ideal maximum reverse beta)	10	10	1	1
NR (Reverse current emission coefficient)	1	1	1	1
RB (Zero-bias (maximum) base resistance)	0.1	0.1	5	5
RC (Collector ohmic resistance)	0.1	0.1	1	1
RE (Emitter Ohmic resistance)	200.00E-12	200.00E-12	200.00E-12	200.00E-12
TF (Ideal forward transit time)	5.00E-09	5.00E-09	5.00E-09	5.00E-09
TR (Ideal reverse transit time)	2.42	2.2	2.42	2.2
CN (Base-Collector leakage emission coefficient)	0.87	0.52	0.87	0.52

Table 2. Description of operating point parameters

Operating Point Parameter	Under Sziklai CE-mode		Under Sziklai CC-Mode	
	QN1 (NPN BJT)	QP1 (PNP BJT)	QN2 (NPN BJT)	QP2 (PNP BJT)
IB (Current Flowing into base)	27.2 nA	-6.8 $\mu$ A	23.5 $\mu$ A	-0.117 $\mu$ A
IC (Current flowing into collector)	6.8 $\mu$ A	-1.7 mA	11.7 $\mu$ A	-0.58 mA
VBE (Voltage across base-emitter junction)	0.64 V	-0.79 V	0.64 V	-0.74 V
VBC (Voltage across base-collector junction)	0.32 V	0.31 V	-6.25 V	6.89 V
VCE (Voltage across collector emitter junction)	0.31 V	-1.11 V	6.89 V	-7.64 V
BETA DC (Small Signal DC Current gain)	250	250	50	50
GM (Small Signal Transconductance)	0.26 mA/V	65.7 mA/V	0.45 mA/V	0.227 mA/V
RPI (Small Signal AC Base Emitter Resistance)	0.95 M $\Omega$	3.80 K $\Omega$	0.11 M $\Omega$	2.20 K $\Omega$
RO (Small Signal AC collector emitter resistance)	0.77 G $\Omega$	1 T $\Omega$	1 G $\Omega$	1.00 G $\Omega$
BETA AC (Small-signal AC Current gain)	250	250	50	50

### 3. RESULTS AND DISCUSSION

#### 3.1. Performance parameters

The SPICE simulation values of various performance parameters of circuit-1 and circuit-2 are recorded at room temperature 27 °C and listed in Table 3. As evident from Table 3 that under the SPICE user defined model of paired BJTs, Sziklai pair small-signal amplifier in CE configuration gives higher gain and wider bandwidth than the CC configuration. The properties of circuit-1 show that this amplifier when followed by Transimpedance amplifier (TIA) can result in high bandwidth at the receiver end for high-speed communication system [15]. The CC Sziklai (circuit-2) amplifier functions over the frequency range extended up to 383.728 Hz and capable of amplifying low-range signal ( $\mu$ V-mV) therefore it may be used in the preamplifier stages of an electroencephalography (EEG) signal acquisition circuit [16].

The ratio of the output-to-input current and output-to-input voltage of circuit-2 (NPN Sziklai under CC) in transient analysis are much high since it uses common-collector configuration which has high negative feedback imposed by emitter resistor and in-built negative feedback of the Sziklai pair itself [17]. Both the proposed circuit topologies are analyzed with combinations of BJT models, where Case-A1, B1 correspond to circuit-1 and Case-A2, B2 correspond to circuit-2.

- Case–A1: The default model of NPN driver transistor Q2N2222 ( $\beta=255.9$ ) and for PNP follower transistor user defined model QP ( $\beta=250$ ) along with  $R_S=1 \Omega$ ,  $R_1=95 \text{ K}\Omega$ ,  $R_2=54 \text{ K}\Omega$ ,  $R_C=9 \text{ K}\Omega$ ,  $R_E=5 \Omega$ ,  $R_L=400 \Omega$ ,  $C_1=10 \mu\text{F}$ ,  $C_2=10 \mu\text{F}$ ,  $C_E=100 \mu\text{F}$ ,  $V_{CC}=+25 \text{ V}$  and AC input signal source= 1 V, 1 KHz; and the performance parameters obtained are  $A_{IGA}=1,956.6$ ,  $A_{IGA-RMS}=1,917.4$ ,  $A_{VGA}=25.025$ ,  $A_{VGA-RMS}=24.897$ ,  $F_L=106.249 \text{ Hz}$ ,  $F_H=183.889 \text{ KHz}$ ,  $B_W=183.783 \text{ KHz}$ ,  $A_{IGD}=22,089$ ,  $A_{IGD-RMS}=22,082$ ,  $A_{VGD}=25.038$ ,  $A_{VGD-RMS}=24.913$ ,  $P_G$  (in Watt)=48,963.91,  $P_G$  (in dB-Watt)=46.898,  $V_1=0.9991 \text{ mV}$ ,  $V_7=26.033 \text{ mV}$ , Ratio  $V_7/V_1=26.056$ ,  $I(R_S)=31.461 \text{ nA}$ ,  $I(R_L)=65.216 \mu\text{A}$ , Ratio  $I(R_L)/I(R_S)=20.729$ ,  $\theta^\circ = -174.233$  and total harmonic distortion (THD)=0.9%.
- Case–B1: NPN driver transistor is user defined model of QN ( $\beta=250$ ) and PNP follower transistor is default model Q2N2907A ( $\beta=231.7$ ) along with  $R_S=1 \Omega$ ,  $R_1=90 \text{ K}\Omega$ ,  $R_2=52 \text{ K}\Omega$ ,  $R_C=9 \text{ K}\Omega$ ,  $R_E=5 \Omega$ ,  $R_L=700 \Omega$ ,  $C_1=10 \mu\text{F}$ ,  $C_2=10 \mu\text{F}$ ,  $C_E=100 \mu\text{F}$ ,  $V_{CC}=+25 \text{ V}$  and AC input signal source= 1 V, 1 KHz and the performance parameters obtained are  $A_{IGA}=1,952.1$ ,  $A_{IGA-RMS}=1,934.7$ ,  $A_{VGA}=43.071$ ,  $A_{VGA-RMS}=42.913$ ,  $F_L=106.249 \text{ Hz}$ ,  $F_H=183.889 \text{ KHz}$ ,  $B_W=183.783 \text{ KHz}$ ,  $A_{IGD}=22,089$ ,  $A_{IGD-RMS}=22,082$ ,  $A_{VGD}=25.038$ ,  $A_{VGD-RMS}=24.913$ ,  $P_G$  (in Watt)=48,963.91,  $P_G$  (in dB-Watt)=46.898,  $V_1=0.9991 \text{ mV}$ ,  $V_7=26.033 \text{ mV}$ , Ratio  $V_7/V_1=26.056$ ,  $I(R_S)=31.461 \text{ nA}$ ,  $I(R_L)=65.216 \mu\text{A}$ , Ratio  $I(R_L)/I(R_S)=20.729$ ,  $\theta^\circ = -174.233$  and total harmonic distortion (THD)=0.9%.

$R_{MS}=42.668$ ,  $F_L=106.278$  Hz,  $F_H=80.911$  KHz,  $B_W=80.805$  KHz,  $A_{IGD}=55,978$ ,  $A_{IGD-RMS}=55,978$ ,  $A_{VGD}=43.075$ ,  $A_{VGD-RMS}=42.683$ ,  $P_G$  (in Watt)=84,078.89,  $P_G$  (in dB-Watt)=49.246,  $V_I=0.9991$  mV,  $V_7=44.917$  mV, Ratio  $V_7/V_I=44.957$ ,  $I(R_S)=31.373$  nA,  $I(R_L)=64.105$  uA, Ratio  $I(R_L)/I(R_S)=2,043.3$ ,  $\theta^\circ=-174.541$  and THD=0.9%.

- Case–A2: The NPN driver transistor is user defined model QN ( $\beta=50$ ) and PNP follower transistor is default model Q2N2907A ( $\beta=231.7$ ) along with  $R_S=1$   $\Omega$ ,  $R_I=50$  M $\Omega$ ,  $R_2=50$  K $\Omega$ ,  $R_E=12$  K $\Omega$ ,  $R_L=10$  K $\Omega$ ,  $C_1=1$   $\mu$ F,  $C_L=10$   $\mu$ F,  $V_{CC}=+25$  V and AC input signal source= 1 V, 1 KHz, and obtained performance parameters are  $A_{IGA} = 1,971.5$ ,  $A_{IGA-RMS} = 1,971.5$ ,  $A_{VGA} = 0.996$ ,  $A_{VGA-RMS} = 0.996$ ,  $F_H = 592.787$  Hz,  $A_{IGD} = 10,443$ ,  $A_{IGD-RMS} = 10,443$ ,  $A_{VGD} = 17.049$ ,  $A_{VGD-RMS} = 17.049$ ,  $P_G$  (in Watt) = 1,963.6,  $P_G$  (in dB-Watt) = 32.9305,  $V_I=0.9991$  mV,  $V_6 = 9.723$  V, Ratio  $V_6/V_I=9,731.7$ ,  $I(R_S) = 3.1231$  nA,  $I(R_L) = 972.330$  uA, Ratio  $I(R_L)/I(R_S)=3,11,334.8$   $\theta^\circ = -65.369$  and THD = 1.94%.
- Case–B2: The NPN driver transistor is default model of Q2N2222 ( $\beta=255.9$ ) and PNP follower transistor is user defined model of QP ( $\beta=50$ ) with  $R_S=1$   $\Omega$ ,  $R_I=50$  M $\Omega$ ,  $R_2=50$  K $\Omega$ ,  $R_E=15$  K $\Omega$ ,  $R_L=10$  K $\Omega$ ,  $C_1=0.1$   $\mu$ F,  $C_L=10$   $\mu$ F,  $V_{CC}=+25$  V and AC input signal source=1 V, 1 KHz, and the obtained performance parameters are  $A_{IGA}=1,557.9$ ,  $A_{IGA-RMS}=1,557.9$ ,  $A_{VGA}=0.975$ ,  $A_{VGA-RMS}=0.975$ ,  $F_H=423.013$  Hz,  $A_{IGD}=4,686.5$ ,  $A_{IGD-RMS}=4,684.5$ ,  $A_{VGD}=392.400$ ,  $A_{VGD-RMS}=382.537$ ,  $P_G$  (in Watt)=1,518.9,  $P_G$  (in dB-Watt)=31.815,  $V_I=0.9991$  mV,  $V_6=7.7842$  V, Ratio  $V_6/V_I=7,791.2$ ,  $I(R_S)=10.346$  nA,  $I(R_L)=778.415$  uA, Ratio  $I(R_L)/I(R_S)=75,238.2$ ,  $\theta^\circ=-67.957$ , and THD=1.81%.

Table 3. Comparative table of performance parameters

Performance Parameters	Circuit-1	Circuit-2
Amplifier Current Gain, $A_{IGA}$	1,746.5	1,202.8
AC Current Gain of Amplifier, $A_{IGA-RMS}$	1,745.0	1,202.8
AC Voltage Gain of Amplifier, $A_{VGA-RMS}$	48.410	0.957
Amplifier Voltage Gain, $A_{VGA}$	48.453	0.958
Lower Cut-off frequency, $F_L$	107.166 Hz	Unavailable
Higher Cut-off Frequency, $F_H$	3.1977 MHz	383.728 Hz
Bandwidth, $B_W$	3.1976 MHz	Unavailable
Device Current Gain, $A_{IGD}$	62,096	2,499.9
AC Current gain of the device, $A_{IGD-RMS}$	62,096	2,499.9
Device Voltage Gain, $A_{VGD}$	48.455	439.783
AC Voltage Gain of the device, $A_{VGD-RMS}$	48.413	439.480
Power Gain in Watt	84,623.16	1,152.28
Power Gain in dB-Watt	49.274	30.61
Input Current, $I_{R_S}$	34.548 nA	8.5221 nA
Output Current, $I_{R_L}$	62.873 uA	598.974 uA
Ratio, $I_{R_L}/I_{R_S}$	1819.8	70,284.78
Input Voltage, $V_I$	0.9991 mV	0.9991 mV
Output Voltage, $V_7$	50.299 mV	13.315 V
Ratio, $V_7/V_I$	50.3443	13,326
Phase Difference, $\theta^\circ$	-173.901	-68.964
Total Harmonic Distortion (THD)	0.9%	1.86%

Figures 2 (a) and (b) show frequency responses of both the topologies under four cases discussed above. Case-A1 gives amplification in the frequency range 106.249 Hz to 183.889 KHz with bandwidth 183.783 KHz and Case-B1 in frequency range 106.278 Hz to 80.911 KHz with bandwidth 80.805 KHz respectively. Amplifiers under Case-A2 and Case-B2 produces higher cut-off frequency 592.787 Hz and 423.013 Hz respectively; hence useful in ultra-low frequency range (ULF-range) applications [18].

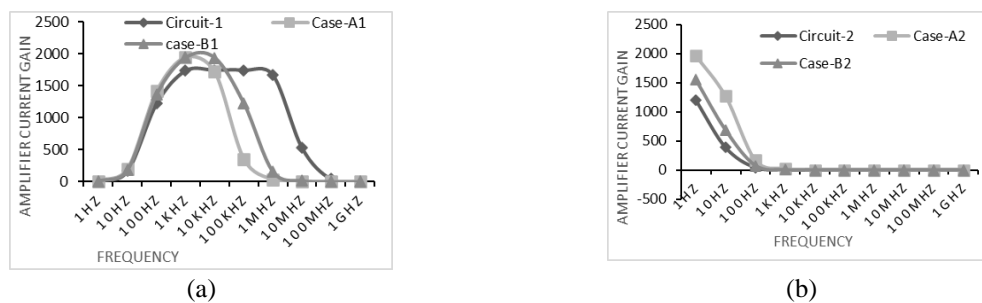


Figure 2. Frequency response curve (a) circuit-1 and (b) circuit-2

### 3.2. Effect of additional biasing resistance $R_A$ on circuit-1

Performance parameters of circuit-1 amplifier are greatly affected by additional biasing resistance  $R_A$ , whose value is 200 K in Case-A1 and 100 K in Case-B1. In addition to  $R_A$  the value of  $R_1$  is decreased to 90 K from 95 K in Case-A1 and 85 K from 90 K in Case-B1, to maintain bias point at node 3, keeping other circuital parameters unaltered. Table 4 lists the performance parameters of these amplifiers under effect of  $R_A$ . Increment in the base-collector voltage of follower transistor in Sziklai pair combination, from 0.3 V-1.22 V, results in significant improvement of the performance parameters of both the amplifiers with increased THD (2.06%).

Table 4. Effect of additional biasing resistor  $R_A$  on performance parameters of amplifier

Performance Parameters	Circuit-1	Case-A1	Case-B1
Amplifier Current Gain, $A_{IGA}$	8,177.8	8,800.7	9,205.7
AC Current Gain of Amplifier, $A_{IGA-RMS}$	8,166.6	8,233.0	9,131.8
AC Voltage Gain of Amplifier, $A_{VGA-RMS}$	303.117	194.040	350.205
Amplifier Voltage Gain, $A_{VGA}$	303.701	197.078	356.401
Lower Cut-off frequency, $F_L$	678.321 Hz	856.118 Hz	922.633 Hz
Higher Cut-off Frequency, $F_H$	6.1001 MHz	286.790 KHz	247.288 KHz
Bandwidth, $B_w$	6.0094 MHz	285.934 KHz	246.366 KHz
Device Current Gain, $A_{IGD}$	32,160	19,446	22,468
AC Current gain of the device, $A_{IGD-RMS}$	32,160	19,398	22,467
Device Voltage Gain, $A_{VGD}$	303.715	197.124	356.422
AC Voltage Gain of the device, $A_{VGD-RMS}$	303.132	194.096	350.232
Power Gain in Watt	24,83,606.03	17,34,424.3	32,80,920.6
Power Gain in dB-Watt	63.950	62.391	65.159
Input Current, $I_{R_s}$	42.770 nA	46.365 nA	46.265 nA
Output Current, $I_{R_L}$	321.231 uA	382.083 uA	384.024 uA
$I_{R_L}/I_{R_s}$	7,510.66	8,240.7	8,300.5
Input Voltage, $V_1$	0.9991 mV	0.9991 mV	0.9991 mV
Output Voltage, $V_7$	257.082 mV	153.056 mV	268.125 mV
$V_7/V_1$	257.313	153.193	268.336
Phase Difference, $\theta^0$	-146.093	-140.126	-138.275
Total Harmonic Distortion, THD	2.06%	2.15%	2.28%

### 3.3. Effect of biasing resistors $R_1$ and $R_2$ on circuit-2

Effect of biasing resistors  $R_1$  and  $R_2$  on the performance of circuit-2 has also been figured out. It has been found that biasing resistors  $R_1$  and  $R_2$  has significant impact on the performance parameters of the circuit-2. Optimum performance of circuit-2 is reported when their values are high (Mega ohm). However, biasing resistors at  $R_1=25 \text{ M}\Omega$  and  $R_2=50 \text{ M}\Omega$  gives very high THD (46.78%) however the device voltage gain  $A_{VGD}$  gets distorted giving lesser power gain [19].

### 3.4. Range of operation of AC input signal

For all the amplifier circuits configurations the observation reference is made at 1 mV, 1 KHz AC input signal for distortion-less amplification. Amplifier circuit-1 produces distortion less output for 0.1  $\mu\text{V}$  (THD=0.89%) to 6 mV (THD=5.60%) range of AC input signal at 1 KHz frequency. Similarly, Case-A1 gives distortion-less output for 1  $\mu\text{V}$  (THD=0.88%) to 11 mV (THD=5.85%) and Case-B1 gives fair response for 1  $\mu\text{V}$  (THD=0.87%) to 10 mV (THD=5.64%). Similarly, amplifier circuit-2 is capable of amplifying AC input signal ranging between 100  $\mu\text{V}$  (THD=1.63%) to 11 mV (THD=5.56%) whereas Case-A2 and Case-B2 produce undistorted output waveform for the input signal ranging between 100  $\mu\text{V}$  (THD=1.19%) to 11 mV (THD=5.43%) and 100  $\mu\text{V}$  (THD=1.50%) to 18 mV (THD=5.42%) respectively.

THD of all the amplifiers fluctuate with the range of AC input signal whereas all the other performance parameters remain mostly unaltered. Lowest value of THD for the amplifier under Common-Emitter and Common-Collector configuration is received at the range (0-1  $\mu\text{V}$ , 1 KHz) and (0-1 mV, 1 KHz) respectively. It has also been found that Fourier analysis is aborted at the range (0-10 V, 1 KHz) of the amplifier circuit-1 and (0-100 V, 100 KHz) range of Case-A1 and circuit-2.

### 3.5. Effect of capacitors

The distortion of the waveform in the output signal is found to be a very serious problem in BJT based common-emitter and common-collector amplifiers at higher frequencies [20]. It has been observed that bypass capacitor  $C_E$  and load capacitor  $C_L$  play a very significant role in minimizing this problem. Variation of total harmonic distortion (THD) with respect to bypass capacitor  $C_E$  for circuit-1, Case-A1 and Case-B1 and load capacitor  $C_L$  for circuit-2, Case-A2 and Case-B2 has been observed. It has been found that THD of circuit-1 increases to  $C_E=100 \text{ nF}$ . From  $C_E=100 \text{ nF}$  to  $C_E=10 \text{ uF}$ , THD fluctuates and tends to saturation at higher values of  $C_E$  (e.g.,  $C_E \geq 100 \text{ uF}$ ). Similarly, for case-A1 and case-B1, THD peaks at 100 nF and

decreases beyond this value. Similarly, THD of circuit-2 remain almost constant up to  $C_L=100$  nF. It must be noted that  $C_L$  is an essential component for the Circuit-2. When it is detached from circuit-2, amplifier current gain increases to 1,559.8 and total harmonic distortion decreases to 0.7% (worth noting that the combination device current gain  $A_{IGD}$  remains unaltered).

### 3.6. Tuning performance of circuit-1

Tuning performance of the amplifier is studied by varying emitter bypass capacitor  $C_E$  under no load condition ( $C_L$  removed) and under varying load ( $C_L$ ) keeping emitter bypass capacitor  $C_E$  fixed at 100  $\mu$ F under constant biasing condition [21]. Tuning with  $C_E$  and  $C_L$  is received for the variation between 10 nF-100 mF and 1 fF-10 nF. Amplifier voltage gain and amplifier current gain remains almost constant for any variation in  $C_E$  whereas  $F_L$  decreases from KHz to Hz range and  $F_H$  remains unchanged on increasing  $C_E$ . Similarly, tuning performance with  $C_L$  is obtained for the variation between 1 fF to 10 nF. Increment in  $C_L$  causes  $F_H$  to shrink from MHz to KHz range whereas voltage gain and current gain remains unchanged.

Tuned frequency response of the circuit-1 has been drawn in Figure 3 under two different combination of tuning capacitor, first with  $C_E=100$   $\mu$ F and  $C_L=10$  pF and second with  $C_E=50$   $\mu$ F and  $C_L=1$  pF which is referring to the fact that proposed amplifier can be used to obtained desired frequency of a specific channel by the proper adjustment of  $C_E$  and  $C_L$ .

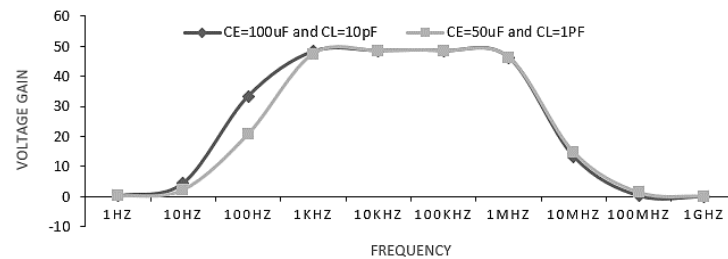


Figure 3. Tuned frequency response of circuit-1

### 3.7. Range for biasing components of circuit-1

It has been found that variation in base resistance  $R_S$  does not affect amplifier current gain  $A_{IGA}$  whereas amplifier voltage gain  $A_{VGA}$  decreases with increasing  $R_S$ . Minimum value of amplifier voltage gain  $A_{VGA}$  is received at  $R_S=1.3$  M $\Omega$  ( $A_{VG-MIN}=1.0507$ ) and maximum value at  $R_S=1$   $\Omega$  ( $A_{VG-MAX}=48.453$ ) with meaningful amplification in  $1 \Omega \leq R_S \leq 1.3$  M $\Omega$  range. Similarly,  $A_{IGA}$  and  $A_{VGA}$  both decreases with rising value of collector resistance  $R_C$  up to a critical limit 9 K $\Omega$  but beyond this critical limit, response curve of both  $A_{IGA}$  and  $A_{VGA}$  distorted badly. Maximum value of  $A_{VGA}$  is received at  $R_C=9$  K $\Omega$  ( $A_{VGA-MAX}=48.453$ ) and minimum value at  $R_C=16$   $\Omega$  ( $A_{VGA-MIN}=1.0348$ ) with faithful amplification range  $16 \Omega \leq R_C \leq 9$  K $\Omega$  whereas Maximum value of  $A_{IGA}$  is received at  $R_C=9$  K $\Omega$  ( $A_{IGA-MAX}=1,746.5$ ) and minimum value at  $R_C=1\Omega$  ( $A_{IGA-MIN}=2.3753$ ) with purposeful amplification range  $1 \Omega \leq R_C \leq 9$  K $\Omega$ . It is worth noting that the proposed amplifier switches-ON at 2 V DC supply voltage. Amplifier voltage gain  $A_{VGA}$  gives distortion-less responses in 2 V-35 V range of  $V_{CC}$  whereas amplifier current gain  $A_{IGA}$  gives distortion-less responses in 2-60 V range of  $V_{CC}$ . Both  $A_{IGA}$  and  $A_{VGA}$  rises gradually up to 30 V and falls linearly beyond this value. It is also to be noted that increment in load resistance  $R_L$  causes corresponding increase in  $A_{VGA}$  and simultaneous decrease in  $A_{IGA}$ . Therefore, Minimum value of  $A_{VGA}$  is achieved at  $R_L=16$   $\Omega$  ( $A_{VGA-MIN}=1.0535$ ) but beyond this value it gradually rises and becomes saturated at  $R_L=7$  M $\Omega$  ( $A_{VGA}= 591.068$ ) whereas maximum value of  $A_{IGA}$  is received at  $R_L=1$   $\Omega$  ( $A_{IGA-MAX}=1902.3$ ) and minimum value at  $R_L=17$  M $\Omega$  ( $A_{IGA-MIN}=1.0013$ ) with purposeful amplification range  $1 \Omega \leq R_C \leq 17$   $\Omega$ .

### 3.8. Effect of $\beta$ variation on overall performance of proposed amplifier

Modelling of  $\beta$  is important for small-signal amplifiers based hence observations are recorded for range of 'ideal maximum forward beta'  $\beta$  in the modelled BJTs [22]. Although the theoretical gain of such combination is the product of current gains of constituent BJTs but practical gain is always lower due to secondary effects. The overall device gain of such pair also depends on the arrangement of stage gain as leakage and bypass currents also get amplified at later stage. This section covers detailed simulation analysis of impact of stage gain and their order on overall device gain along with frequency response.

### 3.8.1. Effect of $\beta$ variation on the circuit-1

Performance parameters of circuit-1 at identical values of: i)  $\beta$ , ii) fixed  $\beta_1$  and varying  $\beta_2$ , and iii) fixed  $\beta_2$  and varying  $\beta_1$  has been studied. It has been observed that at identical values of  $\beta$ ,  $A_{IGA}$ ,  $A_{VGA}$ ,  $A_{VGD}$  and  $A_{IGD}$  increases and bandwidth decreases with increasing  $\beta_1$  and  $\beta_2$ , however THD remains constant at 0.9%. Variation of  $A_{IGA}$  and  $A_{IGD}$  with frequency at identical  $\beta$  values is illustrated in Figures 4 (a) and 4 (b). It has been observed that amplifier current gain remains constant at mid frequency ranges extended from 1KHz to 1 MHz and decreases at higher ( $\leq 1 \text{ MHz}$ ) and lower frequency ranges ( $\leq 1 \text{ KHz}$ ) whereas device current gain remains constant at 1 Hz to 100 KHz frequency range and decreases at higher frequency ranges ( $\leq 100 \text{ KHz}$ ). As a usual feature of small-signal amplifier, performance parameters of the proposed amplifier increase with rising values of like and unlike  $\beta_1$  and  $\beta_2$  which authenticate the proposed amplifier.

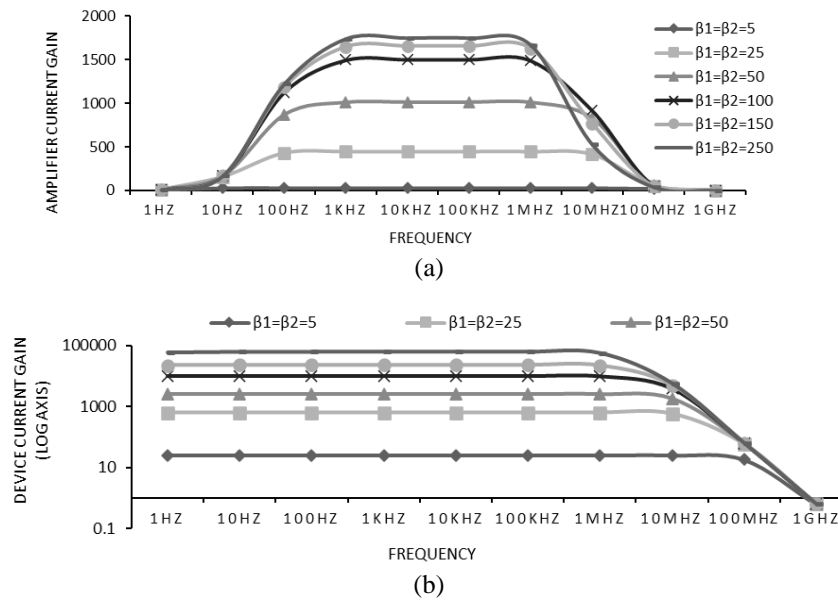


Figure 4. Variation of current gains of circuit-1 at identical values of  $\beta_1$  and  $\beta_2$  for (a) amplifier current gain and (b) device current gain

When  $\beta_2$  is fixed at 250 and  $\beta_1$  is varied up to 250,  $A_{IGA}$ ,  $A_{VGA}$ , device voltage gain  $A_{VGD}$  and  $A_{IGD}$  increases whereas THD remains constant at 0.9%. However, bandwidth undergoes sharp decrement at  $\beta_1=100$   $\beta_2=250$ . As per % variation of  $A_{IGD}$  reported, ideal response of the amplifier is achieved at  $\beta_1=5$  and  $\beta_2=250$ . Similarly, when  $\beta_1$  is fixed at 250 and  $\beta_2$  is varied up to 250, increment in  $A_{IGA}$ ,  $A_{VGA}$ ,  $A_{VGD}$ ,  $A_{IGD}$  and bandwidth is observed whereas THD remains constant at 0.9%. Ideal behavior of the proposed amplifier under this condition is achieved at  $\beta_1=250$ ,  $\beta_2=5$  and  $\beta_1=250$ ,  $\beta_2=25$ . The proposed amplifier shows idealistic behavior at lower values of both  $\beta_1$  and  $\beta_2$ . Increasing the range of  $\beta_1$  and  $\beta_2$  causes corresponding decrease in bandwidth [23].

### 3.8.2. Effect of $\beta$ variation on the circuit-2

Performance parameters of the circuit-2 with different values of  $\beta$  has also been observed. Circuit-2 works well up to  $\beta_1=\beta_2=50$  with high  $A_{IGA}$  (1,202.8) and low THD (1.87%) but beyond this value, this amplifier suffers from Higher THD, consequently could not retain the status of matched Sziklai pair small-signal amplifier. Moreover, maximum amplifier current gain  $A_{IGA-MAX}$  is obtained at  $\beta_1=\beta_2=75$  but due to high level of distortion, this condition could not be taken under consideration for matched pair of BJTs for the proposed amplifier. The optimum performances with matched pair of BJTs is obtained at values of  $\beta_1$  and  $\beta_2$  below 50.

When  $\beta_1$  is fixed at 50 and  $\beta_2$  is varied up to 100, all the performance parameters increase with increasing range of  $\beta$  except THD which becomes higher at lower value of  $\beta_2$  and lower at higher value of  $\beta_2$  keeping  $\beta_1$  fixed at 50. This also refers that proposed amplifier gives acceptable performance with unmatched pair of BJTs. Ideal behavior of the proposed amplifier under this condition is obtained with unmatched pair of BJTs under the condition  $\beta_1=50$   $\beta_2=2$ ,  $\beta_1=50$   $\beta_2=20$  and  $\beta_1=50$   $\beta_2=30$ . Similarly, when,  $\beta_2$  is fixed at 50 and  $\beta_1$  is varied up to 100, all the performance parameters increase with increasing range of  $\beta$

except THD. High value of THD is obtained at lower value of  $\beta_2$  and vice-versa. Optimum performance under this condition is obtained when  $\beta_1 < \beta_2$ .

Variation of  $A_{IGA}$  and  $A_{IGD}$  with frequency at equal values of  $\beta$  is shown in Figures 5 (a) and 5(b). Proposed amplifier gives 'Maximum Amplifier current gain'  $A_{IGA-MAX}$  at  $\beta_1=\beta_2=50$  and 'Minimum Amplifier current gain'  $A_{IGA-MIN}$  at  $\beta_1=\beta_2=100$ . Similarly, 'Maximum Device current gain'  $A_{IGD-MAX}$  is obtained at  $\beta_1=\beta_2=50$  and 'Minimum Device current gain'  $A_{IGD-MIN}$  is obtained at  $\beta_1=\beta_2=100$ . The overall result show that  $\beta_1$  and  $\beta_2$  are not to be kept above 50 for the circuit-2 to act as matched Sziklai pair small-signal amplifier. Also, the amplifier in discussion provides ideal behavior for both the  $\beta$  below 50.

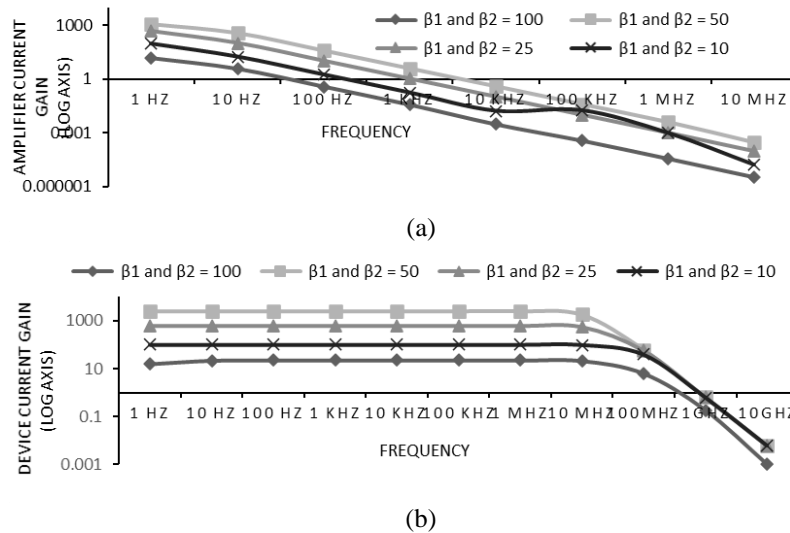


Figure 5. Variation of current gains of circuit-2 at identical values of  $\beta_1$  and  $\beta_2$  for (a) amplifier current gain and (b) device current gain

### 3.9. Temperature variation

Temperature dependency of the circuit-1 and circuit-2 has also been studied [24]. It has been found that all the performance parameters of the circuit-1 decrease with rise in temperature except bandwidth which increases up to  $-10^\circ\text{C}$  undergoes sudden decrement at  $0^\circ\text{C}$  which further attain rising trend at higher temperatures. This happens due to the fact that base-collector voltage of second BJT decreases with increasing temperature which causes decrement in collector current which in turns reduces current gain and voltage gain.

Similarly, in circuit-2, no significant impact of temperature is reported on device current gain  $A_{IGD}$  and  $A_{VGA}$ . However,  $A_{IGA}$ ,  $A_{VGD}$  decreases and THD increases initially and thereafter decreases beyond. This shows that proposed amplifier is thermally stable over the wide range of temperature  $-30^\circ\text{C} \leq T \leq 50^\circ\text{C}$ . Possible reason for such behavior is that when temperature is increased within the range  $-30^\circ\text{C} \leq T \leq 50^\circ\text{C}$ , base-collector voltage of second transistor  $V_{BC}$  drops from 6.96-6.87 V which causes reduction in collector voltage  $V_C$  which results in the lowering of  $A_{IGA}$  &  $A_{VGD}$ .

### 3.10. Noise sensitivity

Noise analysis of the circuit-1 at 100 Hz, 1 KHz, 10 KHz, 1 MHz and 100 MHz frequencies and circuit-2 at 10 Hz, 100 Hz, 1 KHz, 100 KHz and 1 MHz frequencies with respect to temperature has also been observed [25]. It has been found that input noise of the circuit-1 increases with rise in temperature whereas output noise increases with temperature elevation at 100 Hz and 100 MHz frequencies. But, at 1 KHz, 10 KHz and 1 MHz operating frequencies, it increases up to room temperature ( $27^\circ\text{C}$ ) but decreases beyond this value. It has also been observed that input noise remains constant up to 10MHz frequency and thereafter increases exponentially whereas output noise remains constant over the frequency range 1 KHz to 100 KHz and decreases at higher ( $\leq 100\text{ KHz}$ ) and lower frequency ( $\leq 1\text{ KHz}$ ).

Similarly, both input and output noise of circuit-2 increase with rise in temperature which demonstrates the usual feature of small-signal amplifier. It is noteworthy that at 10 Hz, 100 Hz and 1 KHz frequency, range of both input and output noises are equal to each other (range  $10^{-9}\text{ V/Hz}$ ) whereas range of



input noise ( $10^{-9}$  V/Hz) become greater than range of output noise ( $10^{-12}$  V/Hz) at 100 KHz and 1 MHz frequency ranges [26].

### 3.11. Phase variation

The phase-frequency response allows us to see exactly how the output gain and phase changes at a particular point over range of different frequencies [27]. Simulated responses of Phase-frequency variation of output current to input current for proposed amplifiers has been observed. It has been found that under the Sziklai CE-configuration, phase variation of circuit-1 and Case-A1 decreases with frequency elevation whereas in Case-B1, phase variation decreases up to 10 MHz frequency and increases beyond this value. Similarly, under Sziklai CC-configuration, phase variation of Case-A2 and Case-B2 decreases up to 1 MHz frequency and increases beyond this limit whereas in Circuit-2, it decreases with simultaneous rise in frequency [28].

### 3.12. Small-signal AC analysis

#### 3.12.1. Mathematical analysis of circuit-1

For the amplifier circuit-1  $\beta_1=250$ ,  $\beta_2=250$ ,  $r_{\pi 1}=0.951$  M $\Omega$ ,  $r_{\pi 2}=3.80$  K $\Omega$ ,  $r_{o1}=0.772$  G $\Omega$  and  $r_{o2}=1$  T $\Omega$ . Since  $r_{o1}$  and  $r_{o2}$  of the amplifier circuit-1 is high and therefore can be ignored during small-signal AC equivalent analysis [29], [30]. Hence the small-signal AC equivalent circuit will take the form as sketched in Figure 6.

Analysis of the equivalent circuit of Figure 6 provides the expression for the AC voltage gain of the proposed amplifier as,

$$A_V = \frac{R_o \left[ \left( 1 + \frac{r_{\pi 2}}{R_A} \right) + \beta_1 (1 - \beta_2) \right]}{r_{\pi 1} [(R_A + r_{\pi 2}) - (1 - \beta_2) R_o]}$$

and the expression for the AC Current gain can be obtained as equal to,

$$A_I = \frac{i_o}{i_{b1}} = \frac{\left[ 1 + \frac{\beta_1 (1 - \beta_2)}{\left( 1 + \frac{r_{\pi 2}}{R_A} \right)} \right]}{\left[ 1 - \frac{(1 - \beta_2) R_o}{R_A \left( 1 + \frac{r_{\pi 2}}{R_A} \right)} \right]}$$

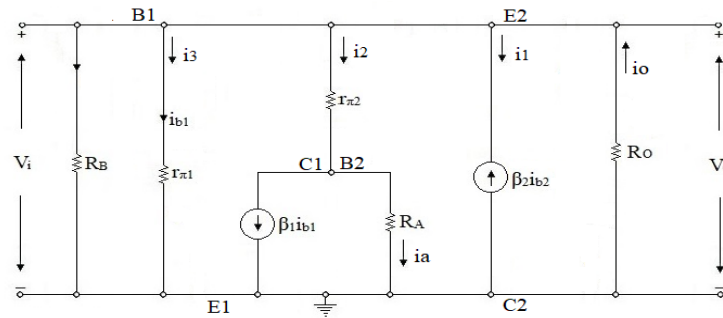


Figure 6. Small signal AC equivalent circuit of circuit-1

#### 3.12.2. Mathematical analysis of circuit-2

For present case  $\beta_1=50$  and  $\beta_2=100$ ,  $r_{\pi 1}=1.10 \times 10^5$ ,  $r_{\pi 2}=2.20 \times 10^3$ ,  $r_{o1}=1.00 \times 10^{12}$ ,  $r_{o2}=1.00 \times 10^{12}$ . Higher  $r_{o1}$  and  $r_{o2}$ , may be treated as open circuit, hence the small signal AC equivalent circuit of the circuit-2 amplifier will be as shown in Figure 7. Analysis of the equivalent circuit of Figure 7 provides the expression for the AC voltage gain of the proposed amplifier as,

$$A_V = \frac{V_o}{V_i} = \frac{-i_{b1} R_L [\beta_1 \beta_2 + (1 + \beta_1)]}{i_{b1} [r_{\pi 1} - \beta_1 \{r_{\pi 2} - R_E (1 + \beta_2)\}]}$$

and the expression for the AC Current gain can be obtained as equal to:

$$A_I = -[1 + \beta_1 + \beta_1\beta_2]$$

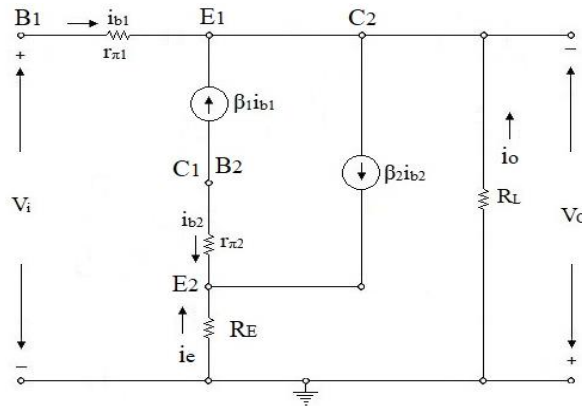


Figure 7. Small signal AC equivalent circuit of Circuit-2

#### 4. CONCLUSION

Sziklai compound pair are often used in output stages and also in areas requiring very high current gain with smaller drive voltage. Present paper covers a detailed analysis of Sziklai Pair as device with varying component characteristics along with NPN Sziklai pair small-signal amplifier under CE and CC mode using matched pair of BJTs. Proposed amplifiers removes the narrow-bandwidth problem of PNP driven Sziklai pair small-signal amplifier and poor response problem of Darlington pair small-signal amplifiers at higher frequencies. It has also been found that at 1 KHz of operating frequency, circuit-1 shows better noise performance than that of circuit-2. Moreover, phase difference of output-to-input current in circuit-1 is lower in comparison to circuit-2. Proposed amplifiers are capable of amplifying 0.1  $\mu$ V-6 mV and 100 $\mu$ V-11mV range of AC input signal at 1KHz frequency respectively.

The circuit-1 performance parameters are improved in the presence of additional biasing resistance  $R_A$  with elevated THD, however it limits faithful current amplification in the range 2-60 V of DC supply voltage at room temperature along with excellent thermal stability over the operational temperature range  $-30^\circ\text{C} \leq T \leq 50^\circ\text{C}$ . At lower values of  $\beta$  ( $\beta \leq 50$ ), this amplifier is also found to exhibit ideal behavior with narrow bandwidth. Similarly, Circuit-2 amplifier produces higher current gain with strong dependency on  $R_1$  and  $R_2$ . It has been found that this amplifier works well as the matched pair of BJTs up to  $\beta_1 = \beta_2 = 50$  but beyond this value, this amplifier suffers from higher THD, consequently could not retain the status of matched Sziklai pair small-signal amplifier. This amplifier gives considerable responses at  $R \geq 9 \text{ K}\Omega$  and  $R_P \leq 20 \text{ K}\Omega$  and the high margin between the output-to-input current and output-to-input voltage in transient and AC analysis in circuit-2 can be justified as it is a Sziklai pair small-signal amplifier under common-collector configuration.





Present study covers a broad-spectrum of analysis of proposed two amplifiers configurations including effect of biasing resistance  $R_A$ , variation of 'ideal forward maximum beta'  $\beta$ , temperature dependency, noise sensitivity and phase variation. First amplifier configuration circuit-1 operates on very low input voltage range (0.1 $\mu$ V-6 mV) and gives high current gain (1,746.5), high amplifier voltage gain (48.453), wider bandwidth (3.1976 MHz) and low THD (0.9%). The second amplifier configuration circuit-2 works on input voltage range of 100  $\mu$ V-11 mV and gives undistorted output with high current gain (1,202.8), nearly unity voltage gain (0.958) for signals below 383.728 Hz.

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**BIOGRAPHIES OF AUTHORS**

**Sachchida Nand Shukla**     born on January 20, 1967, is presently serving as Professor, Department of Physics & Electronics at Dr. Ram Manohar Lohia Avadh University, Ayodhya, UP, India. He did his Masters in Physics (Electronics) in 1988 and Ph.D. in 1992 from the same university. Dr. SachchidaNand Shukla holds 28 years' experience of teaching He has published 95 research papers in peer-reviewed/ indexed journals of International/National repute & conference proceedings and 06 books. In his supervision 14 research scholars have been awarded Ph.D. degree. He can be contacted at email: [sachida.shukla@gmail.com](mailto:sachida.shukla@gmail.com).



**Syed Shamroz Arshad**     received his B.Sc. and M.Sc. degree in Physics from Lal Bahadur Shastri P.G. College Gonda in the year 2015 and 2017 respectively. Currently, he is pursuing Ph.D. in Physics (Electronics) from the department of Physics & Electronics, Dr. Ram Manohar Lohia Avadh University, Ayodhya. During past two years, he has published 1 paper in international journal, 1 paper in the international book-chapter and 2 papers in conferences. He can be contacted at email: [shamroz.inspire@gmail.com](mailto:shamroz.inspire@gmail.com).



**Geetika Srivastava**     received the B.Sc. and M.Sc. degree in Electronics from DDU Gorakhpur University, India. She obtained her Ph.D.in Electronics from Dr. RML Avadh University, India. She is currently working as Associate Professor with the Department of Physics and Electronics Dr. RML Avadh University, India. She has published more than 30 papers in international journals and successfully running two funded research projects and one consultancy project on VLSI signal processing. She has got one International Multilateral Research Grant from SERB, DST, Government of India. She won best Project award from UNESCO Category 1 Institution ICTP, Italy and IAEA, Vienna, Austria. She has successfully guided three doctoral thesis and currently guiding six research scholars. She has also supervised 20 PG dissertations. Her research interests include biomedical signal processing, VLSI, machine learning and deep learning. She can be contacted at email: [gsrivastava@rmlau.ac.in](mailto:gsrivastava@rmlau.ac.in).