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Design and implementation of reduced number of switches for new multilevel inverter topology without zero-level state

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ABSTRACT

Currently, multilevel inverter (MLI) has been chosen over conventional inverter because of less harmonic distortions and higher output voltage levels. In this paper, 15-level inverter with reduced number of power switching devices is designed. Different output voltage levels can be obtained including zero-level or with none zero-level (NoneZero-level). Single-phase MLI inverter with 7-switches is built, simulated, and implemented practically. The system depending on modified absolute sinusoidal pulse width modulation (MASPWM) controller strategy is adopted. Simulation results clarified that MLI with NoneZero-level provides output voltage with total harmonic distortion (THD) percent less than with zero-level. The THD of the 15-level output voltage with zero-level is 3.39%, while with NoneZero-level is 3%, respectively. The system is tested at different output levels. The THD values at different output voltage levels is reduced by 12% depending on NoneZero-level state. Depending on what has been achieved, the system has been implemented practically with NoneZero-level and the THD value was 3.1%. These results prove the success of the suggested MLI circuit and MASPWM controller to obtain the required voltage level and THD.

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1. INTRODUCTION

Power electronics devices commonly utilize power from renewable energy systems like photovoltaic, biofuel and many other sources. Renewable energy source (RES) generates direct current (DC) power, which is converted to alternating current (AC) power by inverters. The output from inverters is staircase waveforms that contain many harmonics. The difference between conventional inverter and multilevel inverter (MLI) that the MLI have a number of advantages such as less output harmonics shape and higher output voltages. So that, many scientists are working to design best circuits of MLI and controller techniques to get low cost, small size, and high efficiency. Thus, MLI is suitable in medium/high power industrial applications than conventional types [1]. The cascaded H-bridge inverter is a recent MLI type that produces a higher number of output voltage levels with fewer switches. It is easy to build and control. The problem of the cascaded MLI is needing single-separated DC voltage source, which may be not balanced at all phases of inverter [2]. The Cascaded MLI is good for renewable energy applications such as PV energy system as a separate-DC-sources [3]. The cascaded MLI is formed by series connection of several single cell H-bridge inverters with separate DC sources. Each inverter cell is set to produce three output voltage (+Vdc, 0, and −Vdc) [4]. Improving the MLI output voltage levels enhance system quality, reduce distortion, and make it is suitable for HV applications [5]. Multilevel inverter contains cascaded single-phase inverters with

sequence DC sources. These DC sources with different values are the output of different forms of renewable energy sources. The challenging to get efficient DC-AC converter is to reduce number of power electronics switches. Reduced the number of switches will minimize the power loss in the system. In 2016 [6], a symmetrical MLI topology that consumes lesser component account was developed to get output voltage total harmonic distortion (THD) of 8.65%.

In the same year [7], a new type of cascaded MLI that produces a different output level with a reasonable number of components was proposed. In 2017 [8] a single-phase inverter with eight switches and three DC sources was described with THD of 1.77%. The performance of the system as well as its cost relies on the number of the employed power switches. In the same year [9], four voltage sources, seven power switches, three additional diodes and seven driver circuit were used in order to implement nine-level switches including the zero-level with output voltage and current THD of 5% and 1.03%, respectively. In 2018 [10], a multilevel three-H-bridge inverter with DC inputs of (Vdc, 3Vdc, 9Vdc) was built to get 27-level voltage output depending on a modified absolute sinusoidal pulse width modulation (MASPWM) strategy. The output current and voltage distortion values for three-phase circuit were 0.0857% and 0.67%, while the THD values of the single-phase were 0.238% and 1.165%, respectively.

In 2019 [11] a low voltage rated switches that leads to noticeable reduction in total standing voltage was utilized. In this manner, the switching losses and the cost are significantly reduced. They used 11 switches in their work. In 2018 [12] the switching losses was decreased by using a small duty cycle while it comprises high-speed DC-DC converter with switched capacitive converter. In 2019 [13] seven switch transistors with reduced number of diodes for model predictive control was proposed and produced THD of 1.23%. While in same year [14], a MLI with and with absence of zero-level states was proposed. The THD value of the 9-level output was 9.5% with zero-level and 12.5% with absence zero-level. In 2020 [15], the same power and control circuits suggested by [10] built with sensor less speed/torque control of an induction motor at different operation conditions. The suggested circuit provided good response and quality. In the same year [16], a 15-level inverter with ten-switches and zero-level state was built and modelled. The voltage value was 312V. In 2021 [17], asymmetrical 21-level MLI for PV energy with reduced number of switches with the zero-level-state was introduced with distortion of 3.49%.

Also, in 2021 [18], a hybrid cascaded H-bridge MLI was discussed with eight power switches to produce seventeen level including the zero level with THD of 3%. Moreover in 2021 [19], a four input DC sources and nine semiconductor switches was suggested to reduce the voltage stress and the number of power switches where the THD was 3.2%. Additionally in 2021 [20], a circuit to reduce the number of isolated DC-sources without reducing output levels was developed. The circuit utilizes six two-quadrant switches, three four-quadrant switches and four capacitors. Furthermore in 2021 [21], a detailed survey on MLI such as symmetric, asymmetric, hybrid and modularized were introduced in order to generate 81-level. Besides reducing number of switches, reducing the number of harmonics at the output of inverters are of great importance [22]-[24].

There are two types of MLI which are symmetrical and asymmetrical categories. The symmetrical one is built with equal dc-source and switches in each cell, while the asymmetrical type is designed with reduced number of switches and unequal dc-source at each unit cell [25]. In this work, the implementation of new topology of MLI with advanced controller and with zero-level and none zero-level states is proposed. A practical set for the MLI with Arduino microcontroller set is implemented and the results are validated by MATLAB software environment. The objective of this study is to explain that the system without zero-level state gives better-quality than with zero-state. This objective has been verified by simulation and practical results.

2. MULTILEVEL INVERTER TOPOLOGY

The suggested topology of multilevel inverter shown in Figure 1 has been considered to produce 15-level output voltage. This topology uses 7-switches, 3-diodes and three input DC voltage sources with values of (V_{dc}, $2V_{dc}$, and $4V_{dc}$). Table 1 explains the multilevel cases of the output inverter voltages. Figure 2 explains the connection diagram for selected mode of operation according to switching states explained in Table 1. Figures 2(a) V_{Load}=2 V_{dc}, (b) V_{Load}=-3V_{dc}, (c) V_{Load}=4V_{dc}, and (d) V_{Load}=7V_{dc}. The states of the power transistor switches named as T1 to T7 and the diodes D1 and D3 are assigned as (0) for the off condition and as (1) for the on condition. For example, to get $2V_{dc}$ output we implement column 3 in Table 1 and the same procedure is followed for outputs for $0V_{dc}$ to $7V_{dc.}$

Table 1. Switching mode operation

Level / switch	0 V_{dc}	1 V_{dc}	2 V_{dc}	3 V_{dc}	4 V_{dc}	5 V_{dc}	6 V_{dc}	7 V_{dc}
T1	0	1	0	1	0	1	0	1
T2	0	0	1	1	0	0	1	1
T3	0	0	0	0	1	1	1	1
T4	0	1	1	1	1	1	1	1
T5	0	1	1	1	1	1	1	1
T6	0	0	0	0	0	0	0	0
T7	0	0	0	0	0	0	0	0
D1	0	0	1	0	1	0	1	0
D2	0	1	0	0	1	1	0	0
D3	0	1	1	1	0	0	0	0

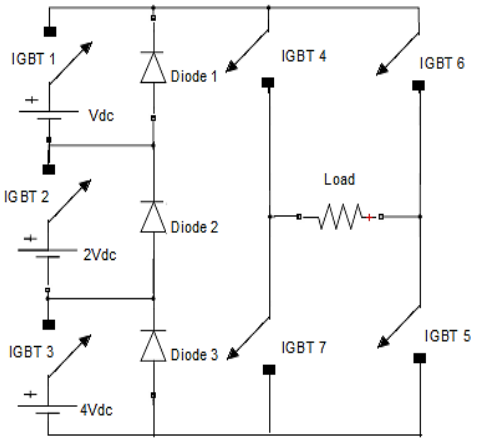


Figure 1. Suggested 15-level inverter circuit

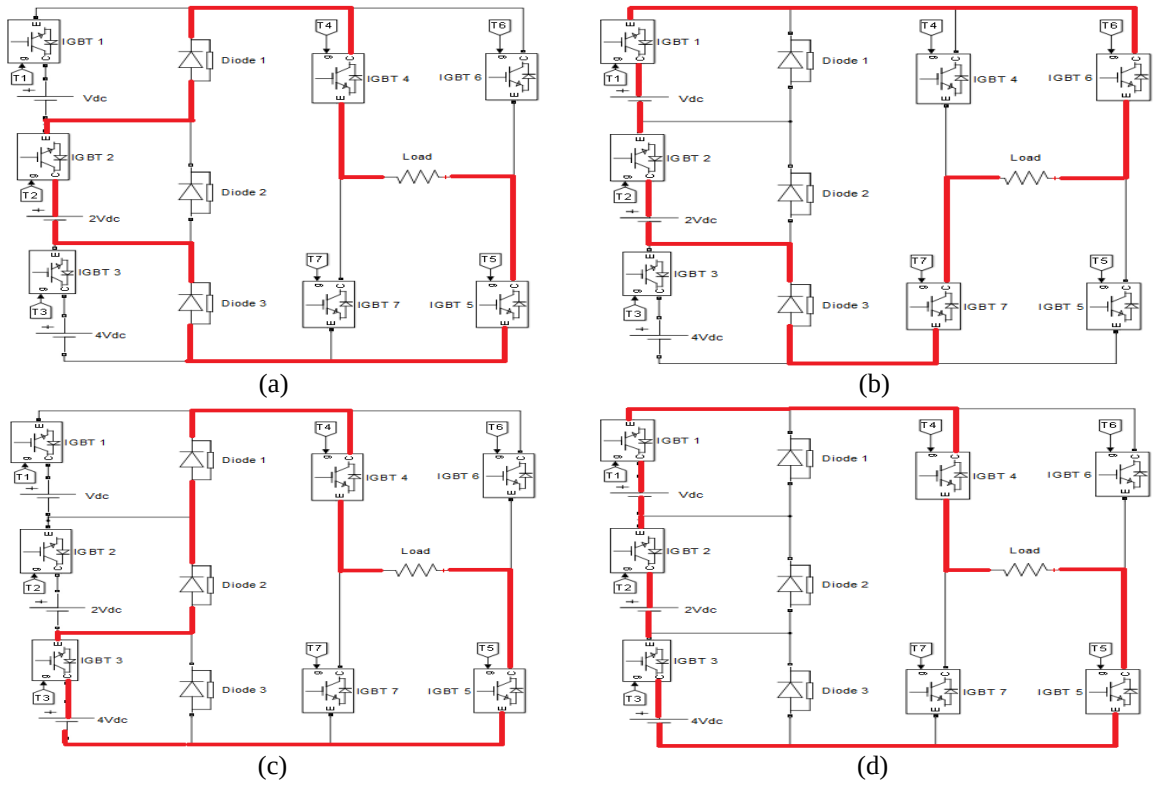


Figure 2. Circuit configuration cases of the proposed multilevel topology: (a) $V_{Load} = 2\ V_{dc}$, (b) $V_{Load} = -3V_{dc}$, (c) $V_{Load} = 4V_{dc}$, and (d) $V_{Load} = 7V_{dc}$

3. MASPWM CONTROLLER

In order to drive the multilevel inverter switches, different PWM techniques were used. In this paper, a modified absolute sine PWM (MASPWM) controller suggested by [9] is used and modified to get multilevel output voltages. It has ability to dive the multilevel inverter to get different output levels with zero-level state and none zero (NoneZero) level state as illustrated in Figure 3. Its principle depends on producing reference signal, reference MASPWM signal. The procedure of this control focuses on sensing positive and negative zero crossing points of the sine signal with amplitude represents the required output voltage level. Then converting absolute sine signal to discrete type. The differences between these two signals gives MASPWM signal as shown in Figure 3. After that, the MASPWM signal is compared with one triangular signal to create PWM pulse. The final step is programming embedded s-function, according to the Table 1 and the created PWM pulse, to get and spread pulses over the IGBTs of the multilevel inverter depending on the required output level. The MASPWM controller can offer different output voltage levels relying upon the structure of the DC input voltage. Consequently, fifteen levels arise in the output voltage of the suggested multilevel inverter.

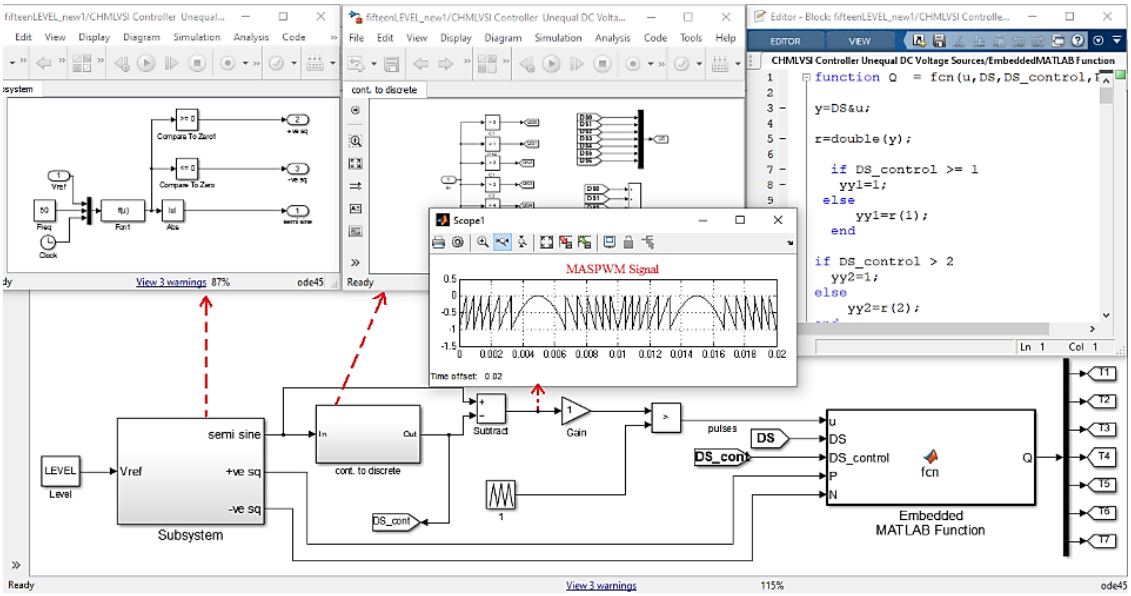


Figure 3. MASPWM controller circuit

4. SIMULATION RESULTS

The suggested single-phase multilevel inverter based on MASPWM controller with Zero-level and NoneZero-level states using less power electronics switching devices is designed and reformed by MATLAB/Simulink. The DC input voltages are selected equal to 5, 10 and 20V with 3 kHz carrier frequency and 100Ω load. The multilevel inverter waveforms of the output voltage(v_s), output current(i_s), with Zero-level and NoneZero-level states at 5-level are shown in Figure 4. Figure 4 (a) output voltage and current, Figure 4 (b) FFT spectrum using Zero-level state, Figure 4 (c) output voltage and current, and Figure 4 (d) FFT spectrum using NoneZero-level-state. Figure 5 shows simulation results of the 15-level inverter, Figure 5 (a) output voltage and current, Figure 5 (b) FFT spectrum using Zero-level state, Figure 5 (c)output voltage and current, and Figure 5(d) FFT spectrum using NoneZero-level-state. These figures explain that the THD values of NoneZero-level state is less than Zero-level state which prove that the system without zero-state gives quality better than with zero-state. The THD value of the output is 24.056% with Zero-level and 21.14% with NoneZero-level state at 5-level. While it is equal to 3.3904% with Zero-level state and 3% with NoneZero-level at 15-level. The MASPWM controller can be set and programmed to have output voltage and current waveforms with Zero-level and NoneZero-level states. The THD results of the suggested multilevel inverter at different output levels is shown in Figure 6. It can be seen that THD results for NoneZero-level case is less than with Zero-level. The THD values at different output voltage levels is reduced by 12% depending on NoneZero-level state. The performance of the suggested circuit is improved with NoneZero-level compared with Zero-level which is illustrated by THD waveforms.

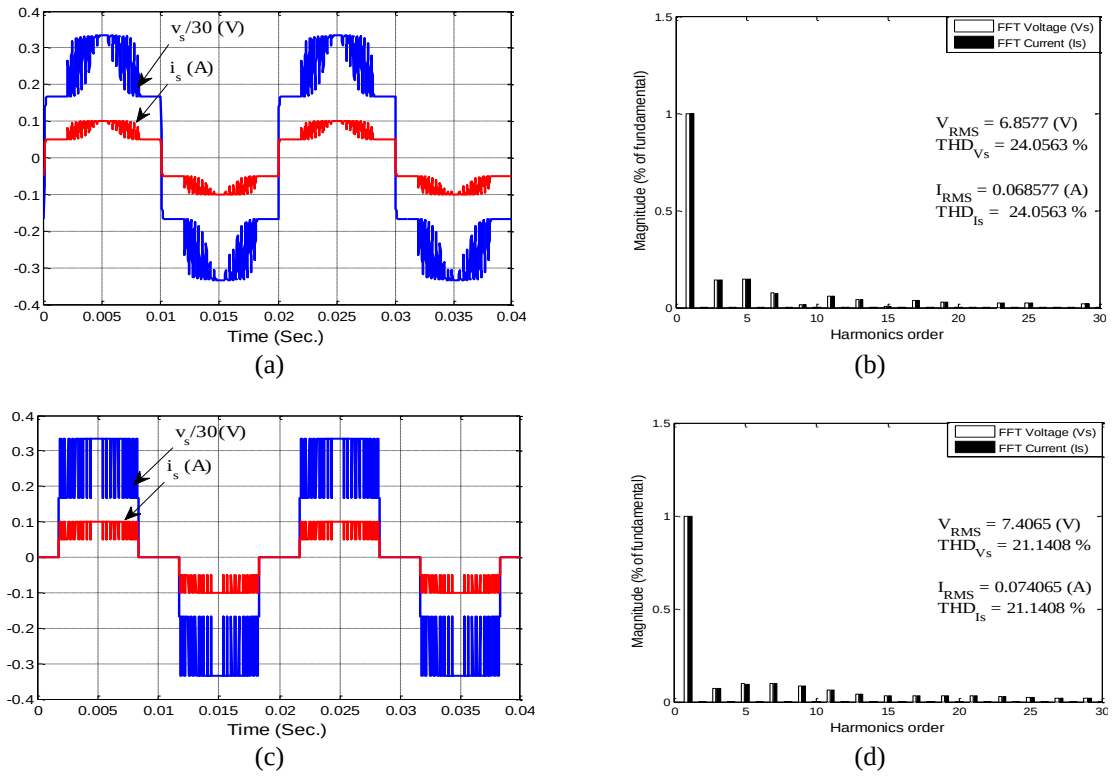


Figure 4. Simulation results of the 5-level inverter: (a) output voltage and current, (b) FFT spectrum using Zero-level state, (c) output voltage and current, and (d) FFT spectrum using NoneZero-level-state

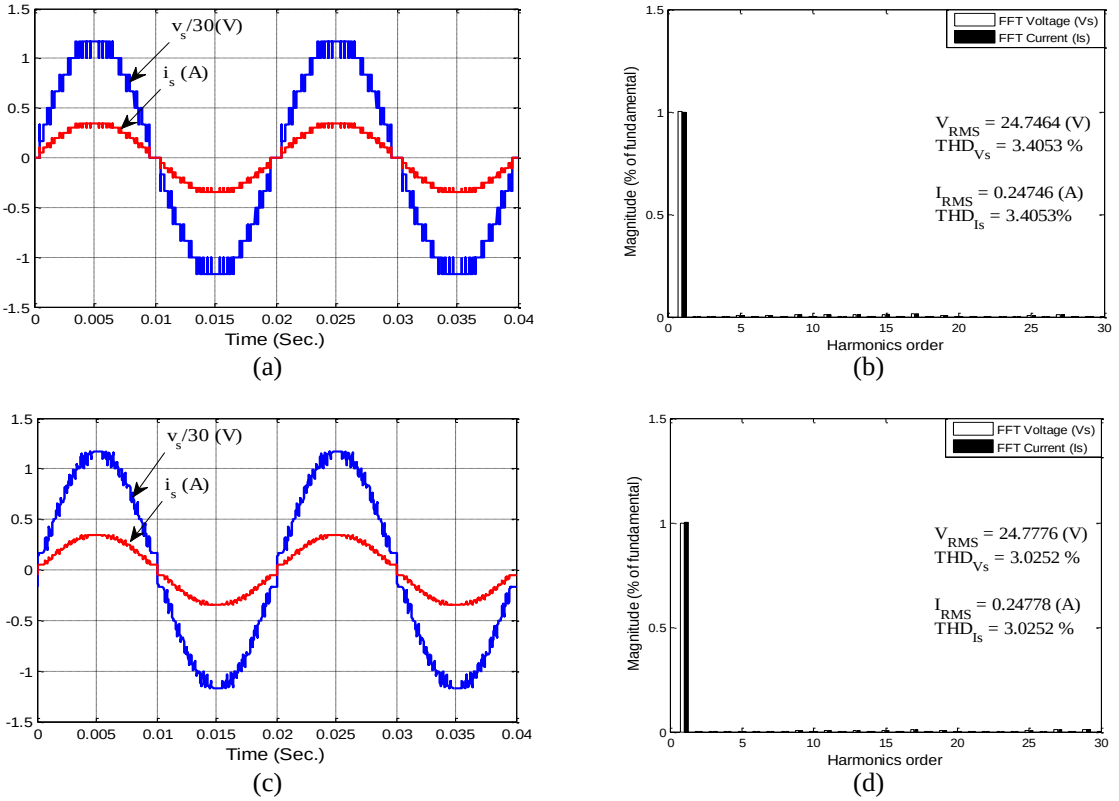


Figure 5. Simulation results of the 15-level inverter: (a) output voltage and current, (b) FFT spectrum using Zero-level state, (c) output voltage and current, and (d) FFT spectrum using NoneZero-level-state

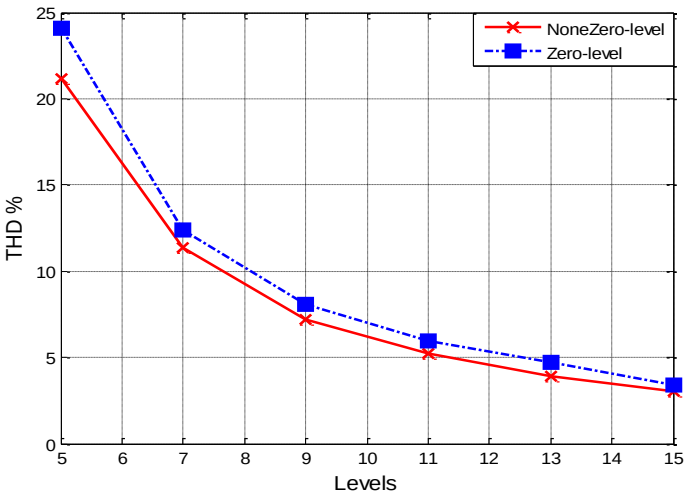


Figure 6. Simulation THD results of the output voltage for different levels with zero and NoneZero states

5. EXPERIMENTAL RESULTS

An Arduino is used in this study as a data acquisition data acquisition card (DAQ). The gating signals for the proposed MLI hardware are derived from the MATLAB/Simulink software in three steps. Firstly, the power switches gating signals are extracted as time pulses and stored in 20,000 samples for each switch transistor and for one complete cycle at a desired frequency of 50 Hz. Secondly, high and low, instants of time pulses are converted to true or false respectively in a text file. Then, a C# program is developed to read five files and transform them to an appropriate matrix form that is compatible with Arduino software. The C# program reads the first-time signal values from each of the five files and rearrange them in an 8-bit form. The later 8-bit values are then stored for the next high or low time signals. This process is repeated for one complete cycle, i.e. 20msec. When all are completed, a file named "array-X" will save all the on-off gating instants for each desired level. Here X stands for 5, 7,9,11 and 15 MLI respectively. Finally, a program is initialized to output a hardware digital gating signals to the power transistor switches through an appropriate output Port in Arduino and the cycle is repeated endlessly. A dead time of 1μs is taken into consideration to avoid a possible short circuit within any part of the MLI topology. The suggested MLI circuit is implemented experimentally. The complete experimental system is divided into four modules and discussed briefly. The first stage is pulses generator unit using Arduino kit, which is considered as a drive circuit. The gate drive circuit includes the Arduino pulses kit of the IGBTs and an optical isolated input-output. The second stage is the power circuit, which is constructed based on the power circuit illustrated in Figure 1 using seven IGBT switches and three diodes. The third stage is the R-load having 100 ohms. The fourth stage is the DC sources, which is three DC supplies of 5, 10, and 20V. The experimental circuit performs, executes, and carried out. Simulation and experimental results shown in Figure 7 (see Appendix) represents the output voltage and current waveform of the 5, 7, 9, 11, 13, and 15 levels at switching frequency of 3 kHz and NoneZero-level state.

The output voltages and currents frequency are 50Hz as expected and shown at each section of Figures 7 (a)-(f). The simulation results at this part are in good agreement as compared with the practical results. The transient output voltage and current waveform at levels from 5 to 15-level with NoneZero-level is shown in Figure 8. This figure shows level 5, 7, 9, 11, 13, and 15 at a preset value of time for each level. This is accomplished by proper instructions in the C# program. Then the program is uploaded to the Arduino Due via the Arduino software. Again, the simulation and practical results agreed with each other. The THD values at levels of 5-15 levels for NoneZero-level are explained in Figure 9. The slight differences between the simulation and practical results is a possible outcome of the ideal consideration of the components suggested by the Simulink MATLAB software. The THD measurements are taken with Huazeng portable three-phase power quality analyzer device. These results explain the effective of the proposed circuit and controller to get the required output voltage with minimum THD value which demonstrated the success of the proposed circuit and controller.

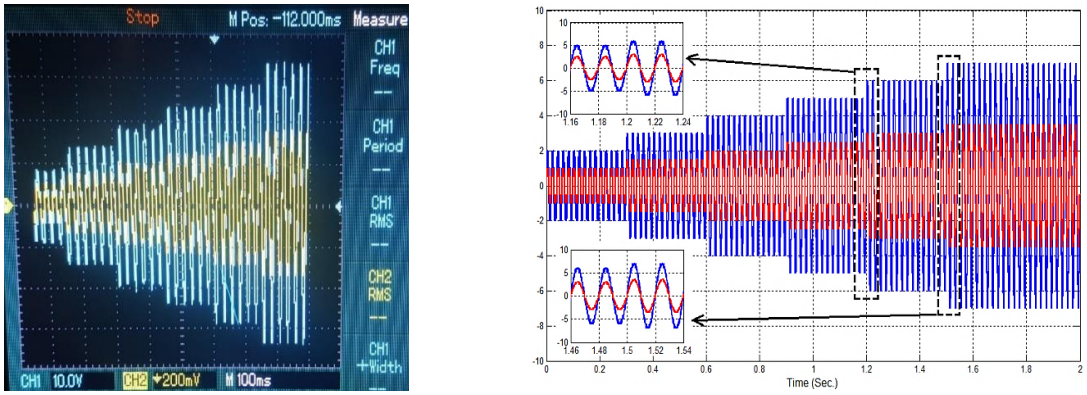


Figure 8. Experimental results of output voltage for different levels with NoneZero state and simulation results of output voltage and current at different levels with NoneZero state

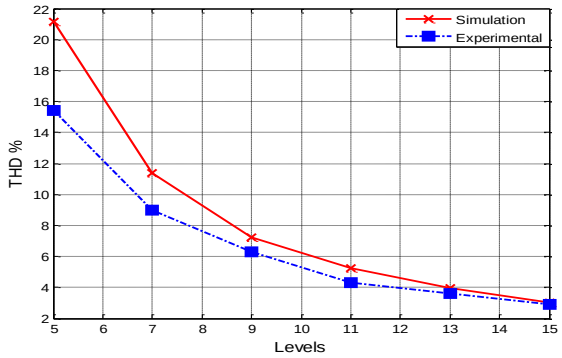
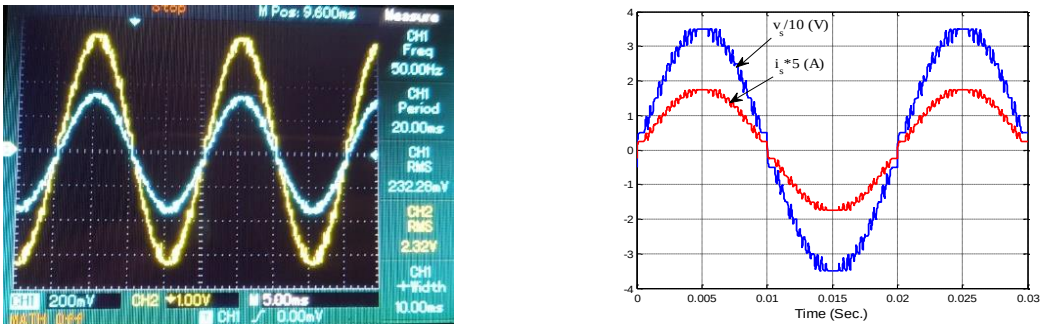


Figure 9. Experimental and simulation THD results of the output voltage with NoneZero-level states

6. CONCLUSIONS

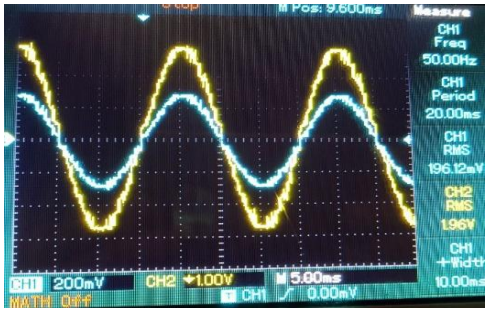
In this paper, a MLI with 7-switches and 3-unequal DC sources has been recommended. The significant of the circuit is to demonstrate the effectiveness of the circuit with MASPWM controller and NoneZerol-level state. This circuit provides THD values less than with zero voltage state. In addition, it is built to produce 5 to 15 output levels with less THD than conventional form. The experimental setup of the proposed circuit has been built in Lab. Simulation and experimental results show clearly the reduction of the THD for NoneZero level compared to zero level. The success of the proposed circuit with and without zero state is accompanied with acceptable distortion rate which verify that the system can work in both zero-level and NoneZero-level states with acceptable THD values. The THD values with NoneZero method are less than with zero state method as illustrated in the simulation and experimental results.

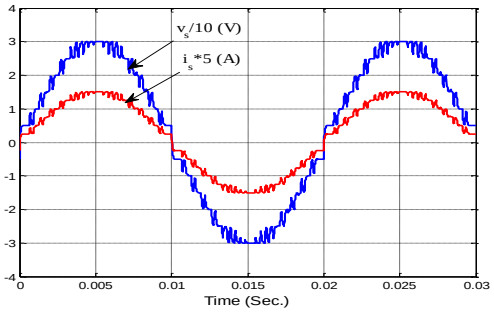
APPENDIX



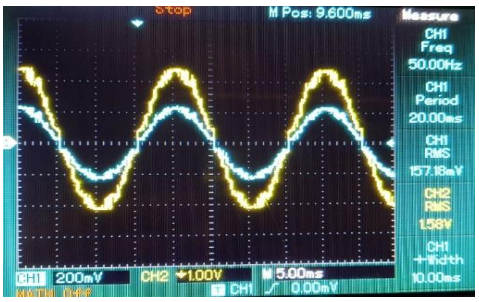
(a)

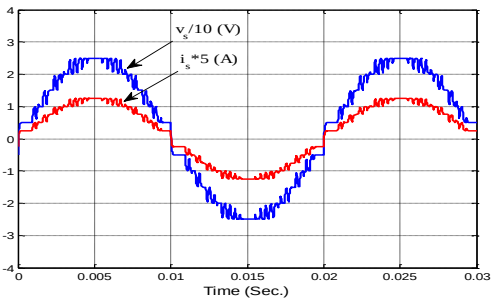
Figure 7. Practical and simulation results of output voltage and current with NoneZero-level: (a) 15-level



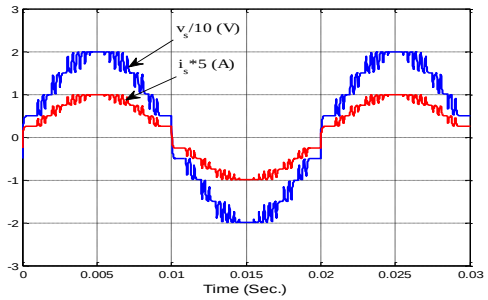


(b)





(c)



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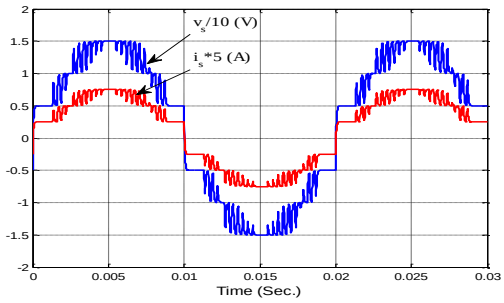
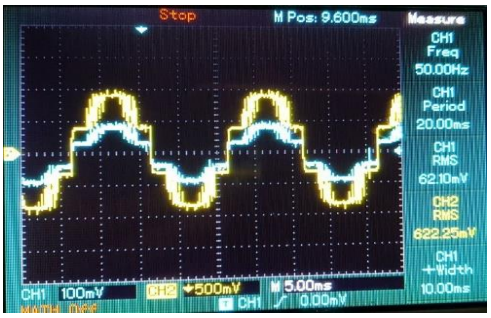
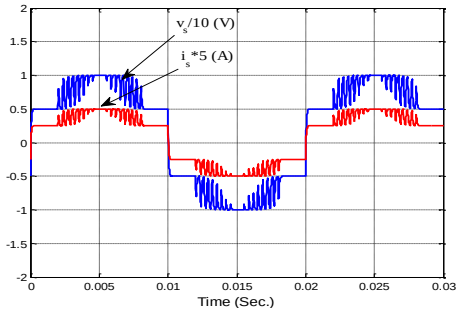


(e)





(f)

Figure 7. Practical and simulation results of output voltage and current with NoneZero-level: (b) 13-level, (c) 11-level, (d) 9-level, and (e) 7-level and (f) 5-level (*continue*)

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