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Performance analysis of capacitor voltage balancing in modular multilevel converter by sorting algorithm

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ABSTRACT

Due to the modularity of modular multilevel converter (MMC), therefore it has been considered as a substitute for the diode-clamp multilevel inverter in applications of high-voltage high-power. Where it can obtain any level of voltage without imposing complexity on the control system. This study analyses in detail the operation principle and balances the capacitor voltage of sub-module (SM) in modular multilevel converter by sorting algorithm. The output voltage control and capacitor voltage balancing technique are confirmed by MATLAB/Simulink and the obtained result has been discussed, where the capacitor voltage of the sub-module has controlled within the acceptable deviation limit, which is 5-10%. In addition, the circulating current has been controlled and reduced.

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1. INTRODUCTION

The modular multilevel converter (MMC) considers a novel version of power electronic converters. The schematic diagram of MMC is shown in Figure 1(a). It is made up of three identical arms, which could be named phases or legs, they are connected in a parallel manner and fed by DC voltage source V_d. Each phase has 2n sub-modules (SM) that are identical in each arm (phases). The inverter output is taken from the middle point of each leg. The diagram of the sub-module is illustrated in Figure 1(b), where the circuit is built by two IGBTs with a diode connected antiparallel to each switching device, and there is a capacitor, which is charged to the voltage V_c.

2. OPERATING PRINCIPLE

The switching devices IGBT of the Sub-module are turned on in opposite direction, where if T_1 is ON, T_2 is OFF and vice versa. Hence, the terminal voltage $V_{xy} = V_c$. On the other hand, when T_1 is OFF and T_2 is ON, the voltage $V_{xy} = 0$. Therefore, the semi-phase voltage V_{a1} or V_{a2} would vary from 0 to nV_c. The capacitor voltage value V_c. should be equal to V_d/n. The sub-modules are controlled in such a way, that in one arm the n sub-modules are in an active state at any instant [1]–[5]. Thus, the voltage of the semi-phase changes from 0 to V_d.

The sinusoidal modulation technique is used for operating the switching devices. Therefore, the reference voltage used for operating phase A (upper and lower semi-phase) is given by:

$$V_{ref1,2} = \frac{V_d}{2} \pm \frac{mV_d}{2}\ sin\omega t \quad (1)$$

where m is the modulation index and its value $0 \leq m \leq 1$. The reference voltage equation for the other phases, B and C, is the same as that of A, but with a phase shift 120° for B and 240° for C. If it is required to increase the voltage, a third harmonic would be injected to the reference voltages, that would lead to increase the modulation index to 1.15. The line-line voltage equation is expressed by:

$$V_{ab} = \frac{V_d}{2} + \frac{mV_d}{2}\ sin\omega t - \left(\frac{V_d}{2} + \frac{mV_d}{2} sin\left(\omega t - \frac{2\pi}{3}\right)\right) = 0.866\ m\ V_d\ sin\ \left(\omega t + \frac{\pi}{6}\right) \quad (2)$$

The currents shown in Figure 1(a), can be expressed as:

$$i_{phase} = i_{upper} - i_{lower} \quad (3)$$

$$i_{upper} = \frac{1}{3} i_{dc} + i_{circulating} + \frac{1}{2} i_{phase} \quad (4)$$

$$i_{lower} = \frac{1}{3} i_{dc} + i_{circulating} - \frac{1}{2} i_{phase} \quad (5)$$

where i_{phase} , i_{upper} , i_{lower}, and $i_{circulating}$ are the output phase current, upper arm phase current, lower arm phase current, and circulating phase current respectively.

The expression of DC link voltage of MMC can be defined as:

$$\frac{V_d}{2} = \frac{(V_{upper\ arm} + V_{lower\ arm})}{2} + L\left(\frac{di_{circulating}}{dt}\right) + r i_{circulating} \quad (6)$$

$$V_{phase} = \frac{(V_{lower\ arm} - V_{upper\ arm})}{2} \quad (7)$$

$$V_{upper\ arm\ (a1)} = \frac{V_d}{2} - V_a - L\left(\frac{di_{(a1)}}{dt}\right) - r\ i_{(a1)} \quad (8)$$

$$V_{lower\ arm\ (a2)} = \frac{V_d}{2} + V_a - L\left(\frac{di_{(a2)}}{dt}\right) - r\ i_{(a2)} \quad (9)$$

One of the benefits of such converters is the modularity, which enables to build of high voltage converters and dispense (give out) the use of transformers for high voltage network connections. Another advantage is the ability to replace the faulted module and then easy maintenance; this would increase and improve the system's reliability and sustainability. The MMC gained wide applications in high voltage direct current (HVDC), where the industry produced MMC, with a number of the sub-modules in each phase would reach 200 for power up to 400 MVA and the voltage would reach as high as 200 kV.

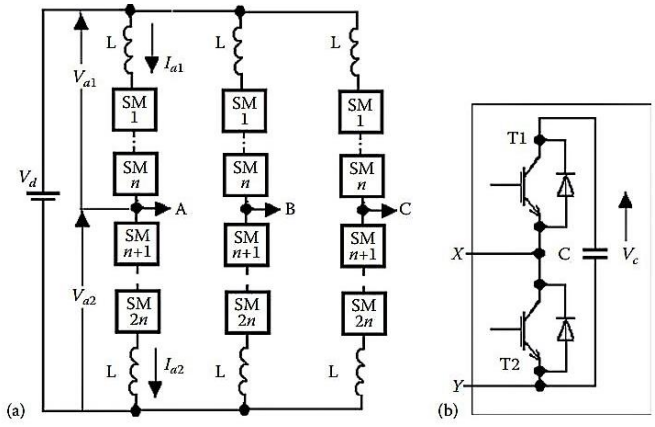

Figure 1. The modular multilevel converter MMC: (a) a schematic diagram of MMC and (b) the diagram of sub-module

There is a challenge in developing a control system to operate a large number of sub-modules, where it is difficult to use PWM for every sub-modules. However, there are many types of research have been conducted in this area and many control techniques have been proposed and developed ever since. In this paper, the simpler version of this control technique would be investigated and explained in detail. Where the reference modulation voltage expressed earlier is employed after dividing it by V_c. After that, the resulting voltage is rounded to the total number, therefore the k modules that must be operated or in an active condition are found. The whole operation process is conducted every $T_{me} = 1/F_c$ which will be explained n detail later [6]–[9].

The period of PWM is T_m and arm reference voltage V_{ref} is fixed. The function $floor$ and rem would be employed for the switching operation process. Where, the integral part and the fractional part as well, would be calculated of the value V_{ref}/V_c. During the subsequent period T_m, $k = floor(V_{ref}/V_c)$ decides the times that sub-modules are required to be enabled. While, $k_{pwm} = rem(V_{ref}/V_c)$ gives guidance of which fraction of the next period of T_m, $k + 1$, the sub-modules SM that are desired to be enabled. Thus, the SM would be operated in a PWM manner, where in the period mentioned, the voltage average value would equal to the used reference voltage [2], [5], [8].

The capacitor voltage balancing is conducted due to the advantage of redundancy and this occurs because most interval of modulating signal $k + 1$ less than n. This is conducted as follows; Initially, the sub-module capacitor must be charged to the voltage V_c. That can be performed by using a low power source, where the output voltage is connected instead of the source V_d. Firstly, in each sub-module, the switches T_1 are turned ON. Then, after turning ON the switches T_1 in each sub-module (T_2 is switched OFF), there will be sufficient time to charge the capacitor; after that, the process is reversed, where T_2 is switched ON and the sub-module's capacitor will be in the storage mode. After $2n$ cycles and to charge the capacitor, all the capacitors are put out, and at the same time, all the phases would be charged.

For the mentioned process, the system would act accordingly. Where, if the current flowing in the semi-phase is greater than zero, the active capacitors in the sub-modules would increase their voltage, which means when T_1 ON the sub-module capacitors make a contribution in voltage of the phase. The process is the opposite when the semi-phase current is less than zero, where there will be decreasing in the voltage of active sub-module capacitors. Hence, if the current is greater than zero, the k sub-module having the smallest voltage must be set to be in active states, and the sub-module with high voltage would operate in PWM mode. When the current is less than zero, the process is vice versa, where the sub-modules that are in active states are the ones with the largest voltage, and the next sub-module in PWM mode is the one with a low voltage value. In this operation mode, the loads can be balanced on different inverter sub-modules.

It is required to perform voltage control across a three-phase load of 4 Ω, 1 mH, and $V_d = 10$ KV. The diagram shown earlier has been used to build the model with sub-modules $n = 10$ in each arm. It has been assumed that all the sub-modules capacitors have charged to the voltage 1000 V already. In the semi-phases or upper arm of each phase a1, b1, and c1, the quantities k and k_{pwm} are implemented. The system acts with a periodicity equal to $1/F_c$, where the carrier frequency $F_c = 1$ kHz. The signal of such frequency is made by using a pulse generator, which is named T_{me}. With the help of this signal and zero-order hold elements, it can achieve the clamping of calculated and measured values.

The inputs of SORT are the sign of semi-phase current, the output of PWM, the quantity k, and the voltage vector across the sub-module capacitor in semi-phase and all these are designated by $V_c = [V_{c1}, V_{c2}, V_{c3}, V_{c4}]$, for the sake of simplicity four modules have been considered in this explanation. In order to order the vector components, a function from MATLAB® is employed, which is $[B, IX] = SORT(V_c)$. When this function is conducted, vectors B and IX will be formed. The vector components V_c are organized in ascending order and are contained in the former B, and the second vector IX contains indices of the components in an order that is positioned in the vector B. An example for illustrating the process is that if $V_c = [1050, 980, 1060, 990]$, then $IX = [2, 4, 1, 3]$. The role of the commutator changer, shown in Figure 2, is to change the order of the index to opposite one IXi; it should be mentioned that based on the sign of current in the semi-phase, the vectors IXi or IX would be used. To select the active sub-modules in a semi-phase, a block called SORT would be used. The input circuit for control MMC is shown in Figure 2.

The *selector* would select, from the input vector components, one that is corresponding to the total number at the selector Control Input *CI*. When $CI = 1$, then it will select the first component, and when $CI = 2$, t will pick the second component, and so on. For example, let $K = 4$ and the modules 5, 3, 9 and 7 have the minimum capacitor voltages, thus, in block 1, $CI = 4$, so that the output select would be 7; in block 2, $CI = 3$, so that the output *select* would be 9, in block 3, $CI = 2$, so that the output *select* would be 3 and in block 4, the output *select* would be 5. For blocks 5-10, the outputs of *select* is less than 1, therefore the adder $Sum2$ in the diagram of control of MMC is set for preventing the failure. Where it sends to the comparison some of the ineffective numbers, for example, 100.

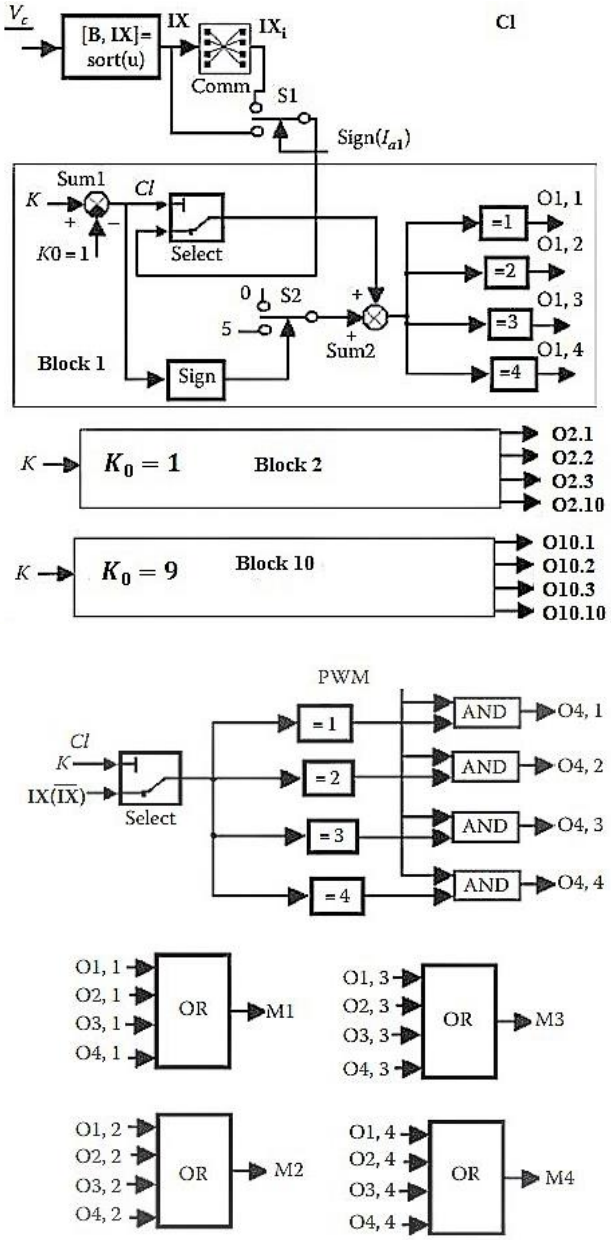

Figure 2. A schematic diagram of MMC control

Therefore, at the outputs O1.7, O2.9, O3.3, and O4.5 of the blocks 1, 2, 3, and 4, there will be logic 1, while in the other blocks the outputs will be logic 0. The control signals of the sub-modules M1-M10 are formed with the help of OR gates. That justifies the explanation mentioned earlier, which states that the gate pulse will be sent to the modules with minimum capacitor voltages, which are modules 3, 5, 7, and 9.

The operation of sub-module $k + 1$ by PWM is performed in the following manner. The integrator is reset when the successive pulse T_{me} has appeared, then it integrates numerically the signal which is equal to F_c. When the output of the integrator is less than k_{pwm}, the comparison block output there will be logic 1, hence, the sub-module $k + 1$ is in an active condition. While if the integrator output is greater than k_{pwm}, the logic 0 would be on the output of comparator $Comp$ as shown in Figure 3, then deactivate the sub-module. It should be mentioned that in the negative semi-phase, the value k is a complement of nine compared to the value k in the positive semi-phase. In doing so, it is realized strictly that there is a condition states that in a phase, the number of active sub-modules must be equal to n. The PWM generation control is illustrated in Figure 3.

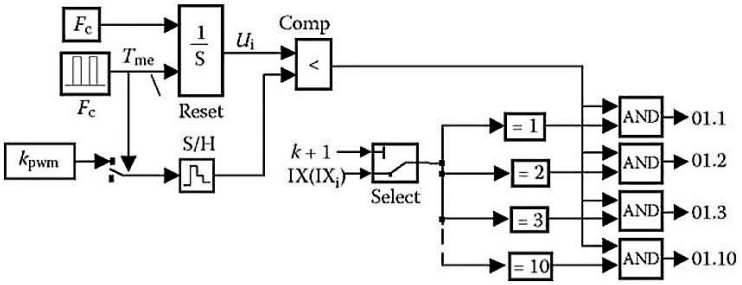

Figure 3. A schematic diagram of PWM controls the successive module

3. CIRCULATING CURRENT SUPPRESSION

Referring to (3)–(5), the occurrence of circulating current could be attributed to pulsation in capacitor voltage, the circulating current does not appear in the output current of the converter. By using (2) and equating the DC and AC power, the relation between DC current and peak of output phase current I_{peak} could be obtained.

$$I_{dc} = \frac{3}{4} m I_{peak} \tag{10}$$

From (4), (5):

$$i_{circulating} = \frac{i_{upper} + i_{lower}}{2} - \frac{1}{3} I_{dc} \tag{11}$$

There are even harmonics in the circulating current, the second one among them considered the largest harmonics [10]-[19]. This current should be decreased because it burdens the elements in the system. The resonant controller is used to reduce the circulating current, and its' transfer function is expressed by:

$$G(s) = K_{res}(s/s^2 + {\omega_{res}}^2) \tag{12}$$

where ω_{res} is the resonant frequency and is selected to eliminate the second harmonic in the circulating current.[20]–[28] The reason for using this controller is to obtain zero steady-state error, where this controller provides infinite gain at the AC resonance frequency ω_{res}. The control diagram for circulating current is shown in Figure 4.

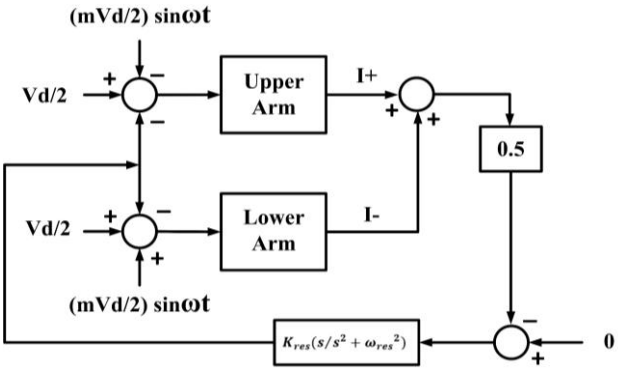

Figure 4. The control diagram of circulating current

4. RESULTS AND DISCUSSION

If it is desired to control the output voltage, a three-phase sinusoidal signal with an amplitude less than 1.15, a frequency of 50 Hz, and a third harmonic injection would be generated by using PI voltage controller. The output of the voltage controller is the amplitude-modulated reference signal, which is multiplied by phase

voltage base value 4 kV. The simulation has been conducted for the amplitude-phase voltage reference to be 5000 V and is increased up to 7000 V at $t = 1\ sec$. The parameters used are shown in Table 1. The responses of the simulation system, line to line load voltage and load current, the first harmonic magnitude of phase A voltage are shown in Figure 5. The measured voltages have tracked the reference and the currents have a sine shape.

Table 1. The system parameters

Parameter	Value	Unit
DC link voltage V_d	$10k$	Volts
Number of SM n	10	Modules
Carrier frequency f_c	$1k$	Hz
Base voltage	$4k$	Volts
Load resistor	4	Ohm
Load inductor	0.1	mH
SM capacitor	6	mF
Arm inductance	0.01	mH
Reference output voltage	$5-7\ k$	Volts
Resonant frequency	$2\pi \times 100$	Rad/sec
Resonant gain K_{res}	100	non

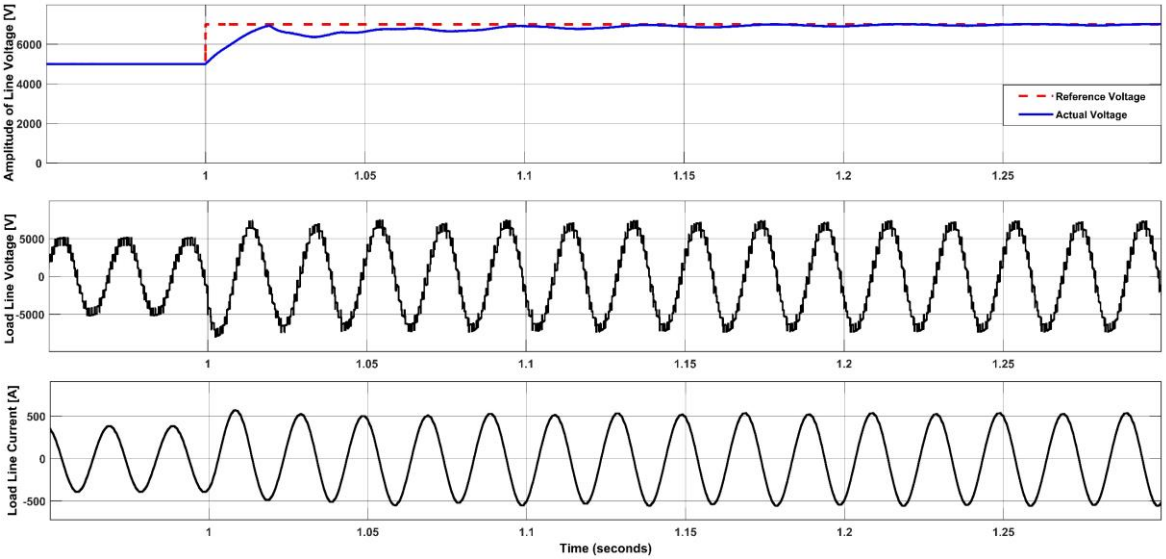

Figure 5. Amplitude and line load voltages and currents

The capacitor voltages of the sub-modules phase A upper arm and their average value are shown in Figure 6. The sorting algorithm is bubble sort algorithm, which makes sure that the voltage DC voltage of the capacitors are balanced over time. In Figure 6, it has been observed that the average value of capacitor voltage is approximately 1000 V, which would ensure real power flow from DC to AC and vice versa, where without sorting, the capacitor voltage will deviate. The acceptable level of capacitor voltage deviation range is within $\pm(5-10)\%$ from the capacitor voltage.

The voltages of the semi-phases a1 and a2 are shown in Figure 7. The arm currents have both AC and DC components, if the ripple of the capacitor voltage is neglected, then half of the load current will flow through the arm at the fundamental frequency. It should be mentioned that the arms current would have DC components to maintain power balance. Because of single-phase power flow, 2nd harmonics voltage ripple would appear across the capacitor voltage, this would make the 2nd harmonic voltage appear in the arms. Therefore, the arms current has higher harmonics. Refer to (4) and (5), which would imply the circulating current has higher harmonics (mostly 2nd harmonics and fundamental) and DC components, which then would be reflected on the arm voltage as well. In Figures 7(a) and 7(b), the upper and lower voltages are identical and they have DC and AC components. The output phase voltage with respect to the mid-point of the DC bus is shown in Figure 7(c), which satisfies (7), where the switching delay between upper and lower arms has been neglected, hence the voltage components related to the circulating current are neglected. Figure 7(d) is the phase A voltage with respect to neutral point of the load.

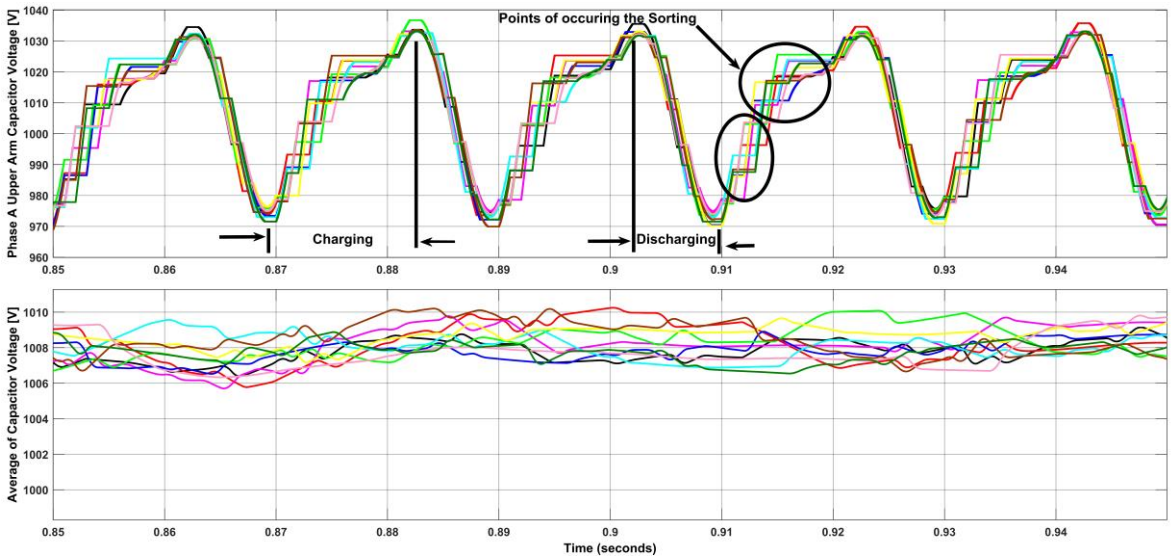

Figure 6. Capacitor voltages of phase A upper arm and their average

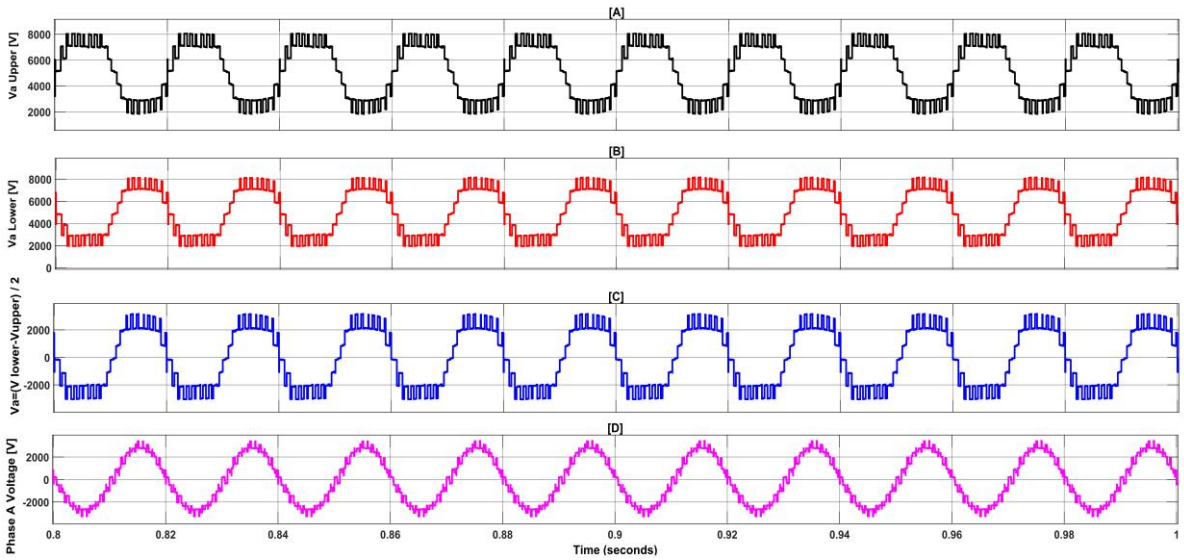

Figure 7. The voltages of the semi-phases a1 and a2: (a) the voltage of phase A upper, (b) the voltage of phase A lower arms, (c) the output phase voltage with respect to mid-point of the DC bus, and (d) phase A voltages

It is noticed that the load current in Figure 5 is sinusoidal, however, the currents of semi-phase Figure 8 are not sinusoidal, where there are irregularities that are attributed to the frequent sub-modules commutation. The fluctuation of capacitor voltages is the reason for the second harmonics in the arms current. Where the sub-modules capacitor voltage variation would make the three phases, which are connected in parallel, may have different voltages. That would make the circulating current flow in the arm of each phase and distort the arm current, which would increase the rms semi-phase current and converter losses.

Three resonant controllers are used, and the input to them is the first part of (12). The output of the resonant controller is added to the modulation signal, this is shown in Figure 4. The controller of the circulating current is set to be activated at $t = 1.5\ sec$, and it has been observed that the circulating current has reduced considerably from 225 A to 75 A rms, as shown in Figure 9. The reduction in the circulating current would have an impact on the pulsation of the capacitor voltage, which would be reduced slightly as well.

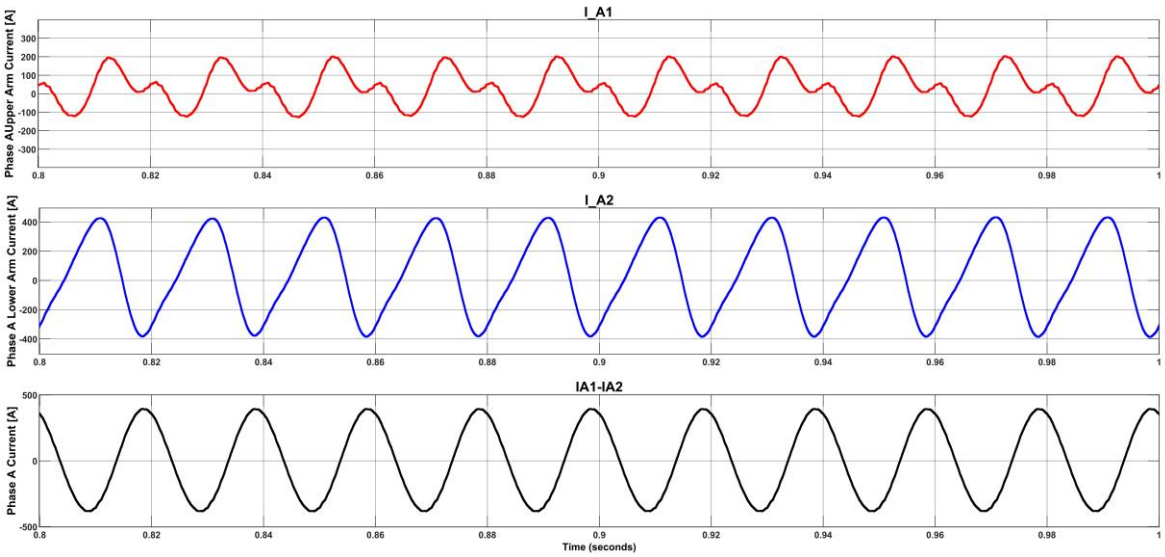

Figure 8. Upper and lower arm current and load phase current

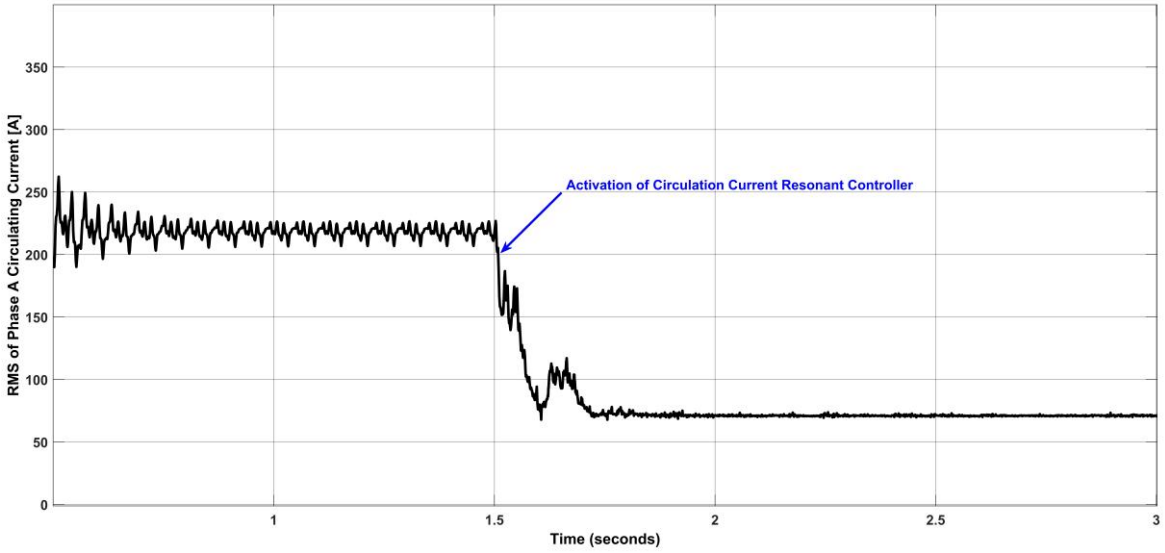

Figure 9. RMS of phase A circulating current

5. CONCLUSION

The operating principle and strategy of capacitor voltage balancing for MMC with 10 sub-modules per arm have been discussed. The MMC shows its' superiority in terms of attaining the capacitor voltage balancing for any number of levels, and that does not depend on the modulation index, power factor of the load, and the unbalance. It is shown that for equal periods, switching devices have been used. In the steady-state, the capacitor of each cell has been operated for T/((n-1)), n is the number of levels, which means that each capacitor would be used for a very short period of the fundamental at the increased number of levels, hence smaller capacitor would be used (cost reduced). The level-shifted PWM has been used and it is behind the scene, and since this method is used, therefore the switching frequency of the devices is directly equal to the carrier frequency. The THD is reduced extremely, specifically, if a high number of levels is used, this is also could be attributed to the method of modulation, which is level shifted PWM. The capacitor voltages settled at the average value within a feasible period of time. The procedure of capacitor voltage balancing has been analyzed and studied and the circulating current has reduced considerably. This paper could be considered as a step toward understanding and modifying the strategy of capacitor voltage balancing by the researchers.

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