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Design and performance analysis of asymmetric multilevel inverter with reduced switches based on SPWM

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ABSTRACT

Multilevel inverters have the benefit of producing high output voltage values with little distortion. This paper deals with decreasing total harmonic distortion (THD) and providing an output voltage with various step levels switching devices. In this study, a 27-level inverter with three asymmetric H-Bridge was designed and simulated based on level shift sinusoidal pulse-width modulation and phase shift sinusoidal pulse-width modulation methods. MATLAB/Simulink has been used to create this model and test it at different types of loads. The results showed that a multilevel inverter with (PS-PWM) produces less (THD) than a multilevel with (LS-PWM), when the resistive load was used, the produced voltage and current THD in (PS-PWM) and (LS-PWM) are 3.02% and 4.30% respectively, that has resulted from the linearity between voltage and current in the resistive load. While in the case of applying an inductive load, the THD in the voltage is constant in both (PS-PWM) and (LS-PWM) methods and has the same values as the THD in a resistive load. However, the THD in the current with inductive load decreased to 2.79% in (PS-PWM) and 4.04% in (LS-PWM). Finally, these results show that the performance of the proposed power circuit with PS-PWM is better than (LS-PWM).

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1. INTRODUCTION

Multilevel inverters (MLI) have recently been used to compensate for static variables, active power filters, and motor driving applications due to their multiple advantages including high-quality power, reduced switching loss, and the ability to work at a high level of voltage [1]–[5]. Multilevel inverter topologies are divided into three categories: flying-capacitor, diode-clamped, and cascaded inverters [6]–[8]. It has been used to control the cascaded H-bridge (CHB) for its flexibility and simplicity [9]–[13]. There are two types of CHB inverter, symmetrical and asymmetrical topologies [14]–[18]. Equal DC sources are used in the symmetrical MLI structure while unequal DC sources in asymmetrical MLI. Three separate output voltages are generated by each dc source linked to its H-bridge. +Vdc, 0, and –Vdc use numerous switching combinations with the four switches. Seven levels of output voltage are created using three symmetric H-bridges in cascade: +3Vdc, +2Vdc, +Vdc, 0, -Vdc, -2Vdc, -3Vdc. The literature proposes many techniques, using a five-level inverter to solve an electromagnetic disturbance problem in common mode [19], a seven-level inverter that operates on a DC supply and is controlled in real-time using artificial intelligence [20], [21]. By reducing the number of switches, the nearest state control and multicarrier-based SPWM schemes are the most common applications used for MLIs [22], [23].

In a cascaded H-bridge inverter, the output voltage levels are calculated as follows: m=2n+1, where n is the total number of H-bridge and m is the total number of levels, while asymmetric is formed with three H-bridge and different dc source values, (vdc, 3vdc, 9vdc) [11], so, the inverter will produce 27-level of voltage. All of these characteristics of cascade H-bridge multilevel inverter make it possible to use a variety of carrier-based PWM methods [17]. Therefore, carrier-based PWM employs many triangular carrier signals that may be altered in phase and/or vertical position to lower the output voltage harmonic content. A silicon carbide (SiC) switches inverter could be used to generate a sinusoidal voltage [24]–[26]. In this paper, a 27-level single-phase inverter is proposed and a new H-bridge design was tested, a three cascaded H-bridges with asymmetrical voltage sources are presented based on carrier pulse-width modulation techniques. Level-shift pulse-width modulation (LS-PWM) and phase shift carrier PWM technique (PSPWM) have been used in multilevel inverters to reduce THD and increase the output voltage.

2. PROPOSED 27-LEVEL INVERTER TOPOLOGY

Figure 1 shows the designed topology circuit diagram. Each cascaded H-bridge has been fed by the asymmetric voltage source [27], [28]. Whereas the magnitudes of the DC voltage sources are in the ratio 1vdc:3vdc:9vdc and the circuit can generate a 27-level output voltage with a range from +13Vdc to -13Vdc including zero voltage level. The level of the output waveform in this structure can be determined by using a formula: 3^n, where n is the number of H-bridges linked in cascade. While the inverter DC source voltage must be in the following ratio: 1vdc: 3vdc: 9vdc: 27vdc: 81vdc, etc. So, with two cascaded H-bridges, a 9-level of output voltage waveform may be obtained, while five H-bridges may give 243-level output waveform. Table 1 shows the configuration of the twelve -switches to create different voltage levels between +13Vdc and -13Vdc.

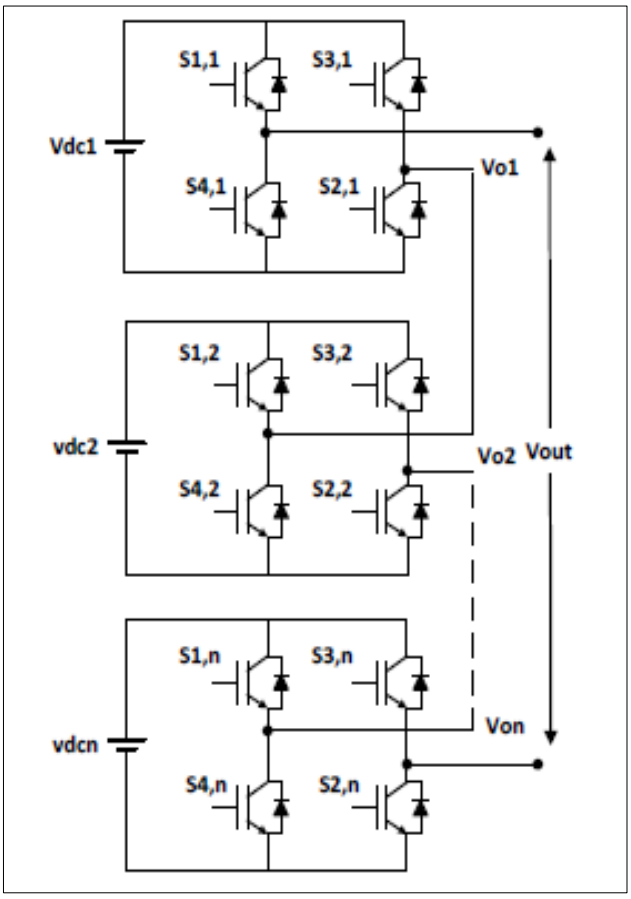


Figure 1. Proposed 27-level inverter topology

Table 1. 27 level inverter switching table

T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	LEVEL	OUTPUT
1	1	0	0	1	1	0	0	1	1	0	0	0	-13_{VDC}
1	1	0	0	1	1	0	0	0	1	0	1	1	-12_{VDC}
1	1	0	0	1	1	0	0	0	0	1	1	2	-11_{VDC}
1	1	0	0	0	1	0	1	1	1	0	0	3	-10_{VDC}
1	1	0	0	0	1	0	1	0	1	0	1	4	-9_{VDC}
1	1	0	0	0	1	0	1	0	0	1	1	5	-8_{VDC}
1	1	0	0	0	0	1	1	1	1	0	0	6	-7_{VDC}
1	1	0	0	0	0	1	1	0	1	0	1	7	-6_{VDC}
1	1	0	0	0	0	1	1	0	0	1	1	8	-5_{VDC}
0	1	0	1	1	1	0	0	1	1	0	0	9	-4_{VDC}
0	1	0	1	1	1	0	0	0	1	0	1	10	-3_{VDC}
0	1	0	1	1	1	0	0	0	0	1	1	11	-2_{VDC}
0	1	0	1	0	1	0	1	1	1	0	0	12	-1_{VDC}
0	1	0	1	0	1	0	1	0	1	0	1	13	0_{VDC}
0	1	0	1	0	1	0	1	0	0	1	1	14	1_{VDC}
0	1	0	1	0	0	1	1	1	1	0	0	15	2_{VDC}
0	1	0	1	0	0	1	1	0	1	0	1	16	3_{VDC}
0	1	0	1	0	0	1	1	0	0	1	1	17	4_{VDC}
0	0	1	1	1	1	0	0	1	1	0	0	18	5_{VDC}
0	0	1	1	1	1	0	0	0	1	0	1	19	6_{VDC}
0	0	1	1	1	1	0	0	0	0	1	1	20	7_{VDC}
0	0	1	1	0	1	0	1	1	1	0	0	21	8_{VDC}
0	0	1	1	0	1	0	1	0	1	0	1	22	9_{VDC}
0	0	1	1	0	1	0	1	0	0	1	1	23	10_{VDC}
0	0	1	1	0	0	1	1	1	1	0	0	24	11_{VDC}
0	0	1	1	0	0	1	1	0	1	0	1	25	12_{VDC}
0	0	1	1	0	0	1	1	0	0	1	1	26	13_{VDC}

3. CONTROLLING AND SWITCHING

For multi-level inverters, there is a variety of switching and controlling mechanisms. For example, multicarrier pulse width modulation (MCPWM) [17]–[21] and [22], selective harmonic elimination [15], and space vector PWM [16] can be used as modulation control techniques to regulate inverter modulation [29], [30]. In this research, a multicarrier technique will be divided into two types.

3.1. Level shift PWM (LS-PWM)

One of the most popular and straightforward switching strategies for multilevel inverters is a level-shift pulse-width modulation [12]. In the case of an m-level inverter, (m-1) carriers with the same carrier frequency (Fc) and the same amplitude (Ac) are arranged. The reference waveform has peak amplitude (Am) and fundamental frequency (fo). Each carrier signal is continually compared to the reference waveform. If the reference signal exceeds any carrier signal, the active device associated with that carrier is turned off. The modulation index (Mi) and the frequency ratio (Mf) in multilevel inverters are defined as:

$$Mi = \frac{A_m}{(m-1)A_c}) \quad (1)$$

$$Mf = (f_c/f_o) \quad (2)$$

In the continuous LS-PWM, depending on the position of the triangular carrier waves with respect to the reference signal, there are three different points to consider. Figure 2 shows the phase disposition pulse-width modulation (PDPWM) where all the carriers are in the same phase.

3.2. Phase shift carrier PWM

Phase shift carrier PWM is a different technique of PWM theories that uses a constant switching frequency [10]. All triangular carriers in this PWM scheme have the same frequency and peak amplitude. However, any two adjacent carrier waves have a phase change as shown by (3).

$$\theta = 360/((m-1)) \quad (3)$$

Where θ is phase angle between any two carrier waves and m is the number of the voltage level as show in Figure 3.

In this paper, two techniques of PWM will be applied, (LS-PWM) and (PS-PWM) for asymmetric three H-bridge to generate 27-level of the output voltage. A sine wave's frequency is the same frequency of the intended output voltage modulated by the carrier signal. As a triple-N number, the switching frequency of

the carrier signal must be higher than the frequency of the reference signal. When both signals are modulated, the signal pulse for the inverter's switching devices [7].

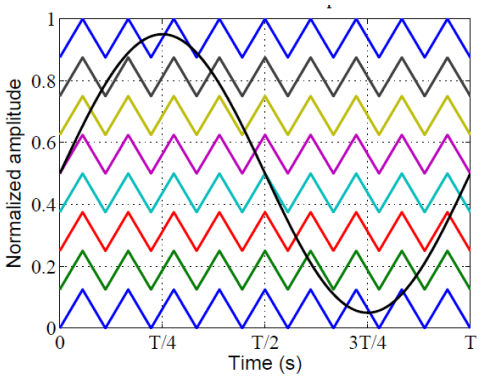


Figure 2. Phase disposition PWM

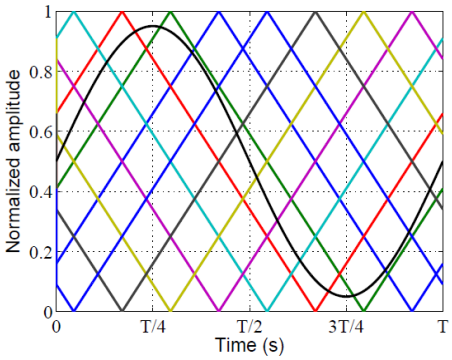


Figure 3. PSC PWM

4. RESULTS AND DISCUSSION

Figure 1 shows a single-phase 27-level inverter architecture with less power switching devices, that is built and reformed to achieve greater levels compared to other types. To test the performance of the proposed power circuit, the simulation is performed in MATLAB/Simulink. The circuit consists of three H-bridge with three dc sources (vdc, 3vdc, 9vdc) and twelve switches. R-load and RL-load are used to test the system by LS-PWM and PS-PWM. Figure 4 shows the output multilevel inverter voltage. Figures 5(a) and 5(b) show the system with PS-PWM where R-load is used, producing voltage THD lower than the system with LS-PWM, 3.02% and 4.30% respectively. Figures 6(a) and 6(b) show that the system with PS-PWM and RL-load produces lower voltage THD compared to the system with LS-PWM, 3.02% and 4.29% respectively. Figures 7(a) and 7(b) show that the system with (PS-PWM) and R-load produces lower current THD than the system with LS-PWM, 3.02% and 4.30% respectively, and Figures 8(a) and 8(b) show that the system with PS-PWM and RL-load produces lower current THD than the system with LS-PWM, 2.79% and 4.04% respectively. Where R=10 Ω and L=1 mH.

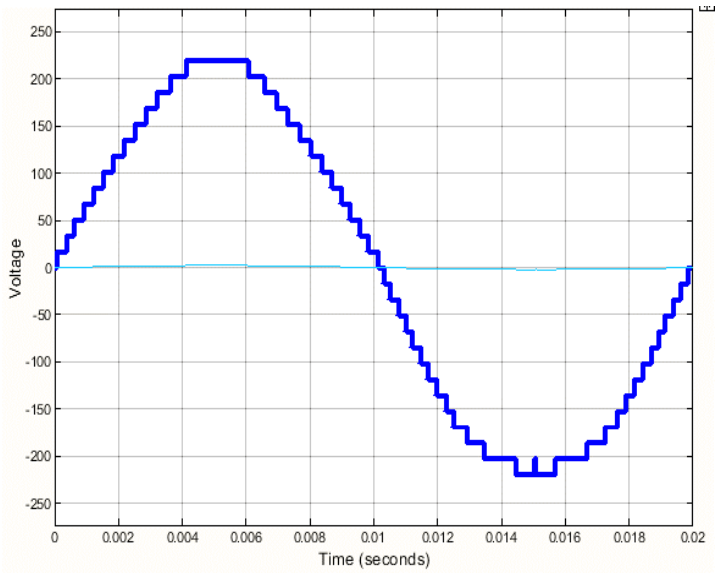
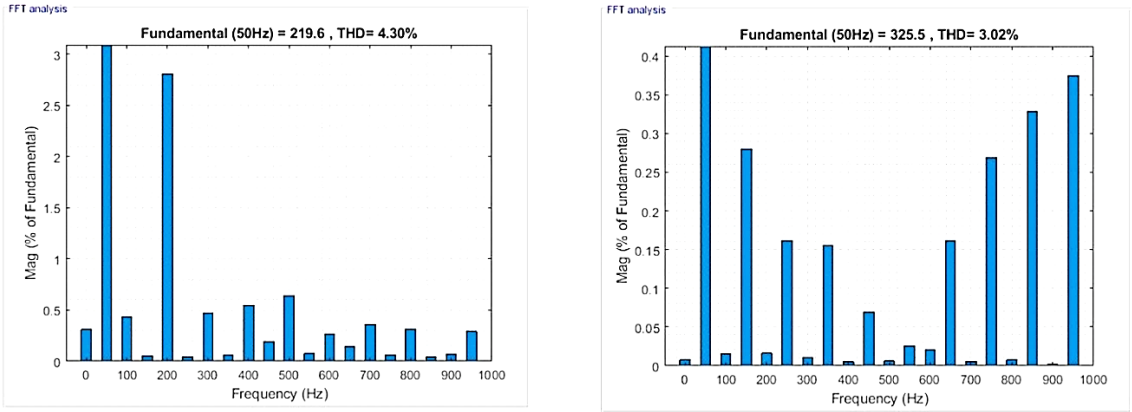
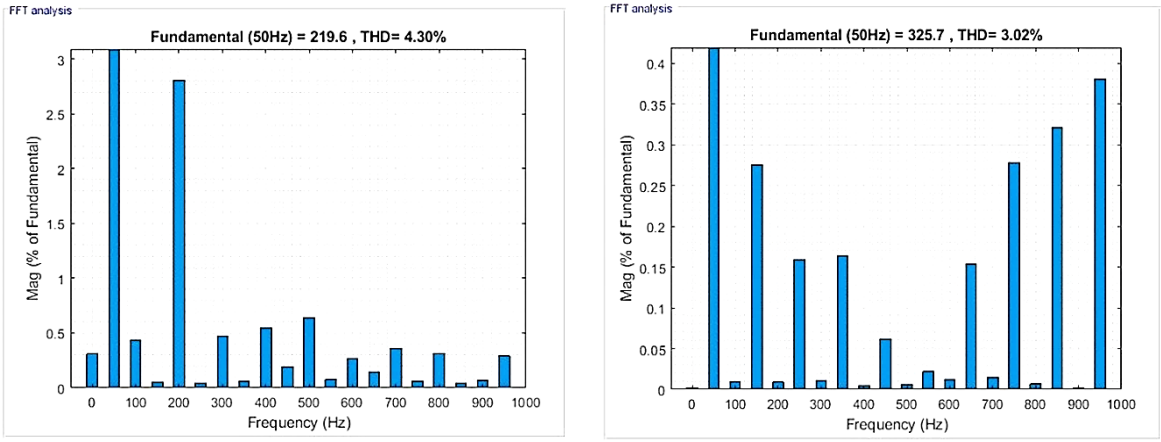


Figure 4. Output MI voltage



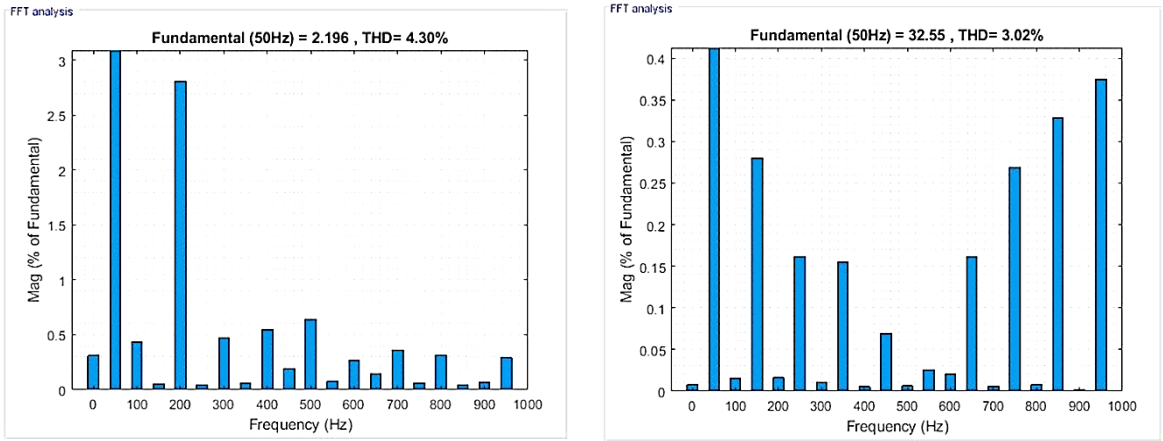
(a) (b)

Figure 5. THD of voltage for 27_level single phase inverter with resistive load, (a) with LS-PWM and (b) with PS-PWM



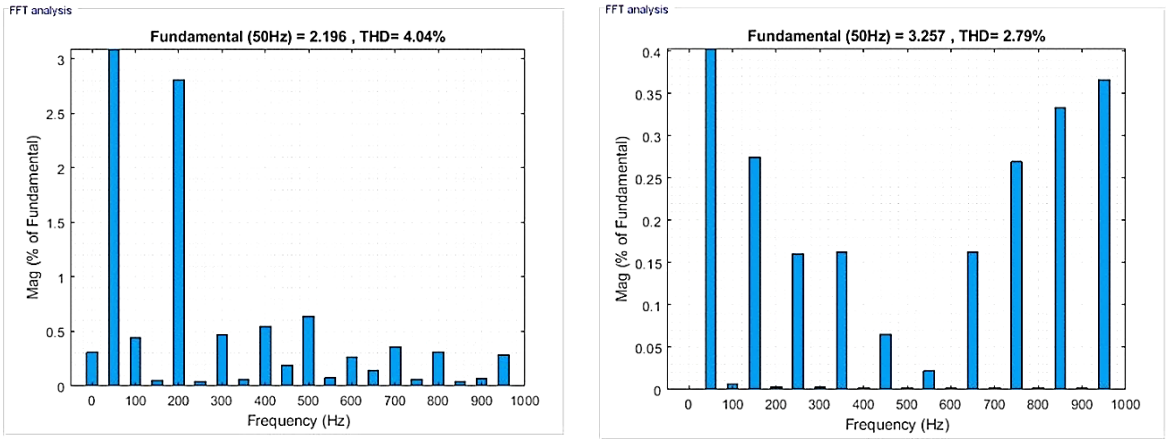
(a) (b)

Figure 6. THD of voltage for 27_level single phase inverter with inductive load, (a) with LS-PWM and (b) with PS-PWM



(a) (b)

Figure 7. THD of current for 27_level single phase inverter with resistive load, (a) with LS-PWM and (b) with PS-PWM



(a) (b)

Figure 8. THD of current for 27_level single phase inverter with inductive load, (a) with LS-PWM and (b) with PS-PWM

5. CONCLUSION

This study proposes an MLI with three H-bridge asymmetric DC sources. The main point of the proposed inverter is to show the comparison between LS-SPWM and PS-SPWM control techniques to get a multilevel inverter with fewer switching components and low total harmonic distortion (THD). The circuit was tested at both resistive and inductive loads, and the results of this investigation reveal that the total harmonic distortion (THD) of the voltage decreased by 1.28% where the loads were either inductive or resistive. THD of the current with resistive and inductive loads decreased by 1.28% and 1.25%, respectively.

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