

A novel multilevel inverter with reduced components and minimized voltage unbalance

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ABSTRACT

Multilevel inverters are an emerging area of research in the field of power electronic circuits and applications. It has many advantages like near-sinusoidal output voltage, lower total harmonic distortion (THD), reduced dv/dt stress, lower peak inverse voltage (PIV) and so on. But there are some associated problems as well such as cost, size complexity, and capacitor unbalance voltage. Here a novel nine level inverter topology has been proposed which addresses the issue of high no of switching and capacitor voltage unbalance. The proposed system has numerous advantages. The cost, size and complexity are reduced and the voltage unbalance problem is solved. The voltage stress across the switches is also reduced. The power loss distribution among the switches is optimum. So, the efficiency of the system is improved. Hence the overall system performance is improved. The system performs well for varying load like resistive, inductive as well as motor load. The stator voltage speed control of a single-phase induction motor has also successfully been achieved. The pulse width modulation PWM technique has been used for producing the switching pulses. The complete simulation analysis of these systems has been realized using MATLAB software. A comparative analysis of this system with the recently proposed systems has been done which shows significant advantages in all the above mention areas.

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1. INTRODUCTION

Recently, multilevel inverters (MLIs) have received much attention. They have many attractive features like near-sinusoidal staircase output voltage waveforms, higher efficiency, lower total harmonic distortion THD, reduced dv/dt stresses across switches, and lower peak inverse voltage (PIV) [1]. They are broadly used for industrial applications such as motor drivers [2]–[3], micro grid applications [4]–[6], and renewable energy [7]–[9]. Conventional MLIs are mainly classified into three types, namely neutral-point-clamped (NPC) [10], [11], flying capacitor [12], [13] and the cascaded H-Bridge (CHB) [14], [15]. To produce a greater number of output levels, NPC requires a greater number of power switches and clamp diodes. In addition, the problem of unbalanced voltage is also in a capacitor [16]. Similarly, flying capacitor type MI needs a large no of capacitors to produce a large number of output voltage levels. It will increase the overall cost. Furthermore, in low-frequency applications high value capacitors are needed. In this case NPC is better than FC [17]. Cascaded H-Bridge (CHB) MLIs does not require a clamping diode and also have low voltage stress unlike NPC and FC type MLIs. An inherent self-voltage balancing capability MLI has been proposed in [18], each capacitor voltage can be automatically balanced without using any additional balance

circuits or auxiliary circuits. FC and NPC can be derived from this new topology MLI, but it requires more power devices and causes limitations. In [19] and [20], the cascaded H-Bridge (CHB) MLIs have been proposed with reduced components. But the problem is that many independent dc sources are required for each H-Bridge in cascaded units.

To create more output voltage levels and reduced THD, a conventional series hybrid MLI has been proposed in [21]–[25]. An active neutral point clamped (ANPC) hybrid inverter has been proposed in [21], this system consists of a combination of FC and NPC to provide combined benefits i.e., flexibility of FC and NPC's robustness. A selective harmonic elimination strategy has been proposed in [23]–[25] to provide a self-balancing of capacitor voltage without additional circuits and reduced voltage stress of the switches. But, the disadvantage of the system is making a complex circuit with large components.

In [26], [27], three 9-level inverters have been proposed by utilizing switch capacitor (SC) networks. The systems of [26] are simple but the capacitors have been always used in series connection to divide the input voltage. Due to that the output currents are not the same in the positive half cycle and the negative half cycle. Due to this unbalanced voltage appears across the capacitors. The unbalanced voltage problem has been resolved in [27], but a large no of power switches have been required. The proposed 9-level inverter system in [27] is divided into two-stages. Increased power loss in each stage causes decrease efficiency of these systems.

With the benefits of SC methods, the numbers of 7-level multilevel inverters have been proposed in [28]–[30]. Especially, in [28] only one capacitor is used. Due to which no voltage balancing problem is there, but two different value DC voltage sources are needed. The systems proposed in [29] and [30] are obtained by three H-bridges connected in cascaded connection with two switches, both switches are bidirectional. They have the benefits of cascaded H-Bridge (CHB) but sixteen switches are needed. The power loss distribution increased with bidirectional switches causes minimized efficiency and increases the system's cost. The switched-capacitor (SC) systems [31]–[34] a step-up series-based inverter (MLIs) system is presented. It can be utilized as a high frequency (HF) power source. But it requires a large no of components and sources for generating the higher level.

Considering the abovementioned challenges, new SC-based 9 level inverters have been proposed. This consists of nine switches, two capacitors, two power diodes, and only one DC voltage source. Compared with the existing systems, the new proposed multilevel inverter has generated a greater number of output voltage levels with lesser components. It also minimized the voltage stress across the switches and reduced the THD of output voltage. The main advantage is that the capacitor has an inherent self-voltage balancing capability without using external circuits. It has also simplified the modulation algorithm. The operating principle and circuit configuration are mentioned in section 2. The parameters determination and modulation method are mentioned in section 3. The simulation results and the comparisons with existing typical multilevel inverter (MLIs) have been shown in section 4. Lastly, section 5 concludes the paper.

2. PROPOSED NINE-LEVEL CIRCUIT

2.1. Circuit configuration

The configuration of the proposed nine-level PWM inverter has shown in Figure 1. It consists of auxiliary and the main circuit. The main circuit is a single H-Bridge circuit with four power switches. It is help change in output voltage polarity. The auxiliary circuit is made of a special combination of switching devices with five power switches, two diodes, two capacitors, and one voltage source. It is responsible for synthesizing the output voltage waveform to produce the nine-level staircase output voltage. For the dc source V_{dc} , it can generate the output levels $0, \pm V_{dc}/2, \pm V_{dc}, \pm 3V_{dc}/2, \pm 2V_{dc}$.

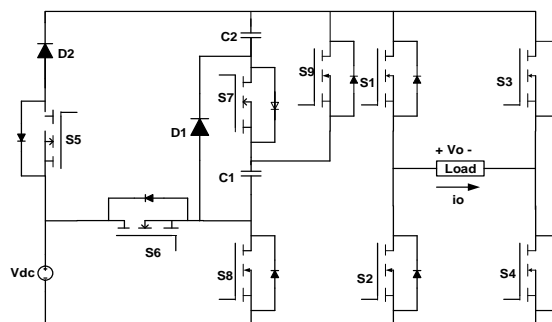


Figure 1. The proposed nine-level multilevel inverter circuit configuration

2.2. Operation cycles

In Figures 2-10, a conductive path loop has been shown by green and blue colors. Assumptions have been considered to make the easy analysis: i) parasitic parameters are not considered and ii) the capacitors and the switches are to be considered ideal components. Switching states has been shown in Table 1.

Here, in the states of the switches and the capacitors (C1, C2), “I” represents switches being turned on, “O” represents switches being turned off, “D” represents capacitors being discharged, “C” represents capacitors being charged, and “-” represents capacitors being uncharged.

- Level 0: Figure 2 shows a state that can produce a 0 level. The switches S2, S4 being turned on and the other switches being turned off.
- Level $V_{dc}/2$: Figure 3 shows a state that can produce a $V_{dc}/2$ Level. The switches S1, S4, S8, and S9 are being turned on. Capacitor C1 and C2 being discharges to the load with two paths. Capacitor C1 being discharges through S1, S4, S8, S9 and capacitor C2 discharges through D1, S1, S4, S8.
- Level V_{dc} : Figure 4 shows a state that can produce a (V_{dc}) level. The switches S1, S4, S5 being are turned on. V_{dc} being discharges to the load through S1, S4, S5, and D2.
- Level $3V_{dc}/2$: Figure 5 shows a state that can produce a $3V_{dc}/2$ Level. The switches S1, S4, S6, S9 are being turned on. Capacitors C1 and C2 being discharges with two-paths and capacitor C1 in series with V_{dc} being discharges to the load through S1, S4, S6, S9 capacitor C2 in series with V_{dc} being discharges to the load through S1, S4, S6, D1.
- Level $2V_{dc}$: Figure 6 shows a state that can produce a $2V_{dc}$ Level. The switches S1, S4, S6, and S7 are being turned on. Capacitors C1, C2 in series with V_{dc} being discharges to the load through S1, S4, S6, and S7.
- Level $-V_{dc}/2$: Figure 7 shows a state that can produce a $-V_{dc}/2$ Level. The switches S2, S3, S8, and S9 are being turned on. Capacitors C1 and C2 being discharges to the load with two-paths, capacitor C1 being discharges through S2, S3, S8, S9; capacitor C2 being discharges through D1, S2, S3, S8.
- Level $-V_{dc}$: Figure 8 shows a state that can produce a $-V_{dc}$ Level. The switches S2, S3, S5 are being turned on and V_{dc} being discharges to the load through S2, S3, S5, and D2.
- Level $-3V_{dc}/2$: Figure 9 shows a state that can produce a $-3V_{dc}/2$ Level. The switches S2, S3, S6, and S9 are being turned on. Capacitor C1 and C2 being discharges with two-paths. Capacitor C1 in series with V_{dc} is discharges to the load through S2, S3, S6, S9 and capacitor C2 in series with dc source (V_{dc}) being discharges to the load through S2, S3, S6, D1.
- Level $-2V_{dc}$: Figure 10 shows a state that can produce a $-2V_{dc}$ Level. The switches S2, S3, S6, and S7 are being turned on and capacitors C1, C2 in series with V_{dc} being discharges to the load through S2, S3, S6, and S7.

Table 1. Switching states and capacitor states of the presented nine-level multilevel inverter

Levels	Switches in Main Circuits				Switches in Auxiliary Circuits					Capacitors	
	S1	S2	S3	S4	S5	S6	S7	S8	S9	C1	C2
$V_{dc}/2$	1	0	0	1	0	0	0	1	1	D	D
V_{dc}	1	0	0	1	1	0	0	0	0	C	C
$3V_{dc}/2$	1	0	0	1	0	1	0	0	1	D	D
$2V_{dc}$	1	0	0	1	0	1	1	0	0	D	D
0	0	1	0	1	0	0	0	0	0	-	-
$-2V_{dc}$	0	1	1	0	0	1	1	0	0	D	D
$-3V_{dc}/2$	0	1	1	0	0	1	0	0	1	D	D
$-V_{dc}$	0	1	1	0	1	0	0	0	0	C	C
$-V_{dc}/2$	0	1	1	0	0	0	0	1	1	D	D

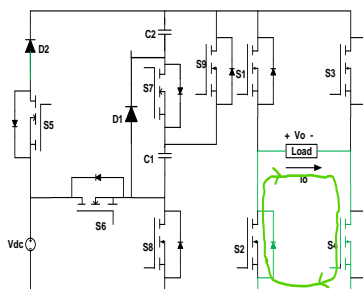


Figure 2. 0 level in forwarding current

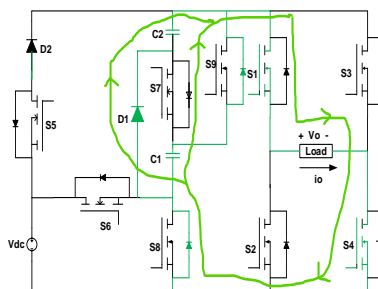


Figure 3. $V_{dc}/2$ level in forwarding current

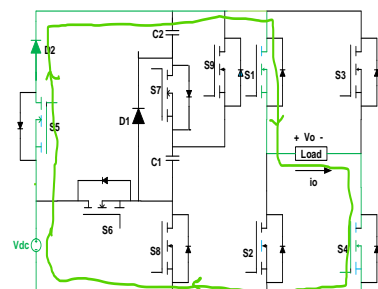


Figure 4. V_{dc} level in forwarding current

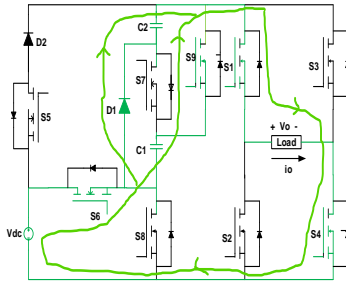


Figure 5. $3V_{dc}/2$ level in forwarding current

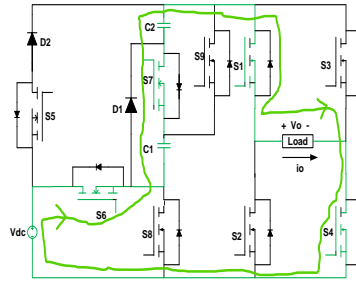


Figure 6. $2V_{dc}$ level in forwarding current

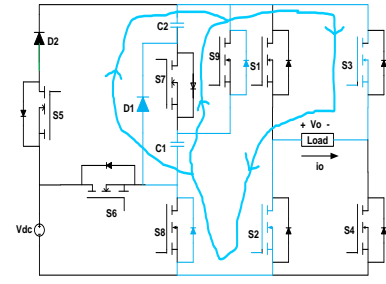


Figure 7. $-V_{dc}/2$ level in reverse current

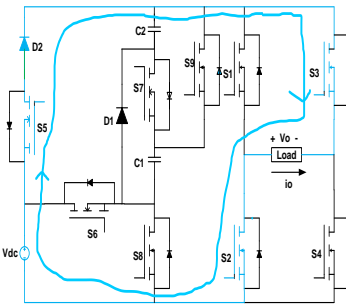


Figure 8. $-V_{dc}$ level in reverse current

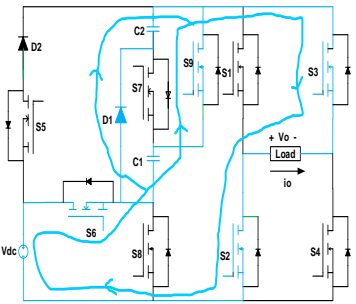


Figure 9. $-3V_{dc}/2$ level in reverse current

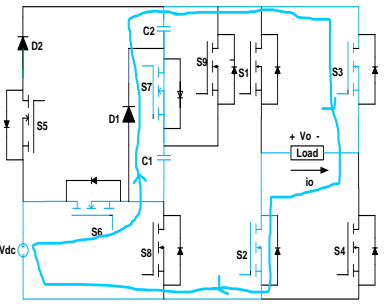


Figure 10. $-2V_{dc}$ level in reverse current

2.3. Modulation analysis

The proposed inverter system operational principle has been shown in Figure 11. The output voltage waveform (staircase structure) of the proposed system consists of four quasi square-waveforms v_{oj} ($j=1, 2, 3, 4$). Its magnitude is $\pm V_{dc}/2$ and conducting angle α_j . Here, the conducting angle must be satisfying the condition given as (1).

$$0 < \alpha_1 < \alpha_2 < \alpha_3 < \alpha_4 < \alpha_5 = 90^\circ \quad (1)$$

For all quasi (square) waveform, the Fourier series representation is (2).

$$v_{oj} = \frac{2V_{dc}}{\pi} \sum_{n=1,3,\dots}^{\infty} \frac{\cos n\alpha_j}{n} \times \sin n\omega t \quad (2)$$

Here, ω represent the angular frequency. Thus, the output voltage Fourier decomposition is (3).

$$v_{oj} = \frac{2V_{dc}}{\pi} \sum_{n=1,3,\dots}^{\infty} \sum_{j=1}^4 \frac{\cos n\alpha_j}{n} \times \sin n\omega t \quad (3)$$

The fundamental component of the output voltage waveform can be written as (4).

$$v_{oi} = \frac{2V_{dc}}{\pi} \sum_{j=1}^4 \cos \alpha_j \times \sin \omega t \quad (4)$$

Consider, the magnitude of modulation index is M_{oi} for the fundamental components. The total harmonic distortion (THD) can be calculated from as (6).

$$M_{oi} = \frac{1}{4} \sum_{j=1}^4 \cos \alpha_j \quad (5)$$

$$THD = \frac{\sqrt{\sum_{n=3,5,\dots}^{\infty} \left[\sum_{j=1}^4 \frac{\cos n\alpha_j}{n} \right]^2}}{\sum_{n=1}^4 \cos \alpha_n} \times 100\% \quad (6)$$

A selected harmonic elimination strategy has been used to modulate the presented proposed system. Here the 5th, 7th, and 11th components have been selected for harmonics elimination. Here the conducting angles α_j can be determined from [23]–[25],

$$\begin{aligned}
 \cos(\alpha_1) + \cos(\alpha_2) + \cos(\alpha_3) + \cos(\alpha_4) &= 4M_{oi} \\
 \cos(5\alpha_1) + \cos(5\alpha_2) + \cos(5\alpha_3) + \cos(5\alpha_4) &= 0 \\
 \cos(7\alpha_1) + \cos(7\alpha_2) + \cos(7\alpha_3) + \cos(7\alpha_4) &= 0 \\
 \cos(11\alpha_1) + \cos(11\alpha_2) + \cos(11\alpha_3) + \cos(11\alpha_4) &= 0
 \end{aligned} \tag{7}$$

When the magnitude of the modulation index M_{oi} is set to 0.8, then, from the above equation, the conducting angles α_j is calculated in (8).

$$\alpha_1 = 10.28^\circ, \alpha_2 = 21.16^\circ, \alpha_3 = 40.36^\circ, \alpha_4 = 61.06^\circ \tag{8}$$

From (6) and (8), the THD value of the presented nine-level multilevel inverter systems have been calculated theoretically as 3.12%.

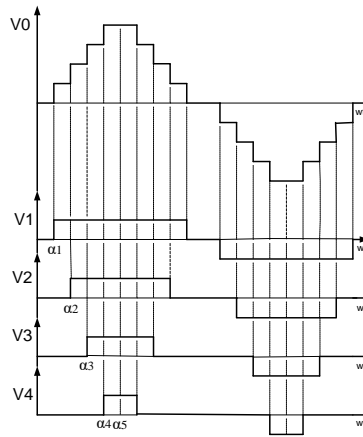


Figure 11. Proposed nine-level multilevel inverter operational principle

3. CAPACITOR CALCULATION AND LOSS ANALYSIS

3.1. Ripple loss analysis and capacitor calculation

The voltage ripple will appear across the capacitors. When the capacitor is discharged to the load, it should be limited to 10% of the self-maximum voltage of the capacitor. The capacitor voltage variations can be determined during the discharging period of capacitors. We can see Table 1 and Figure 11. The maximum continuous discharging period of the both capacitors are equal in the duration from α_3 to $\pi - \alpha_3$ in positive half cycle, when generating the output voltage levels $3V_{dc}/2$ and $2V_{dc}$, and similarly, the same discharging periods obtained in negative half cycle when producing output voltage levels $-3V_{dc}/2$ and $-2V_{dc}$. The current path relations have been shown in the above Figures 2-10. Now, the continuous discharging period of each capacitor in the interval α_3 to $\pi - \alpha_3$ as (9).

$$\Delta Q = \int_{\alpha_3}^{\alpha_4} \frac{i_o}{2w} dw + \int_{\alpha_4}^{\pi - \alpha_4} \frac{i_o}{2w} dw + \int_{\pi - \alpha_4}^{\pi - \alpha_3} \frac{i_o}{2w} dw \tag{9}$$

Here, the maximum voltage ripple for two capacitors and the largest discharging period is determined under pure resistive load condition. The staircase output voltage is generated in the simulation waveform. Thus, the capacitor's voltage ripple can be determined as (10).

$$\Delta V = \frac{V_{dc}}{4\pi f R_L C} (4\pi - 3\alpha_3 - 5\alpha_4) \tag{10}$$

Here, f is the output waveform frequency; C is the capacitance value of both capacitors and R_l is the output load resistance. Taking the acceptable voltage ripple into account, the minimum capacitance can be determined by (11).

$$C_{min} = \frac{V_{dc}}{4\pi f R_l C \Delta V} (4\pi - 3\alpha_3 - 5\alpha_4) \quad (11)$$

In Figures 12 and 13, the plot has been shown between the minimum capacitance vs. the output load and the minimum capacitance vs. the output frequency. Here to maintain the ripple voltage under an acceptable range, we found the capacitance value should be smaller with the increase the frequency and resistance. It verifies the higher frequency is capable of reducing the value of capacitance. Now, the ripple loss can be determined by (12).

$$P_{ripple} = f C (\Delta V)^2 \quad (12)$$

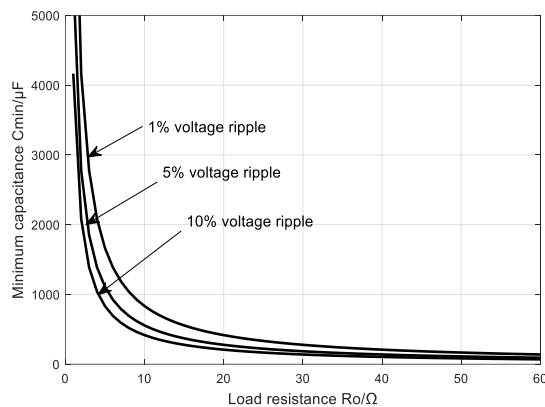


Figure 12. Capacitance vs load at 1 KHz frequency

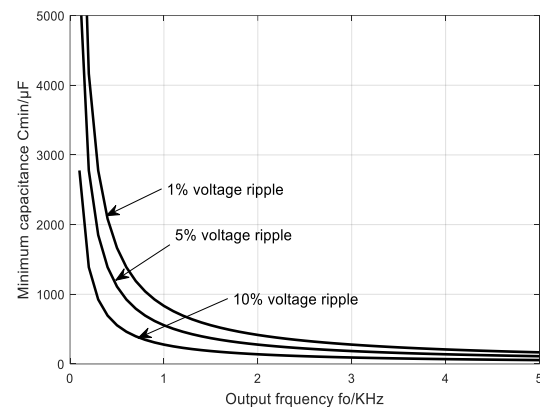


Figure 13. Capacitance vs frequency at 25-ohm load

3.2. Conduction loss

Determination of losses is a very important part of any system design. The three modes of operation such as conduction mode, blocking mode, and switching mode are performed undergoing multilevel inverter system operations. During blocking mode, the losses are considered to be almost negligible. Because there will be no current flow across the devices in this mode, the devices have to withstand the voltage stress on their terminals. Hence, the majority of the losses in the multilevel inverter (MLI) occur in switching and conduction mode. During Conduction mode, the amount of power loss occurs, when the device is in an “ON” state. The equivalent circuit parameters for different output levels have been shown in Figure 14 and Table 2.

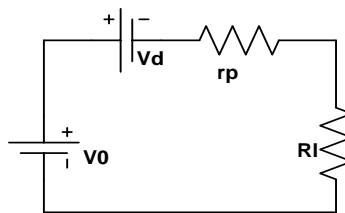


Figure 14. Equivalent circuit parameters

Table 2. Equivalent parasitic impedance for different output level

Output voltage level (V_o)	Equivalent parasitic impedance (r_p)	Eqv diode voltage (V_d)
0	$R_d + R_s$	V_1
$V_{dc}/2$	$\frac{3R_D + ESR_C}{2} + 2R_s$	$2V_1$
V_{dc}	$R_d + 3R_s$	V_1
$3V_{dc}/2$	$\frac{R_D + ESR_C}{2} + 3R_s$	V_1
$2V_{dc}$	$2ESRC + 4R_s$	0

Where V_o is the output voltage, V_d is the Equivalent voltage drop across the diodes, r_p is the eqv impedance, R_d is the diode internal resistance and body diodes internal resistance of the switches, R_s is the switches on-state resistance, V_1 is the diode voltage and body diodes voltage of the switches, and R_l is the output load resistance. The conduction loss can be determined by (13).

$$P_{conduction\ loss} = \frac{2}{\pi} \sum_{j=1}^4 \left[\left(\frac{V_o - V_d}{r_p + R_l} \right)^2 \times r_p \times (\alpha_{j+1} - \alpha_j) \right] \quad (13)$$

In (11) the capacitance value is inversely proportional to the equivalent series resistance of capacitor (ESR_c) of a capacitor. Increasing the capacitance value can not only reduce the ripple loss but also reduce the conduction loss by decreasing the parasitic equivalent series resistance of the capacitor (ESR).

3.3. Switching loss

Switching losses are caused by several switching transitions i.e., transition from one state to another state, in other words, the switching loss is defined as the overlaps of current and voltage during its state's changes, and it can be obtained during discharging and charging periods of the Parasitic capacitance between the source and the drains. It can be determined from as (14) [35].

$$P_{Switching\ loss} = f_s C_{DS} V_B^2 \quad (14)$$

The theoretical efficiency of the presented MLI can be determined as (15).

$$\mu = \frac{P_o}{P_{Conduction\ Loss} + P_{Switching\ Loss} + P_{ripple} + P_o} \quad (15)$$

Here, P_o is denoted rated output power.

4. SIMULATION RESULTS AND DISCUSSION

The simulation has been conducted by MATLAB software to verify the presented nine-level multilevel inverter system's performance. The parameters of the simulation waveform have been enlisted in Table 3. in this system 1 kHz output frequency has been considered, that is optimum frequency for high-frequency alternating currents (HFAC) for micro power grid system [4]–[6]. The driving signals simulation result of the H-Bridge circuit has been shown in Figure 15 for (a) switch S1, (b) switch S2, (c) switch S3 and (d) switch S4 and auxiliary circuits have been shown in Figure 16 for (a) switch S5, (b) switch S6, (c) switch S7, (d) switch S8 and (e) switch S9. For the simulation, the DC input voltage is considered as 50 volts.

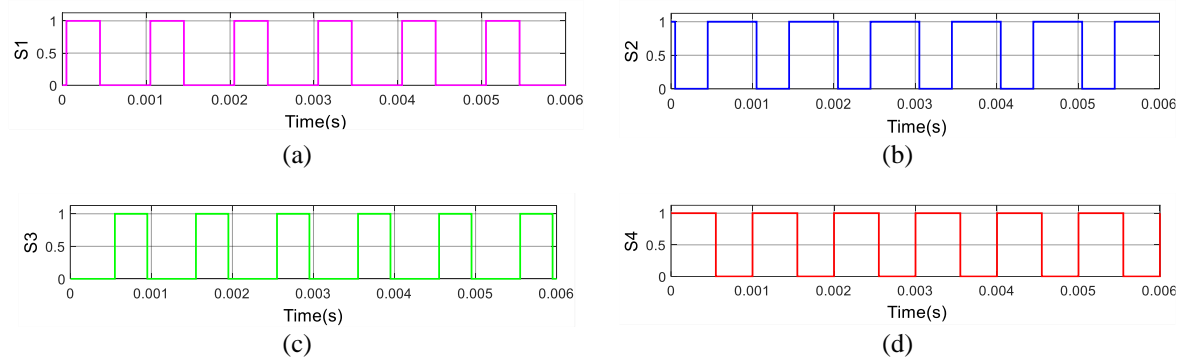


Figure 15. Driving signals simulation waveform of H-Bridge circuit for (a) switch S1, (b) switch S2, (c) switch S3, and (d) switch S4

Table 3. Presented nine-level multilevel inverter simulation parameters

Parameters	Value
Capacitance of capacitor	1000 μF
Switches on-state resistance	4.3 m Ω
Diodes forward voltage drop	0.3 V
Dc Source input	50 V
Output frequency	1 KHz
Load impedance	25 Ω

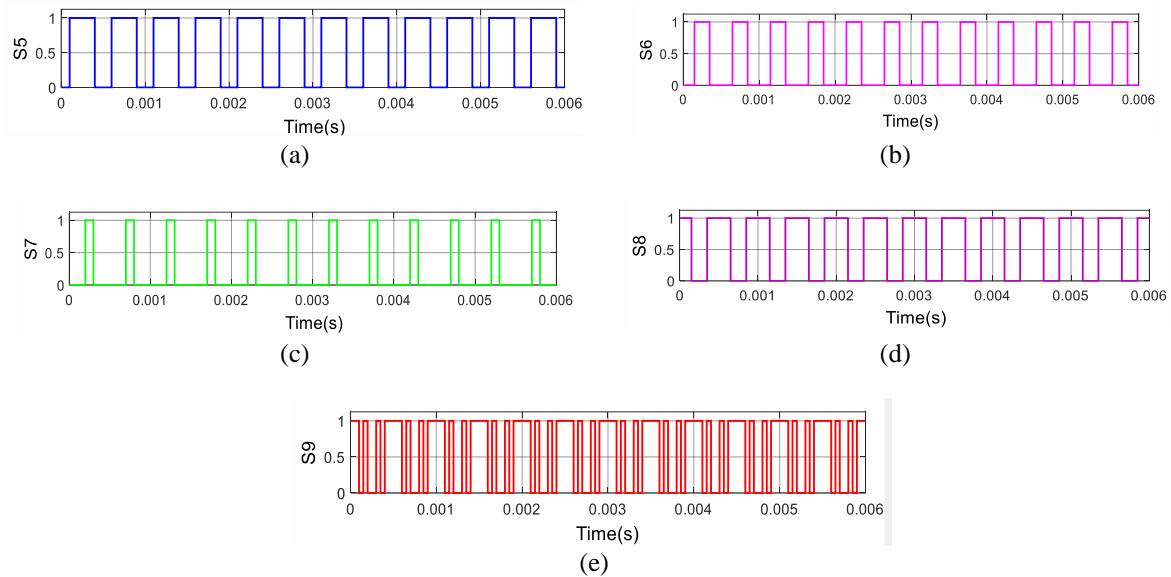


Figure 16. Driving signals simulation waveform of auxiliary circuit for (a) switch S5, (b) switch S6, (c) switch S7, (d) switch S8, and (e) switch S9

4.1. Simulation results of nine-level multilevel inverter with resistive load

The simulation results of the output voltage, voltage across the switch capacitors (C1, C2) and the load currents has been shown in Figure 17 for (a) output voltage, (b) voltage across capacitor switch C1, (c) voltage across capacitor C2 and (d) output current with 50V DC input voltage, obtained 100V peak value of output voltage, which verifies twice voltage gain of the presented topology when supplying a purely resistive load of 25 ohms. It has also verified output voltage and current are in the same phase due to the pure resistive load 25 Ω and their RMS values are calculated as 86.23 V and 3.4492 A, respectively. The capacitor is charged up to 25V volt for boosting the input voltage, which is verified in Figure 17. The voltage step is 25V volts for nine-level output.

4.2. Simulation results of nine-level multilevel inverter with R-L load

Similarly, the simulation waveform has been done for different types of loads. Here, the RL load has been connected in series, whose value is $R_o = 25 \Omega$, $L_o = 3.18$ milli henry, $Z_L = 25 + j20 \Omega$ ($R_o = 25 \Omega$, $L_o = 3.18$ milli henry, $|Z_L| = 32.01 \Omega$, $\phi = 38.67^\circ$). The simulation waveform has been scoped and it has been shown in the above Figure 18 for (a) output voltage, (b) voltage across capacitor switch C1, (c) voltage across capacitor C2 and (d) output current. Here due to the inductive load, it verified the current is lagging to the voltage by a phase angle of 38.67° , the phase angle represents the inductive load impedance angle. The capacitors' voltage simulation waveform has been shown in Figure 17 and Figure 18. The voltage across the capacitor C1 and capacitor C2 remain at 25V which confirms that almost constant voltage is obtained irrespective of the load. The advantage is avoiding the voltage unbalance problem, as a result of the inherent capability of the self-balance Voltage without using any external circuits. The THD value for the proposed systems is also very low theoretically calculated (around 3.12%).

4.3. Simulation results of nine-level multilevel inverter with single phase induction motor as load

The capacitor-start-run single phase induction motor is used as a load in nine-level multilevel inverter to verify the performance characteristics of the motor for this system. The stator voltage speed control of a single-phase induction motor is successfully achieved. Here the speed characteristic of motor has been verified with simulation results at no load, half load and full load with different input voltage. Here the motor is operating at 50HZ frequency and number of poles used 4. The no load speed should be 1500 RPM theoretically. It has been verified by simulation and it has been shown in Figures 19, 20, and 21. And the parameter has been shown in Tables 4, 5, 6, 7. Here the proposed system has been working well for induction motor as load. The main winding current and auxiliary winding current of the motor have been shown in Figures 22 and 23. It has been also verified the phase difference obtained approximate 90 degree between winding. So, the overall performance of the proposed system is good.

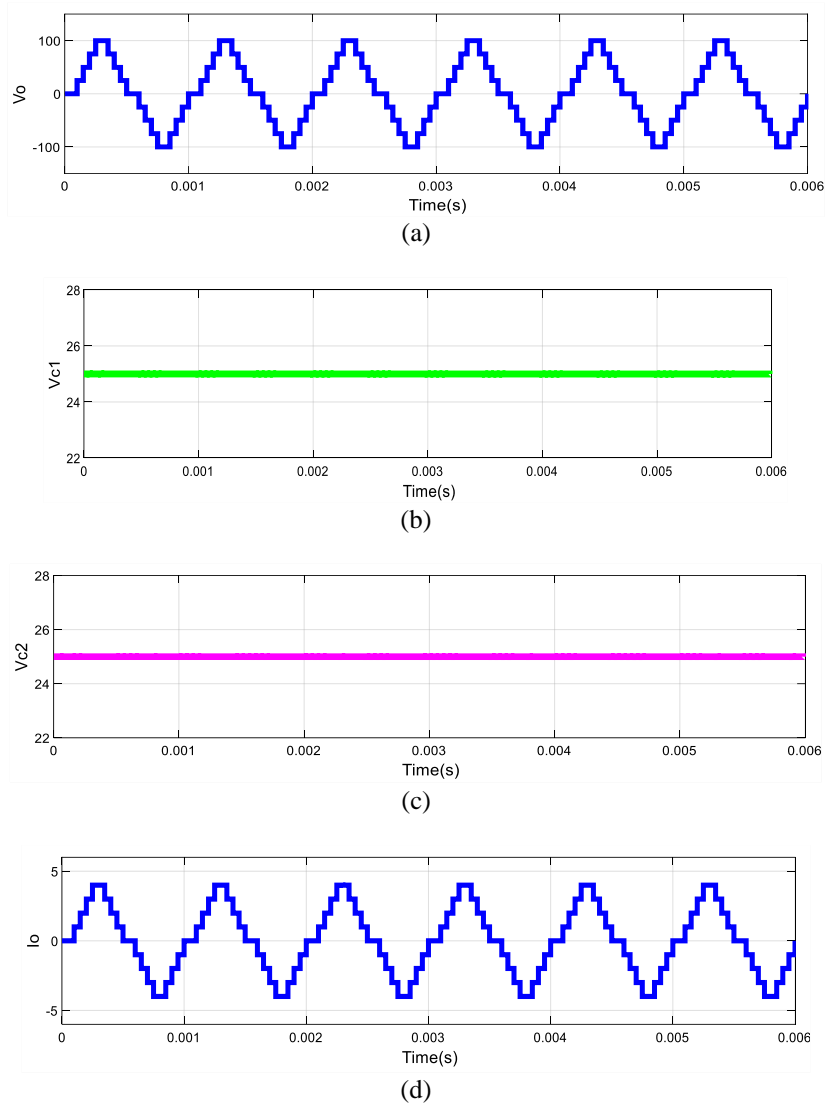


Figure 17. Simulation results of (a) output voltage V_o , (b) capacitor voltage V_{c1} , (c) capacitor voltage V_{c2} , and (d) output current I_o , with resistive load

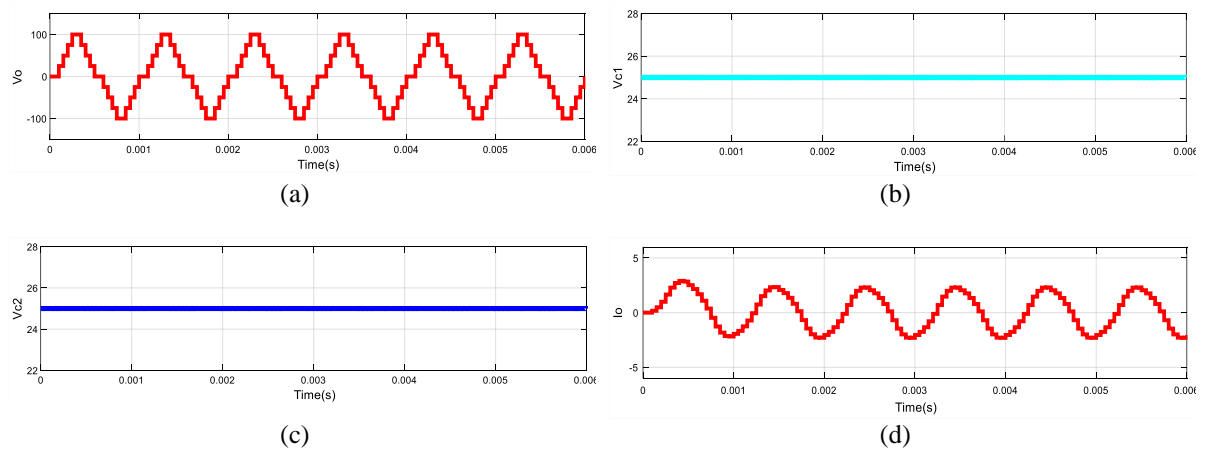


Figure 18. Simulation results of (a) output voltage V_o , (b) capacitor voltage V_{c1} , (c) capacitor voltage V_{c2} , and (d) output current I_o , with resistive-inductive load

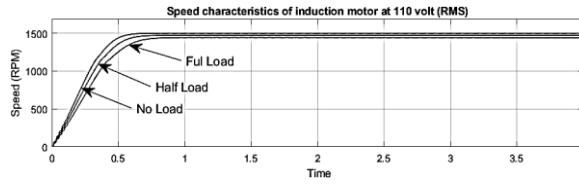


Figure 19. characteristics of motor speed at 110 volts (rms) input

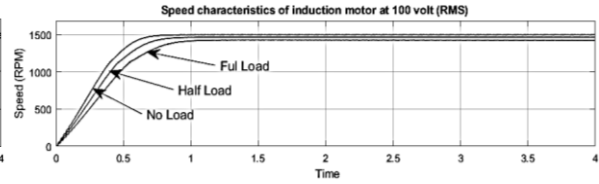


Figure 20. characteristics of motor speed at 100 volts (rms) input

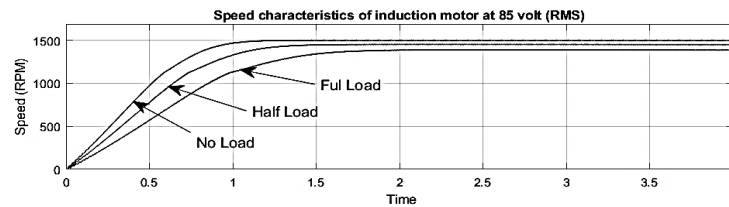


Figure 21. characteristics of motor speed at 85 volts (rms) input

Table 4. Load speed characteristic parameters of motor at 110 volt (rms) input

Motor input voltage (RMS)	Load	Speed (RPM)
110 V	No load	1500
	Half load	1478
	Full load	1451

Table 5. Load speed characteristic parameters of motor at 100 volt (rms) input

Motor input voltage (RMS)	Load	Speed (RPM)
100 V	No load	1499
	Half load	1464
	Full load	1390

Table 6. Load speed characteristic parameters of motor at 110 volt (rms) input

Motor input voltage (RMS)	Load	Speed (RPM)
85 V	No load	1480
	Half load	1341
	Full load	1189

Table 7. Induction motor parameters

Parameters	Value
Frequency	f(HZ) 50
Number of Pole	P 4

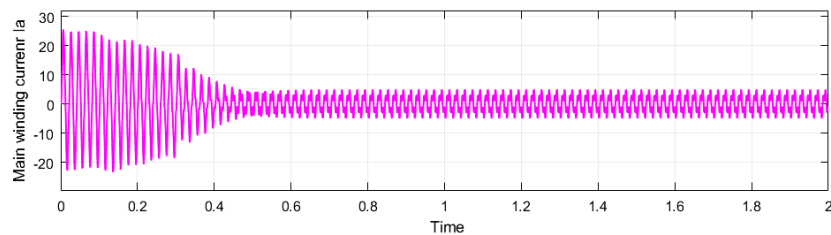


Figure 22. Induction motor main winding current simulation waveform

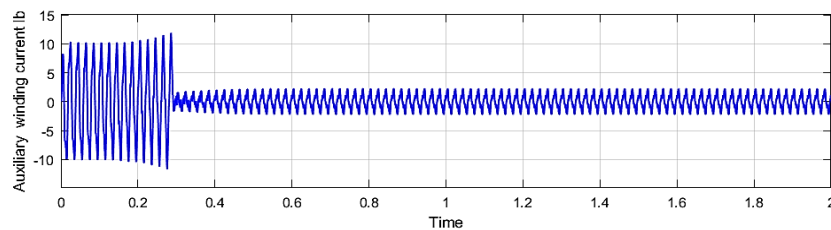


Figure 23. Induction motor auxiliary winding current simulation waveform

4.4. Comparisons the proposed multilevel inverter with the existing topologies

In this section, a proposed system and the switch capacitor multilevel inverters in [31]–[34] are compared where all output nine levels. The comparisons have been done in terms of the number of levels, number of switches, number of capacitors, number of diodes, and voltage stresses. The Table 8 shows the switching frequency and maximum blocking voltage across each switch. Where, C_{DS} , f_s , F_o and V_B are the capacitance (between drain and source), the switching frequency, output frequency and the switches maximum blocking voltage, respectively.

Table 8. Switches operational parameters in detailed

Parameters	Switches in Main Circuits		Switches in Auxiliary Circuits			
	S1-S4	S5	S6	S7	S8	S9
f_s	F_o	$2 F_o$	$2 F_o$	$2 F_o$	$2 F_o$	$6 F_o$
V_b	$2V_{dc}$	$V_{dc}/2$	V_{dc}	$V_{dc}/2$	V_{dc}	$V_{dc}/2$

Table 9 gives the comparison of the all-existing systems and the proposed systems with single input DC source. In this proposed MLI, only nine switches are used to regulate the output voltage. This system comprises a single voltage source, two power diodes, two capacitors, lesser power switches and reduces voltage stress across switches. The proposed topology has been compared with the existing topology [31]–[34]. The existing topology generates nine-level output with a larger number of components, as the result increases the complexity and cost of the systems. The proposed topology has been compared in Figure 24. with the existing topology [31]–[34] in terms of maximum voltage stress across switches and total number of switches.

Here, Capacitor, Source, Switch, and Diode represents: the numbers of total capacitor, number of total voltage source, and number of total power Switches and number of total diodes used. Furthermore, the compressions have also been done in consideration of efficiency. The efficiency has been calculated theoretically with 400 W and 3000 W output power. It shows the optimum power loss distribution among the switches with minimized components. Power loss distribution has been shown in Table 10. The efficiency has been calculated as 95.52% for 500 W output power and 97.85% for 3000 output power. The proposed system has higher efficiency in comparison with the existing topology in [31] and [32]. In this proposed system, the voltage that appears across the capacitor is almost constant, and as a result, circumvents the voltage unbalance problem and the main advantage of the system is reduced voltage stress. Hence, the proposed system is the inherent capability of the self-balance Voltage without using any external complex circuits. So, the system is fully capable of meeting the needs of industrial applications. In Table 10 the P_{sw} , P_c , C_1 , C_2 denotes the switching loss, conduction loss, ripple loss due to capacitors respectively.

Table 9. Comparisons of the presented system with the existing systems in [31–34]

Parameters	Proposed Topology	[31]	[32]	[33]	[34]
Capacitor	2	3	3	3	2
Source	1	1	1	1	1
Switch	9	10	11	12	11
Diode	2	0	0	0	0
Peak Inverse Voltage	$2V_{dc}$	$4V_{dc}$	$2V_{dc}$	$4V_{dc}$	V_{dc}

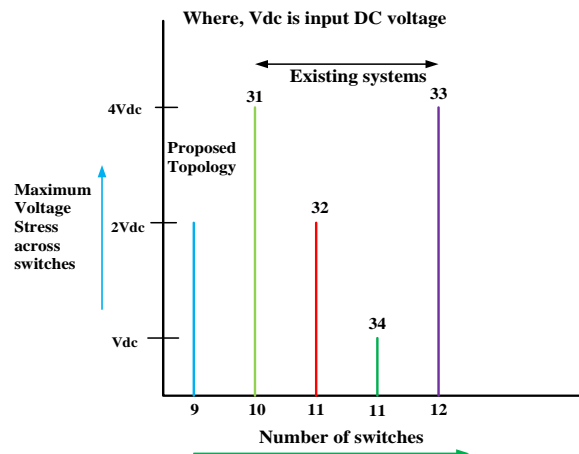


Figure 24. Comparisons of the presented system with the existing systems in [31]–[34] with figure

Table 10. Loss calculation for the proposed system

Output Power (W)	Power Losses	S1	S2	S3	S4	S5	S6	S7	S8	S9	Total Losses	η (%)
400	P_{sw}	0.02	0.026	0.026	0.026	0.013	0.02	0.013	0.02	0.04	0.243	95.52
	P_c	1.85	1.85	1.85	1.85	1.92	1.98	1.92	1.92	2.5	17.64	
	C_1	0.125									125	
	C_2	0.125									125	
	P_{sw}	0.06	0.067	0.067	0.067	0.034	0.05	0.034	0.05	0.10	0.536	
3000	P_c	6.25	6.25	6.25	6.25	6.966	6.95	6.97	6.95	9.5	62.33	97.85
	C_1	0.8									0.8	
	C_2	0.8									0.8	

5. CONCLUSION

A novel nine level inverter topology has been proposed in this paper, which is based on the novel switching strategy. The proposed topology has been optimized in this paper for utilizing a minimum number of switches, diodes, capacitors and voltage sources. A comparative analysis of this system with the recently proposed systems has been done. It generates nine-level output with a lesser number of components, inherent capability of the self-balance Voltage without using any external circuits, the advantage is avoiding the voltage unbalance problem, as the result decreased the complexity and cost of the system. It can also simplify the algorithms or modulation circuits. The total harmonic distortion (THD) value has been obtained at a theoretical very low 3.12%. It also shows the optimum power loss distribution among the switches. Due to this, efficiency of this system is improved. All the feasibility and merits of the proposed system are analyzed by a simulation model with varying load like resistive, inductive as well as motor.




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