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Capacitor voltages balancing method for buck modular DC/DC converter

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ABSTRACT

The most critical problem of the modular DC-DC converter (MDCC) is the voltage balancing of the submodule (SM) capacitors, the MDCC with stepped 2-level modulation has been developed and presents a good solution, however, this type of modulation has many restrictions when there is a wide range of capacitance tolerance of the SM capacitors that results inaccurate capacitor voltages balancing. To solve this problem, this paper discusses a proposed method of capacitor voltage balancing. Compared with stepped 2-level modulation, the voltage balancing method using modified duty cycle modulation offers the merits: i) reduction in output voltage and SM capacitor voltages overshoot during dynamic operation and improvement in the time response of the system and; ii) accurate voltage balancing over wide range of capacitance tolerance of each SM capacitor; and iii) the sorting algorithm replaced with modified duty cycle modulation method for the SM capacitor voltages balancing which reduces the computation burden. The proposed method ensures a stable voltage balancing, improves the time response of the system, and decreases the voltage and current overshoot during the dynamic response compared with prior art of MDCCs, where the stepped 2-level modulation is adopted. An analytical simulation of the MDCC is presented using MATLAB/Simulink to explain the operation.

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1. INTRODUCTION

Recently, high-voltage direct current (HVDC) technology became the preferred transmission and distribution solution for wide-range renewable energy over a long distances due to its advantages, such as relatively small loss, high system modularity, perfect harmonic characteristics and high reliability [1]–[4]. HVDC requires DC/DC converters (buck and boost) developed for medium or high voltages ranges to interconnect electrical transmission systems with multiple voltage levels. Practically the voltage levels of HVDC systems are much more than the voltage ratings of available electronic switches. To solve this problem, a cascaded switches can be consider as suitable solution, but it leads to relatively complex gate driver and additional snubber circuits. Classical multilevel converters like flying capacitor and diode clamped are not appropriate solution, because the circuit layout becomes more difficult as the number of levels is increased [5].

Modular multilevel converter (MMC) that constructed from half or full bridge submodule (HBSM or FBSM) has been considered a suitable solution in medium and high voltages applications [6] for its favorable features of scalability and high modularity [7]–[11]. Isolated modular DC/DC converter (IMMDC) have been discussed in [12]–[14], in (IMMDC) two MMCs ac terminals are connected via a transformer to achieve DC/DC conversion, operation methods and strategies for high efficiency of (IMMDC) have been developed in

[15]–[19]. Despite the fact that (IMMDC) benefits the MMC topology, but using two AC/DC conversion stages results to relatively high losses. In addition, extra cost and the footprint of the ac coupling transformer rated for the full load transmission power is significant. Non-isolated modular multilevel DC/DC converter (MMDC) with single stage derived from MMC phase leg that proposed in [20], [21] has the advantages of low cost, high efficiency and small volume. This type of converters is preferable solution when galvanic isolation does not present a stringent requirement and the compact design of the converter presents relatively high priority.

The most serious problem of the MMC is the voltage balancing of SM capacitors due to the lower and upper arms absorb different amount of power from the dc-sources. Different methods for capacitor voltages balancing have been developed such as switching-cycle capacitor voltage control (SCCVC) that balance the capacitor voltages at each switching cycle [22]–[24], self-voltage balancing and soft switching [25] and 2-level modulation [26]; 2-level modulation method have a simple controlling strategy, but all SMs are inserted or bypassed simultaneously, the voltage of SM capacitors become unbalanced due to capacitance differences among the SM capacitors, in addition a high voltage stress applied on the IGBTs of the SM. To overcome these disadvantages, a steeped 2-level modulation method has been developed [27], instead of inserting or bypassing all the SMs in the same time, sorting algorithm used to insert or bypass each SM at a time according to controlling technique takes into consideration the capacitor voltage and current direction in each arm, practically SM capacitors have not equal capacitance due to tolerance percentage, using fixed step time between each insert or bypass process despite the voltage difference among the SM capacitors leads to inaccurate voltage balancing over wide range of capacitance tolerance.

This paper presents a proposed control method depending on applying modified duty cycle, each SM inserted or bypassed for a specific time proportion to the difference between the average arm voltage and each individual capacitor voltage using proportional controller, i.e., if a SM in a chain link has lower capacitance value than other SMs, as result this SM will has a greater voltage and imbalance capacitor voltages between SMs will occurs, this is where the proposed control technique to reduce the duty cycle applied to that SM, which results in a reduction in the SM capacitor voltage, and vice versa when that SM has greater capacitance value, that accomplishing capacitor voltages balance. The rest of paper is arranged as: section 2 explains the topology, operation principles and analysis of buck MDCC, section 3 illustrates the closed loop control strategy for the buck MDCC and the MATLAB simulation of the MDCC, section 4 shows the MATLAB simulation results for both steady state operation and dynamic response, and section 5 summarizes the conclusion.

2. BUCK MODULAR DC/DC CONVERTER

2.1. Topology of buck MDCC

Figure 1 illustrates the main circuit configuration of the buck MDCC [27] which can be obtained by replacing the electronic switches (MOSFETs and Diodes) of conventional buck converter by two chains of cascaded SMs (chain link 1 and chain link 2) and an arm-inductor L_a, both chain link 1 and chain link 2 are formed by N of series-connected half-bridge SMs (HBSMs), this converter designed to interconnect two different levels of HVDC where $V_{dc1} > V_{dc2}$. Figure 2 shows the structure of the SM [27].

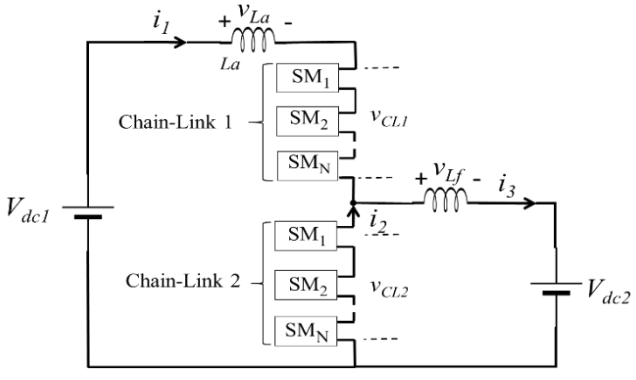


Figure 1. Main circuit of the buck MDCC [27]

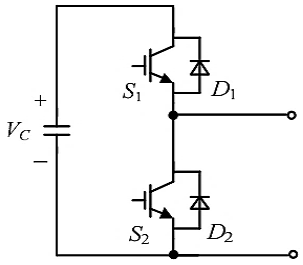


Figure 2. Circuit diagram of SM [27]

2.2. Operation principle of buck MDCC

Two operational states are defined for each chain link in order to clarify the buck MDCC's operation principles: the high level state (HLS), which occurs when all SMs are inserted and the output voltage is N Vc,

and the low level state (LLS), which occurs when all SMs are bypassed and the output voltage is equal to zero.

$$V_{dc1} = NV_C \quad (1)$$

Both chain links 1 and 2 operate in pulse width modulation (PWM) mode, the waveforms have a period T, and the duty cycle of v_{Cl1} is (*1-d*), while v_{Cl2} has a duty cycle equal to *d* as shown in Figure 3 [27]. To achieve SM capacitor voltage balance, an alternating current (AC) circulating current must be generated directly between chain links 1 and 2 [28], to generate this circulating current a shifted phase should be existed between v_{Cl1} and v_{Cl2} as presented in Figure 3 and the phase shifted duty ratio is d_s. According to Figure 3, steady state operation has four switching states:

- During [0, d_sT]: both chain link 1 and chain link 2 operate in *LLS*, V_{La} and V_{Lf} represent the voltages across L_a and L_f respectively, $V_{La}(t) = V_{dc1}$ and $V_{Lf}(t) = -V_{dc2}$, i_1 increases linearly and i_3 decreases linearly.
- During [d_sT, dT]: chain link 1 operates in LLS, while chain link 2 operates in *HLS*, $V_{La}(t) = 0$ and $V_{Lf}(t) = V_{dc1} - V_{dc2}$, i_1 remains constant and i_3 increases linearly.
- During [dT, $(d + d_s)T$]: both chain link 1 and chain link 2 operate in *HLS*, $V_{La}(t) = -V_{dc1}$ and $V_{Lf}(t) = V_{dc1} - V_{dc2}$ respectively, i_1 decreases linearly and i_3 increases linearly.
- During [$(d + d_s)T$, T]: chain link 1 operates in HLS, while chain link 2 work in *LLS*, $V_{La}(t) = 0$ and $V_{Lf}(t) = -V_{dc2}$ respectively, i_1 remains constant and i_3 decreases linearly.

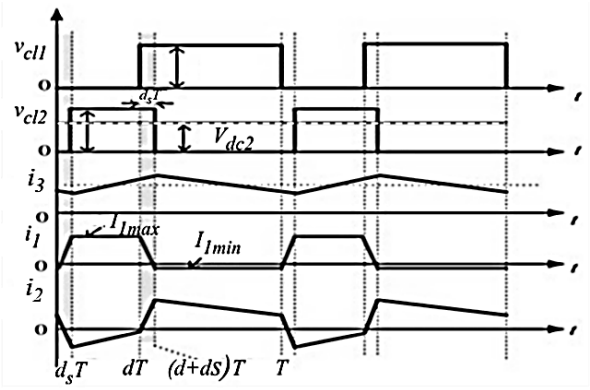


Figure 3. Basic waveforms of buck MDCC [27]

2.3. Steady state operation and analysis

According to You and Cai [29], the voltage-second balance of filter inductor L_f can be achieved, it easy to get.

$$V_{dc2}(1-d)T = (V_{dc1} - V_{dc2})\,dT \quad (2)$$

Manipulating (2) yields,

$$d = D = \frac{V_{dc2}}{V_{dc1}} \quad (3)$$

D represents the steady state of *d*. As shown in Figure 3, i_1 has trapezoidal waveform with maximum and minimum values I_{1max} and I_{1min} respectively, the relationship between I_{1min} and I_{1max} is:

$$I_{1min} = I_{1max} - \frac{V_{dc1}}{L_a} d_sT \quad (4)$$

If *P* is the transferred power of the converter, the average value of i_1 is:

$$\frac{1}{T}\int_0^T i_1(t)dt = I_{1max}D + I_{1min}(1-D) = \frac{P}{V_{dc2}} \quad (5)$$

Combining (4) and (5) I_{1max} and I_{1min} can be expressed as:

$$I_{1max} = \frac{P}{V_{dc1}} + \frac{V_{dc1}}{L_a}(1\text{-}D)d_sT \quad (6)$$

$$I_{1min} = \frac{P}{V_{dc1}} - \frac{V_{dc1}}{L_a}Dd_sT \quad (7)$$

Returning to Figure 3, according to the waveforms of i_1 and v_{Cl1}, chain link *1* absorb energy W_{Cl1} in one period, and can be calculated as shown [29]:

$$W_{Cl1} = \int_0^T v_{Cl1}(t)\, i_1(t)\, dt = \frac{I_{1max} + I_{1min}}{2} V_{dc1}\, d_sT + I_{1min} V_{dc1}(1\text{-}D\text{-}d_s) \quad (8)$$

Substituting both (6) and (7) into (8) gives:

$$W_{Cl1} = P(1\text{-}D)\,T + \frac{V_{dc1}^2 T^2}{L_a}\left[\frac{1}{2} d_s^2 - (1-D)\,Dd_s\right] \quad (9)$$

While chain link 2 absorb energy W_{Cl2} in a one period, and can be calculated as shown,

$$W_{Cl2} = \int_0^T v_{Cl2}(t)\,[-i_3(t)]dt = -P(1\text{-}D)\,T - \frac{V_{dc1}^2 T^2}{L_a}\left[\frac{1}{2} d_s^2 - (1-D)\,Dd_s\right] \quad (10)$$

The major condition to achieve SM capacitors voltage balance is the total energy absorbed by both chain link *1* and chain link *2* in one period must be equal to zero, i.e.

$$W_{Cl1} = W_{Cl2} = 0 \quad (11)$$

Combining (9), (10) and (11) gives D_s [29] which represents the steady state value of d_s

$$D_s = (1\text{-}D)\,D - \sqrt{(1-D)^2\, D^2 - 2P(1-D)La/(V_{dc1}^2\, T)} \quad (12)$$

3. CLOSED LOOP CONTROL STRATEGY OF BUCK MDCC

3.1. Feedback control of the output voltage

Recalling (3), buck MDCC has a voltage ratio that of conventional buck converter. That means the same control strategy can be applied for booth converters. In this paper, the conventional output voltage feedback control is used. As shown in Figure 4(a), the output voltage V_{dc2} compared with reference voltage V_{ref}. The produced error signal is applied to proportion-integral (PI) controller to generate duty cycle signal *d*.

3.2. Phase-shifted control

($\overline{v_{cl1}}$) is the average value of SM capacitor voltages of chain link *1*, and ($\overline{v_{cl2}}$) is the average value of SM capacitor voltages of chain link *2*, which can be fine balanced by adjusting the value of d_s. The difference between $\overline{v_{cl1}}$ and $\overline{v_{cl2}}$ in Figure 4(b) represents the error signal applied to low pass filter (*LPF)* to reduce any fluctuation. The output signal of the filter is applied to *PI* controller to generate d_s signal.

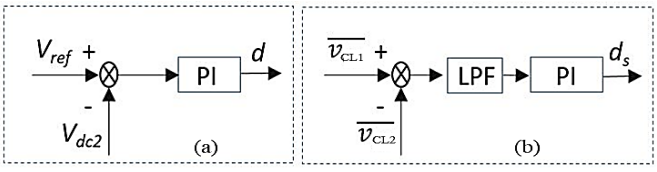


Figure 4. Closed loop scheme for (a) voltage feedback control and (b) phase-shifted control

3.3. Proposed modulation method for voltage balance of SM capacitors

Recalling (1), it is clear that the capacitor voltage of each SM is equal to V_{dc1} divided by the number of SMs in each chain link, theoretically all capacitors have the same value of capacitance, and the duty cycle

applied across all SMs in the same chain link, that leads all capacitors will charge to the same voltage, and capacitor voltage balancing will be achieved without any additional control.

$$\Delta vc = \frac{i\,dT}{C} \tag{13}$$

Referring to the above equation, capacitor voltage directly proportions to charging time and inversely proportion to the capacitance value of the capacitor. Practically, there is a percentage error in capacitance values in manufactured capacitors, if 2-level modulation method is adopted [27], i.e. the same duty cycle applied across all SMs in the same chain link and the same current follows through all SMs since cascaded connection adopted, that leads to charge each capacitor to a different voltage level and imbalance capacitor voltages will occur. Using fixed time step during inserting or bypassing SM capacitors can be suitable solution and accurate voltage control strategy when the difference between capacitance values of SM capacitors is quite small. To solve the problem of capacitor voltages balancing for a wide range of capacitance difference and develop a reliable control strategy a modified duty cycle modulation is developed, this method can be easily explained by applying a duty cycle for each SM proportion directly to capacitance value of that SM, suppose that the *nth* SM capacitor in a chain link 1, has a large capacitance value than others, according to (13) the voltage across that capacitor will be smaller than other capacitor voltages in the that chain link.

To solve this problem, an extra control plan is proposed and will be explained briefly, referring to Figure 5(a), the generated duty cycle signal d in the voltage feedback control part will be modified by comparing both the *nth* SM capacitor voltage (v_{cn}) and the average voltage of capacitor voltages in that chain link 1($\overline{v_{cl1}}$), the error signal applied to proportion (P) controller, the output signal is subtract from the original duty cycle signal d the result are $d_{11} - d_{1n}$ control signals of chain link 1, and vice versa when the SM capacitor have capacitance value smaller than others, according to (13) the voltage across this capacitor will be larger than other capacitor voltages in the same chain link, the output of P controller add to the original duty cycle signal, the same control strategy applied to the capacitors in chain link 2 to generate the control signals of chain link 2 d_{21}- d_{2n} as shown in Figure 5(b), these control signals used to drive the SMs in chain link 1 and 2 as shown in Figures 6(a) and 6(b).

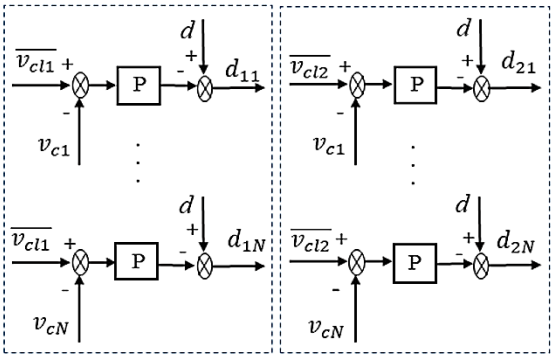


Figure 5. General Scheme for modified duty cycle control for (a) chain link 1, and (b) chain link 2

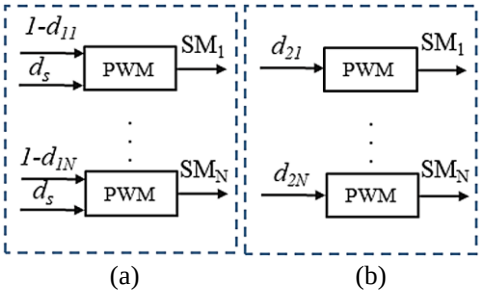


Figure 6. Drive signals of SMs for (a) chain link 1 and (b) chain link 2

3.4. MATLAB simulation

The circuit of the buck MDCC in Figure 1 has been simulated using MATLAB/Simulink R2017B as shown in Figure 7 to interconnect HV side (V_{dc1}) to LV side (V_{dc2}) which represented by a constant load. The simulation model of the control circuit that drives SM_1 at chain link 1 shown in Figure 8(a), an other control circuits with same design used to compare the average voltage of chain link 1 ($\overline{v_{c1}}$) with $v_{c2,}$ v_{c3} and v_{c4} in order to drive SM_2, SM_3 and SM_4 respectively. While The control circuit that drives SM_5 at chain link 2 shown in Figure 8(b), an other control circuits with same design used to compare the average voltage of chain link 2 ($\overline{v_{c2}}$) with $v_{c6,}$ v_{c7} and v_{c8} in order to drive SM_6, SM_7 and SM_8 respectively.

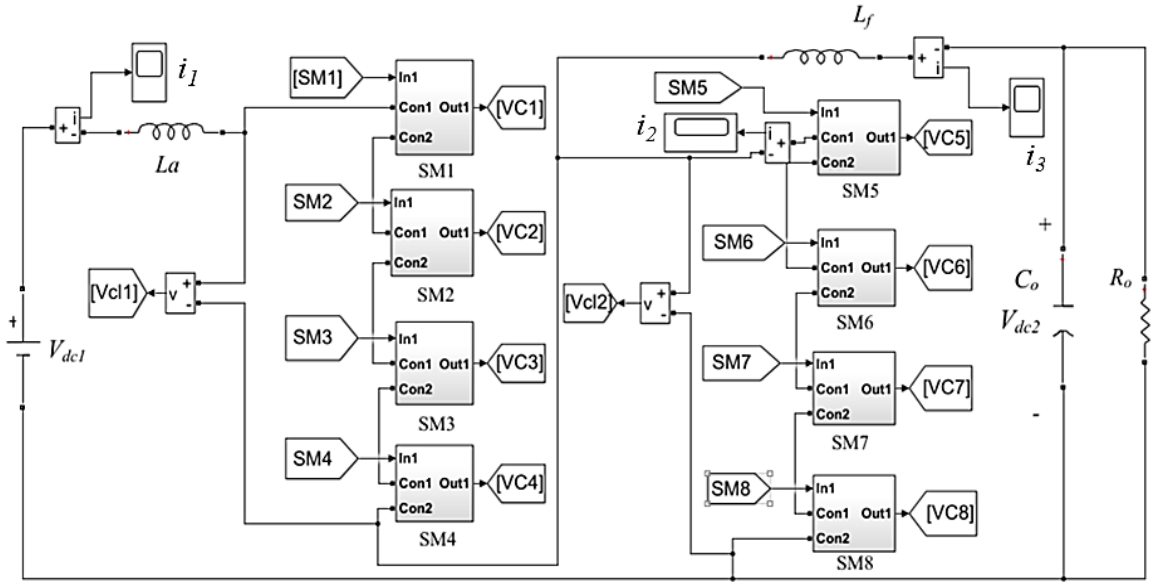
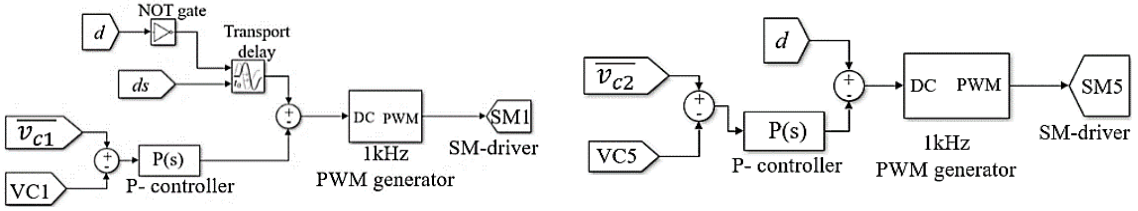


Figure 7. MATLAB simulation model of the buck-MDCC



(a) (b)

Figure 8. MATLAB simulation model of the control circuit for (a) SM_1 in chain link 1 and (b) SM_5 in chain link 2

4. MATLAB SIMULATION RESULTS

The circuit parameters of the simulation model were listed in Table 1 [27] using four SMs in each chain link . To verify the effectiveness of using modified duty cycle modulation in buck MDCC in ensuring an accurate voltage balancing even if there is a wide range of tolerance of capacitance value for SM capacitors, SM capacitors values were chosen with tolerance within ∓40% instead of using fixed capacitor value of 200 µF as in stepped 2-level modulation method, for both chain links; *C1*,*C2*,*C3* and *C4* are 150, 250, 350 and 450 µF respectively.

4.1. Steady state results

Figure 9 demonstrates the waveforms of buck MDCC at steady state operation using modified duty cycle modulation method, the output voltage was regulated to 2 kV. The dotted box shows how the duty cycle of each SM is modified according to the capacitance value of the SM capacitors, that leads to adjust chain link 1 capacitor voltages (v_{c1}-v_{c4}) and chain link 2 capacitor voltages (v_{c5}-v_{c8}) to 2 kV with voltage ripple

within 0.5%. the waveforms show the ripple of i_3, while maximum and minimum values of i_1 and i_2 can be noticed where the minimum value of i_2 is close to zero. Compared with stepped 2-level modulation method, the waveforms show the using of fixed stepped time (5 μs) during the voltage rising period of v_{cl1} and v_{cl2} regardless of the capacitance value of the SM capacitors, that causes a higher SM capacitor voltages ripple which is about 3% [27].

Table 1. Circuit parameters [27]

Parameter		Value
Rated power	P	800 KW
Input voltage	V_{dc1}	8 kV
Output voltage	V_{dc2}	2 kV
Switching frequency	f	1 kHz
Arm inductor	L_a	1 mH
Filter inductor	L_f	20 mH
Capacitance Filter	C_f	2 mF
SM capacitance	C_{sm}	200 μF ∓40%
SM capacitor voltage	V_c	2 kV
Number of SMs per chain link	N	4
Stepped time during transition period	T_d	5 μs

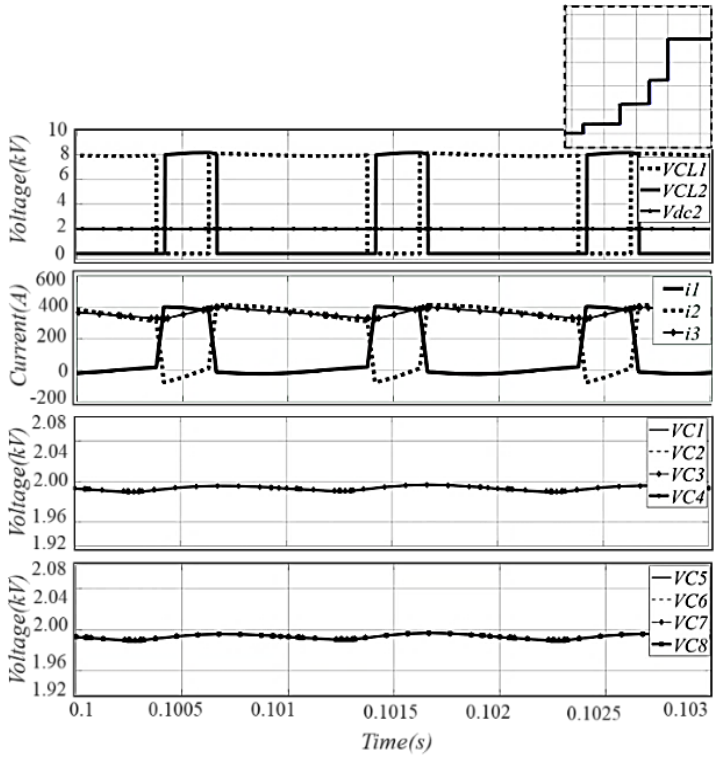


Figure 9. Steady state waveforms using modified duty cycle modulation method

4.2. Dynamic response

The dynamic response using modified duty cycle modulation method is shown in Figure 10, a step change of the load is considered, initially the load is set to 400 kW, then the load stepped to 800 kW, the output voltage (V_{dc2}) and the voltage of SM capacitors reach the steady state in less than 50 msec, and the overshoot of output voltage (V_{dc2}) and SM capacitor voltages are 4% and 3% repetitively. On the other hand, the output voltage (V_{dc2}) and the voltage of SM capacitors reach the steady state within 0.1 sec, and the overshoot of output voltage (V_{dc2}) and SM capacitor voltages are 8% and 6% repetitively when the stepped 2-level modulation method was used [27].

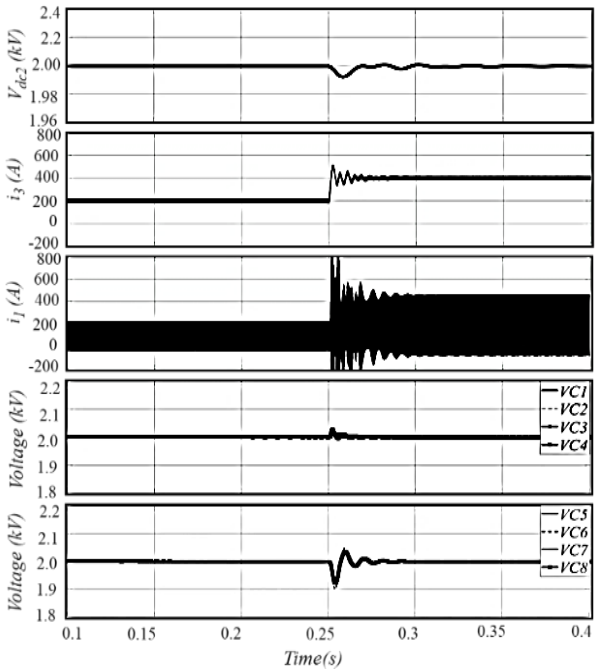


Figure 10. Dynamic response waveforms using modified duty cycle modulation method

5. CONCLUSION

In this paper, modified duty cycle modulation method for buck MDCC has been proposed to achieve SM capacitor voltages balancing. Compared with prior art of MDCCs, where the stepped 2-level modulation is adopted, the proposed method ensures a stable voltage balancing even if there is a wide range of tolerance of capacitance value for SM capacitors, reduces the overshoot of the output voltage and the SM capacitor voltages during the dynamic response, improves the time response of the system, and decreases the computation burden by replacing the sorting algorithm with simple modulation method.

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