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A comprehensive study of grid impedance and its reliability effects on variable frequency drive

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ABSTRACT

Grid impedance is one of the most important parameters for the satisfactory operation of variable frequency drive (VFD) and their interaction with other utilities connected to the same grid. In this research investigation a new approach to analytical evaluation and verification of grid impedance, and short circuit current is discussed. VFD under identical operating and loading conditions is connected to different grid capacities and configurations, being considered in this investigation. Grid impedance variation in terms of measured or estimated values, due to different grid connectivity affects the commutation of uncontrolled front-end rectifiers. This impacts the nonlinearity of input current wave shape, causing a significant change in current harmonics (THDi) and ripple current of DC link. This paper comprehensively investigates the reduction of DC capacitor lifetime and losses of DC inductor, and diode with various grid capacity and configurations under standard load conditions. High-frequency harmonics impact (2-9 kHz) on DC inductor losses is also analyzed. A VFD of 250 kW is considered for entire practical measurement including distortion effects and MATLAB simulation. This research may give a good insight into the sizing of VFD front-end devices. The reliability impact of VFD is also one of the important outcomes of this research.

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1. INTRODUCTION

With rapid technology advancement, VFD has become inevitable in numerous motor-driven applications. Motors in these applications are controlled through VFD, thereby offering substantial energy savings due to load characteristics. IEC 61000-3-2, IEEE 519 and IEC 61000-3-12 standards recommend limits of overall and individual current harmonics [1]–[3] versus grid short circuit ratio (Rsce). Voltage distortion is dependent on system impedance and influences system performance. Voltage distortion created by non-linear currents is seen reduced with lower values of system impedance (short circuit capacity increase). International standards and Grid codes recommend guidelines of grid impedance and short circuit current with reference to harmonic frequency and connected load capacity of VFD. A comprehensive analytical and practical measurement of grid impedance is of utmost importance to establish the reliability, design considerations, and sizing of VFD front-end components. Grid impedance variations impact VFD harmonic performance when connected to the grids of varying configurations. Grid impedance determination helps to identify resonance and stability conditions present in the grid supply [4]. Nonlinear loads have a

substantial impact on both supraharmonics (2 to 150 kHz) and low-frequency harmonics (up to 2 kHz) which significantly affects the power system [5]. This investigation gives much focus on the evaluation and measurement of short circuit current (I_{sc}), grid impedance (Z_{TH}), and grid capability to validate connected VFD harmonic performance. Several research papers are published on grid impedance: characterization [6], high-frequency analysis via current injection [7], monitoring [8], determination through PWM signals [9], results and performance analysis [10], review of impedance in microgrids with electronic gadgets [11], simulation investigation [12], the performance impact on connected modular inverter systems [13], grid impedance versus harmonic emissions impact of grid-connected inverters [14], investigation of input harmonic distortion due to variable frequency drives [15], analysis of measurement device and its system design [16], relevancy of grid integration on renewable energy systems [17], measurement [18] and impact [19] of harmonic impedance in the grid with electronic gadgets, and estimation methods [20]. However, most of the above research works limit the analysis on the reliability impact of connected non-linear loads like VFD. This research investigates grid impedance estimation, and measurement/verification method which adds significant value to power electronic converter manufacturers during product approvals and qualification process. The impact of grid impedance on VFD front-end devices from a design and reliability perspective is the significant outcome of this end-to-end investigation.

VFD front-end reliability due to the grid impedance changes when connected to different grid capacities and configuration is validated under identical loading conditions. Current distortion at VFD input (THD_i) varies due to changes in system impedance of different connected grid configurations.

This research is organized as per activities below:

- Grid impedance/short circuit current analytical estimation and practical measurement under various operating conditions, grid configurations (with VFD as connected load) are detailed.
- Nonlinear current behavior and distortion effects (external AC reactor and built-in DC inductor) under various operating conditions and grid configuration at VFD input have been detailed.
- Modelling, MATLAB simulation, and practical testing of VFD with various grid configurations and identical load conditions are detailed.
- DC capacitor reliability measured as a lifetime in hours is studied.
- DC Inductor losses and their impact with simulated current measurements are estimated including the high-frequency range of 2-9 kHz.
- Front-end rectifier diode losses estimation is analyzed.
- Harmonic distortion and relevant standards are analyzed.

A VFD of 250 kW is connected to different grid capacity/configurations that support verification and validation of this research study. Research outcome with analytical, practical testing, and simulation is inferred in the below sections. Recommendations of this investigation are part of the conclusion.

2. THE COMPREHENSIVE THEORETICAL BASIS

2.1. VFD and grid connectivity

VFD comprises major sections like front end rectifier, intermediate DC link circuit, output inverter, control, and regulation. In this research 250 kW VFD is connected to three test bays (A, B, and C) with six different grid capacity/configurations (grid 1-6) as in Figure 1. Grid HV source of 11 kV is made available to all three test systems which are stepped down to low voltage suitably through 2500 kVA, 1000 kVA, and 500 kVA transformers having automatic voltage tap facility. Test and load motors of 132 kW, 800 kW, and 400 kW connected in the regenerative mode of the load system. VFD is connected to the test motor in the system and loaded at 132 kW and 250 kW output capacity respectively. A standalone 12 pulse, 1 MVA transformer with star output was also interposed at the input of VFD in 800 kW and 400 kW test systems. Input harmonics, voltage, current, and DC link measurements were done using Tektronix DPO7054 oscilloscope and power quality recorder PQ-Box 200. A comprehensive study with a 250 kW VFD loaded in six different grid configurations was performed to analyze, and measure the grid impedance, and harmonic capability to fulfill requirements per IEEE 61000-3-2, IEEE 519, and IEC 61000-3-12 grid standard recommendations.

2.2. Grid impedance and prospective short circuit current

Grid impedance (Z_{TH}) is expressed simply as the ratio of source voltage (Vs) and short circuit current (I_{sc}). Prospective short circuit current (PSCC) is defined as the quantum of current which flows at a specific point on the grid system considering the situation of a real short circuit across phases with power still flowing. The quantum of current flow is limited by the power system impedance. PSCC level is specified in kilo amperes. SCCR refers to the amount of PSCC that VFD is rated to withstand.

PSCC has a significant thermal impact on the VFD input rectifier section and DC capacitor. The VFD input current increase is directly proportional to PSCC and can be limited by the available system impedance since input diodes start conducting only when the input voltage is higher than DC bus voltage. When a VFD is connected to a grid with higher PSCC than its rating, the life expectancy of front-end rectifier diodes and DC capacitors is significantly reduced. Figure 2 and Figure 3 show the impact of a 250 kW VFD input peak current when connected to a 5 kA and 100 kA (500 A and 1500 A) PSCC power system respectively. With higher PSCC, peak and RMS current of VFD input is increased significantly. VFDs are designed for a specified voltage range which is also its SCCR rating. VFD PSCC rating depends on the design of the power components and power section layout. Whenever PSCC at the point of VFD grid connectivity is higher than rated, an AC reactor or built-in DC choke is the preferred solution to reduce the high peak current as observed in Figure 3 to meet VFD SCCR requirements.

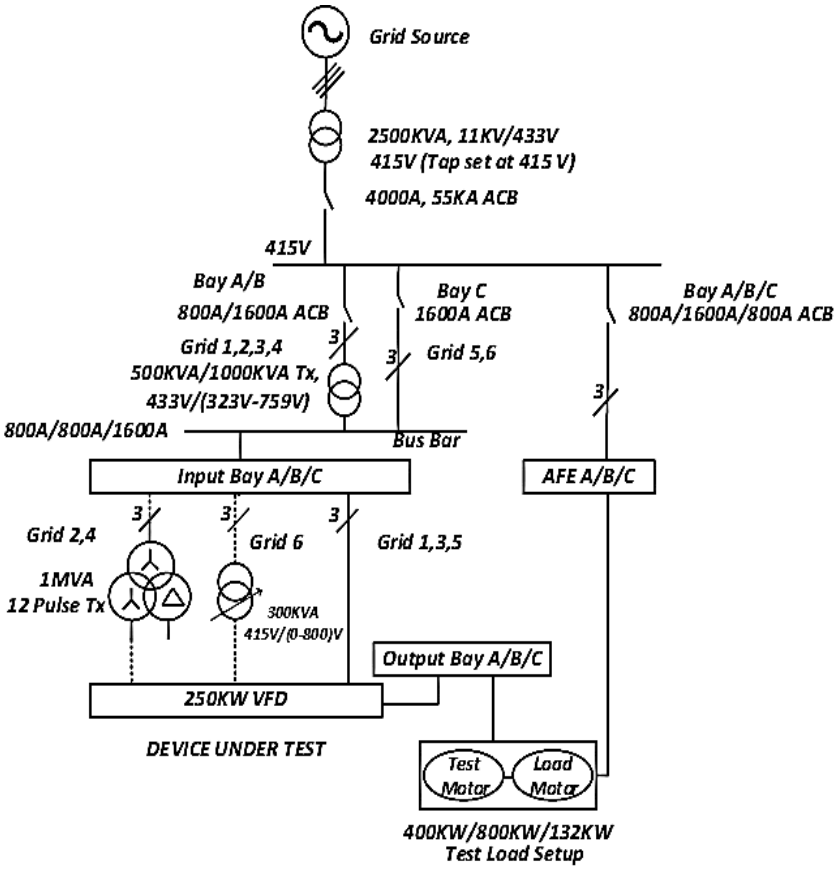

Figure 1. Single line diagram of 250 kW VFD in 400/800/132 kW test system (grid 1 to grid 6)

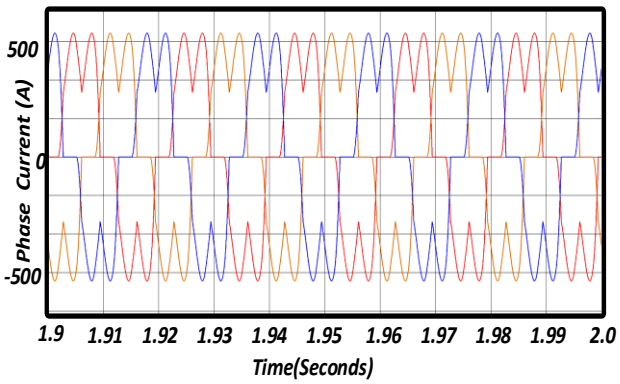

Figure 2. VFD input currents on 5 kA PSCC power system

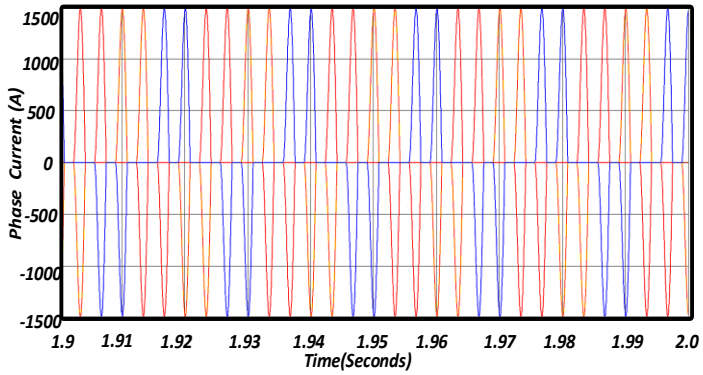

Figure 3. VFD input currents on 100 kA PSCC power system

2.3. Grid impedance and VFD front end rectifier

VFD Front end Rectifier topology is a three-phase diode bridge for smaller kW. For higher power size mixed diode- SCR rectifier in a three-phase bridge is used. The current rating of the diode rectifier is obtained from safe junction temperature determined under nominal and overload conditions. A preliminary study of the datasheet [21] and extraction of the main electrical and thermal parameters are done in order to estimate the power losses under different operating conditions. One way of parameter extraction is using linearization of electrical static characterization of diodes. Another common method of parameter extraction is curve fitting using exponential functions from the datasheet to determine output characteristics. Power loss calculation tools are provided by manufacturers and also developed using MATLAB, saber, and excel in certain cases. Power losses and junction temperatures are calculated at different operating points. With calculated power losses and the chosen reference heat sink temperature, the average diode junction temperature is estimated. The main input parameter used in loss calculations of rectifiers is DC link current both under nominal and overload conditions, from which the average and RMS diode current are calculated. Power losses determine the VFD efficiency and are used in thermal simulations. On the other hand, junction temperature estimation supports reliability and diode selection. A lower grid impedance and higher PSCC increase the peak and RMS current flowing through the diode rectifier. Peak current causes a substantial increase in junction temperature and diode stresses, which is represented as surge current capability in the datasheet (I_{FSM}). On the other hand, RMS or average current (I_{FAV}) increases diode losses. The short circuit capability (I^2t) of the fuse should be properly selected and sized lesser than the diode rectifier to ensure better protection during short circuits. Analytical evaluation of diode losses in VFD tested with different grid configurations/impedances discussed in detail further.

The forward characteristic curve of the combined thyristor/diode (IXYS MCD 501) is as per the datasheet of reference [21] considered in this investigation. From the evaluation using the best curve fitting function, the power dissipation/diode losses are given by (1).

$$P_{FAV} = V_{T0} * I_{FAV} + r_f * I^2{}_{FRMS} \quad (1)$$

Where, P_{FAV} is the power dissipation mean value, $I_{FAV,}$ and I_{FRMS} is the forward mean, and RMS current value, V_{T0} the threshold voltage, and r_f is the forward slope resistance required to determine diode power losses.

2.4. External AC reactor and built-in DC inductor

A 250 kW VFD used in this research investigation is suitably modeled with the equivalent circuit as in reference [22]. VFD front end mainly consists of rectifier bridge, DC inductor, and DC capacitor. DC inductor is by design in between the rectifier and a DC capacitor. DC inductor attenuates harmonic frequency components of lower frequency order. AC reactor is commonly used at the input when VFD is not designed with a built-in DC inductor. However, in certain applications, an AC reactor is also used along with a built-in DC inductor. AC reactor has better performance at higher frequency orders. AC reactor has a significant voltage drop across it during operation which reduces the torque output capability of VFD. AC reactor offers protection of rectifier bridge against mains transient. System reactance constitutes both impedance of the grid and the inductive reactance of the AC reactor. External AC reactor at VFD input or built-in DC inductor plays a significant role in harmonic mitigation and is sized accordingly. Analytical evaluation of grid impedance and its impact on rectifier current, harmonic current spectrum both due to AC reactor and DC link inductor is expressed by (5)-(12), (15)-(17) [22].

Input current distortion (THDi) and peak currents of the diode bridge are substantially increased which impacts DC inductor losses. The voltage drop across the DC inductor is mainly due to its inductance value and also the ripple current of the DC capacitor. DC inductor reduces current ripple due to line variations. VFD with input AC reactor addition results in an overlap of diode current between phases during the commutation process causing transient current peak and voltage notch. System reactance plays a significant role in current transients resulting in increased harmonics on the AC side and DC ripple [22].

3. METHOD

3.1. Analytical method of grid impedance estimation

Protection of electrical systems by design should be safe and selectively coordinated. Estimation of short circuit level supports the determination of interrupting rating specifications, selective coordination, and provision of component protection. The ideal procedure to determine fault current is to represent a single line diagram of the complete electrical system with all sources of short circuit current feed onto the fault in addition to the impedances of the circuit components. System components as part of the utility system are also represented as impedances in the single line diagram like transformers, bus ducts, and cables. Short circuit estimations of the system are done by elimination of current limiting devices, with assumption as copper bus bars, and thereby determine the maximum available short-circuit current with reasonable accuracy. The point-to-point calculation procedure for three-phase circuits, with step-by-step expressions, has already been explained in reference [23] to determine stage-wise short circuit fault and thereby grid impedance including the point of motor connectivity in the applicable power system. An uncontrolled six pulse VFD of 250 kW, 415 V, 420 A rating was tested in Bay A, B, and C under identical operating and load conditions. Analytical evaluation of short circuit fault currents at different downstream stages of test bays is represented in the single line diagram as in reference [24]. Short circuit current and grid impedance of test bays through analytical evaluation (without motor contribution) are consolidated in Table 1.

Table 1. Analytical evaluation of short circuit current and grid impedance of test bays

Operating conditions/grid configuration (at 415 V)	I_{sc} (kA) (VFD input)	Z_{TH} (VFD input)
Bay A/grid 1	4.9 kA	84.7 mΩ
Bay A (12 P)/grid 2	2.4 kA	173 mΩ
Bay B/grid 3	10.2 kA	40.7 mΩ
Bay B (12 P)/grid 4	4.0 kA	104 mΩ
Bay C (direct)/grid 5	14.0 kA	29.6 mΩ
Bay C (300 kVA)/grid 6	2.1 kA	197 mΩ

3.2. Practical measurement methodology of grid impedance

METREL 3144 Euro Z 800 V instrument was used for practical measurement of line/grid impedance (Z_{TH}). A Power system network has both resistive and inductive components involved. Hence impedance measurement (rather than only resistance) needs to be established. The high precision line impedance measurement is performed using high current impulses to ensure adequate voltage drop during the test. METREL 3144 [25] applies a very high loading current onto the power system network typically once per 15 seconds. The measurement principle of voltage or current measurement is through synchronous sampling. Line impedance is the impedance within the current loop when a short circuit occurs (or 3 phase system, between two-line conductors). During the measurement, an internal resistance is connected between C1 and C2 for a period of a half-cycle as load. The instrument's internal shunt resistor measures the current (I_{test}). Voltmeter (across P1 and P2) measures the open circuit voltage with no load ($U_{UNLOADED}$), followed by the second reading with a load (U_{LOADED}) as in reference [25]. The impedance Z_{TH} is determined from the difference of voltage during load and unloaded conditions to the current ratio (I_{test}) as in (2).

$$Z_{TH} = (U_{UNLOADED} - U_{LOADED})/(I_{test}) = \Delta U/I_{test} \quad (2)$$

Displayed prospective current (I_{psc})/(I_{sc}) in METREL is calculated as in (3) where U_n is the nominal source voltage of the grid and k_{sc} is the correction factor.

$$I_{psc} = (U_n * ksc)/Z_{TH} \quad (3)$$

Measured prospective short circuit current and grid/line impedance in test bays under different operating condition is consolidated in Table 2. A typical measurement set-up of impedance with different grid configurations is shown in [24].

Table 2. Measurement of short circuit current and grid impedance in test bays under different grid configurations

Operating conditions/grid configuration	I_{sc} (kA) (VFD Input)	Z_{TH} (VFD Input)
Bay A @ 415 V/grid 1	5.4 kA	76.9 mΩ
Bay A @ 415 V (12 P)/grid 2	2.6 kA	159.6 mΩ
Bay B @ 415 V/grid 3	9.2 kA	45.2 mΩ
Bay B @ 415 V (12 P)/grid 4	4.3 kA	96.5 mΩ
Bay C @ 415 V (direct)/grid 5	15.4 kA	26.9 mΩ
Bay C @ 415 V (300 kVA)/grid 6	1.9 kA	218.4 mΩ

4. RESULTS AND DISCUSSION

4.1. Simulation and test results (external AC reactor and built-in DC inductor)

Simulation (with a 100 kA grid in addition) and testing were performed with an external AC reactor whose value is 58 μH, 1.01 mΩ. VFD has a built-in DC inductor of 78 μH. Results are consolidated in Table 3 with various AC and DC reactor configurations. Following are the observations of the consolidated data:

- There was only a small change observed in VFD input current THDi with external AC reactor in addition to built-in DC reactor versus VFD without built-in DC reactor.
- 250 kW VFD was tested in bay A/B/C with 50% and 100% of its rated capacity. As test bays have different short circuit capacities considerable impact on VFD input current THDi is observed across various configurations.
- Simulation of grid with 100 kA short circuit capacity has a very high impact on VFD input current THDi both at 132 kW and 250 kW loading. VFD input Max and RMS current value is in proportion to grid short circuit capacity and adds to increased diode losses, DC inductor losses, and reduction in capacitor lifetime which are discussed in the following sections.
- VFD without a built-in DC reactor and external AC reactor has a substantial impact on THDi and RMS, Max current versus VFD with both DC and AC reactor respectively under various operating conditions.

Table 3. Simulation and experimental evaluation of VFD input THDi of test bays

Operating conditions	AC + DC reactor/input current *THDi*/RMS/Max	No reactor/input current *THDi*/RMS/Max	AC reactor/input current *THDi*/RMS/Max
Bay A (132 kW)/grid 1	27.1%/224/321	31.8%/226/341	28.5%/225/330
Bay A (250 kW)/grid 1	20.4%/438/593	23.8%/436/610	20.9%/438/599
Bay B (132 kW)/grid 3	31.6%/223/336	41.9%/229/379	34.2%/225/348
Bay B (250 kW)/grid 4	24.5%/423/591	31.3%/427/643	25.9%/425/607
Bay C (132 kW) (direct)/grid 5	33.7%/223/342	54.4%/241/431	38.8%/228/341
Bay C (132 kW) (300 kVA)/grid 6	18.5%/252/337	20.1%/250/341	18.9%/247/332
132 kW/100 kA grid	130.9%/336/877	131.9%/338/887	131.1%/337/880
250 kW/100 kA grid	120.0%/601/1489	121.0%/602/1490	120.0%/601/1489

4.2. Experimental testing and test set-up

To fulfill the objective of this research work and understand in detail the reliability effects of VFD, an experimental setup as in Figure 4 is being utilized for testing. A variable voltage taps change transformer is present in the supply system of the test bays A/B/C which is the power source for VFD under testing. The test system comprises active front end as a regenerative drive with load and test motor of identical capacity coupled against each other. Power analyzer PQ-box 200 is connected for the measurements of VFD input voltage, current, and distortion. Tektronix DPO is additionally connected to measure the voltage and current of the DC inductor and DC capacitor. Consolidation of test results with different grid configurations and identical loading conditions are as follows:

- A 415 V balanced power source to VFD of 250 kW loaded in test bays A and B at 132 kW and 250 kW respectively (grid 1 and grid 3).
- Additionally, 12 pulse transformer (1 MVA) was also interposed in test bays A and B establishing different grid configurations (grid 2 and grid 4) for testing the same 250 kW VFD.
- A 250 kW VFD is connected to test bay C from both 2500 kVA direct supply and alternatively through 300 kVA variable voltage transformer source (grid 5 and grid 6). Test bay C is limited to the loading of a maximum of up to 132 kW.

4.2.1. Test results

Effects of grid impedance variations with test bays of different grid configurations and their reliability effects on VFD front end diodes, DC inductors, and DC capacitor were consolidated and supported by the following measurements:

- VFD input current and distortion
- VFD input voltage and distortion
- Grid impedance measurements of test bays with different configurations (grid 1 to grid 6)
- Voltage and current measurements of the Inductor and capacitor in DC Link

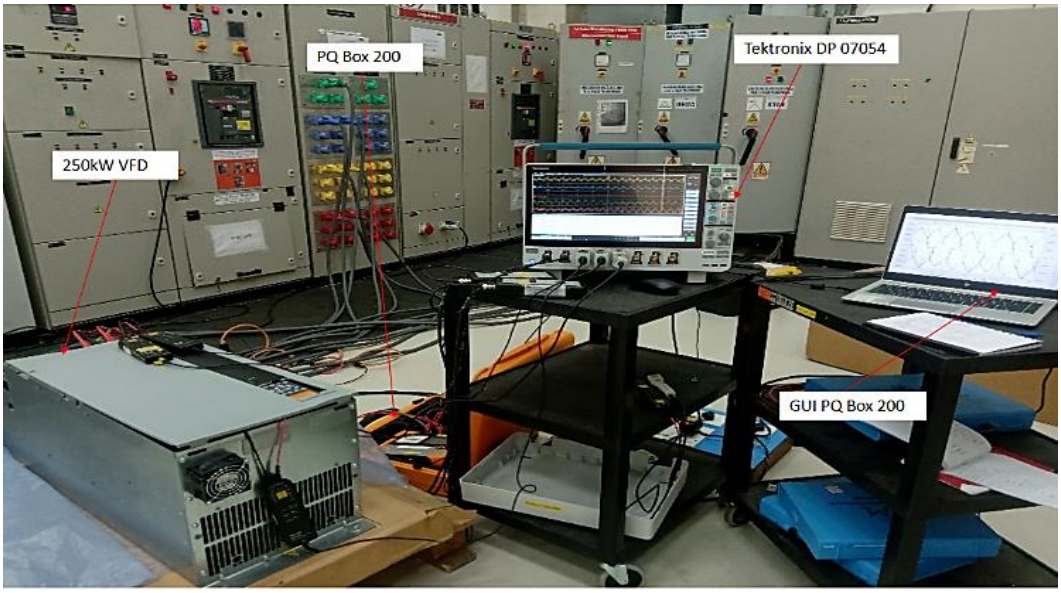

Figure 4. Experimental setup of VFD test system

Experimental results are consolidated in Table 4. VFD input *THDi* and *THDv* values are seen inversely varying across different operating conditions. VFD connected to Bay C (Direct)/Grid 5 during measurement is observed with the highest THDi (49.1%) and Max current value (404 A) at 132 kW as per Table 4. This is in line with bay C short circuit capacity compared to other grid configurations as per Table 2. However, it is observed grid with a short circuit current capability of 100 kA in our investigation has the highest impact on the input current maximum value (748 A). Real-time measurements with maximum possible loading and fine adjustments in the control system of test setup are consolidated as below. VFD input rectifier diode current wave shape is observed changing from continuous conduction mode to discontinuous with a proportionate increase in grid short circuit current of bay C (300 kVA), bay B (12P), bay B, and bay C (direct) as per Table 2 and as shown in Figures 5 to 8 respectively. Drive input THDi is also increased in proportion as shown in Table 4. A significant increase in drive input RMS, Max current, and THD_i across grid configuration is observed, as shown in Table 4. A substantial increase of DC inductor current is also observed during measurements with test bays having different grid short circuit current capability. This also impacts DC current ripple.

Table 4. Measurement results of VFD input THDi and THDv of test bays

Grid configuration	Input *THDv*	Input *THDi*	Input current (A/RMS)	Input current (A/Max)
Bay A (132 kW)/grid 1	5.9%	36.9%	196	351
Bay A (250 kW)/grid 1	9.4%	28.6%	366	608
Bay A (250 kW/12 P)/grid 2	13.8%	24.3%	388	561
Bay B (132 kW)/grid 3	4.9%	39.4%	202	374
Bay B (250 kW)/grid 3	7.6%	30.8%	369	609
Bay B (250 kW/12 P)/grid 4	12.5%	25.3%	379	588
Bay C (132 kW) (direct)/grid 5	2.3%	49.1%	209	404
Bay C (132 kW) (300 kVA)/grid 6	11.3%	28.2%	207	333
132 kW/100 kA grid *	1.2%	74%	259	510
250 kW/100 kA grid *	1.6%	47.2%	430	748

*Simulated grid results

Figure 5. Measured results: VFD input voltage and current, DC link voltage at 132 kW loading in test bay C (grid 6/300 kVA source)

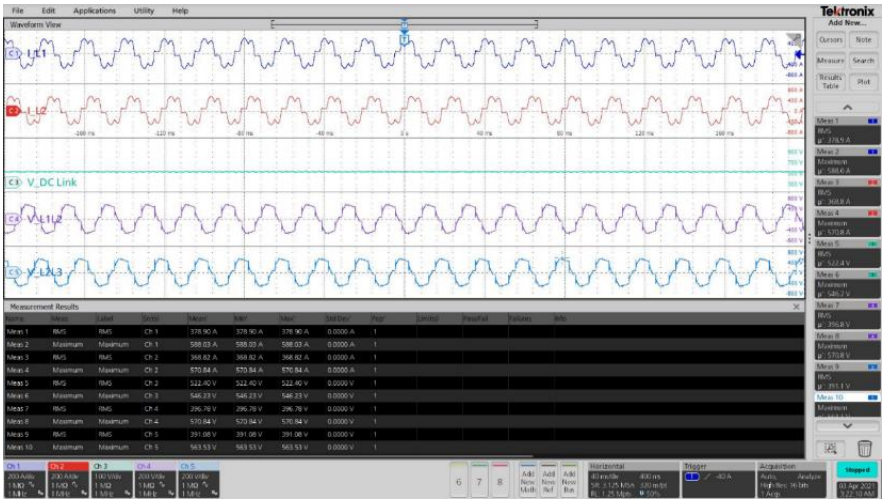

Figure 6. Measured results: VFD input voltage and current, DC link voltage at 250 kW loading in test bay B (grid 4/12 pulse transformer source)

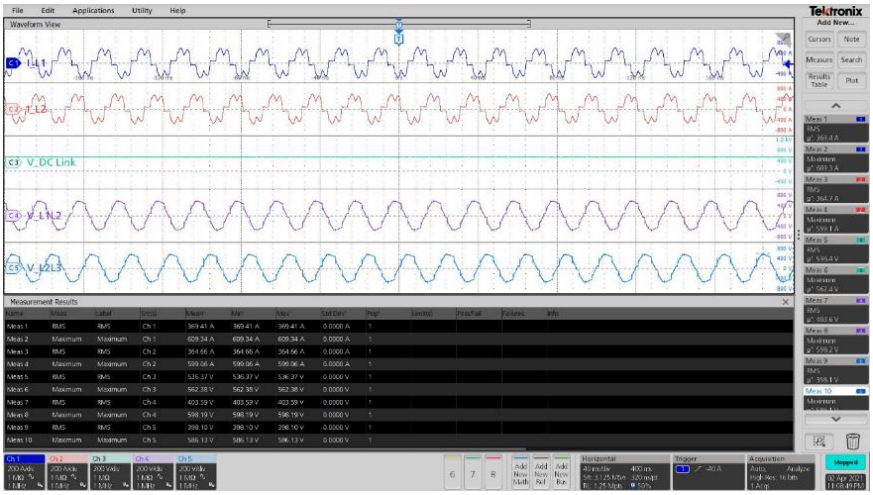

Figure 7. Measured results: VFD input voltage and current, DC Link voltage at 250 kW loading in test bay B (grid 3)

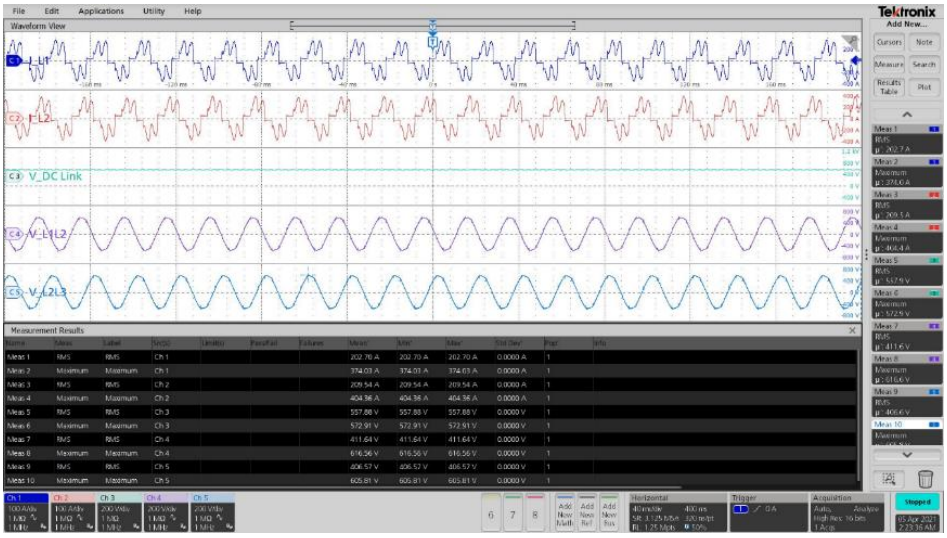

Figure 8. Measured results: VFD input voltage and current, DC link voltage at 132 kW loading in test bay C (grid 5/direct source)

4.3. VFD Simulation with test bay system

A discrete simulation model is developed for 250 kW, 500 V VFD using MATLAB® Simulink. R_S and L_S (X_{LS}) are the equivalent source resistance and inductive reactive component of the grid impedance. Practical measurements, analytical evaluation of test bay grid impedance, and short circuit current values consolidated as per Tables 1 and 2 is being used as the basis for VFD modeling in this research. *X/R* ratio of 2500/1000/500/300 kVA main power transformer as shown in Figure 1 is considered as 7. Effective values of DC link inductor (L_{dc}) and capacitor (C_{dc}) are 78 µH and 11750 µF respectively, considered during modeling. Resistive load (R_L) in the simulation model is selected to suit the VFD full load operating condition and also adjusted to match the required drive input current. DC Power across the resistive load (R_L) is maintained constant and is higher for 132 kW and 250 kW load with shaft power at 146 kW, and 275 kW respectively considering motor efficiency. Simulation results are consolidated in Table 5 as and as shown in Figure 9 to Figure 12 respectively. It is evident that grid impedance and short circuit current capability of test bays have a significant impact on VFD input THDv and THD_i, peak, and RMS currents. Figure 2 and Figure 3 clearly show the increased RMS, and peak current between grids of 5 kA and 100 kA short circuit current capacity. Figure 13 summarizes the grid impedance and short circuit current (kA) versus different test bay operating conditions and configurations. Grid with 100 kA capacity is observed to have the highest input THD_i, less significant THDv, and increased RMS and peak currents. Experimental testing, simulation, and analytical results are observed in agreement among similar grid configurations during analysis in this research.

Table 5. Simulation results of VFD input current and distortion with different grid configuration

Grid configuration	Input *THDv*	Input *THDi*	Input current (A/RMS)	Input current (A/Max)
Bay A (132 kW)/grid 1	6.9%	34.4%	204	339
Bay A (250 kW)/grid 1	10.1%	26.8%	381	593
Bay A (250 kW/12 P) grid 2	16.2%	23.3%	372	575
Bay B (132 kW)/grid 3	6.3%	34.1%	213	367
Bay B (250 kW)/grid 3	9.2%	27.8%	418	604
Bay B (250 kW/12 P)/grid 4	13.7%	24.4%	413	582
Bay C (132 kW) (direct)/grid 5	3.2%	47.7%	207	379
Bay C (132 kW) (300 kVA)/grid 6	10.6%	29.5%	206	337
132 kW/100 kA grid	1.2%	74%	259	510
250 kW/100 kA grid	1.6%	47.2%	430	748

4.4. Estimation of DC capacitor lifetime

DC electrolytic capacitors influence ripple reduction. Ripple current depends on DC inductor value, grid ratio (R_{sce}), and VFD switching frequency. Several performance parameters which affect the lifetime of the capacitor as recommended by manufacturers are operating temperature, applied voltage, ripple current, airflow, and load conditions, which play a significant role [26]. VFD switching frequency has a considerable effect on DC capacitor ripple current resulting in heat generation. Ripple current components contribute to

capacitor losses and equivalent series resistance (ESR) changes. Reduction in DC link voltage also increases capacitor lifetime. Simulated harmonic current spectrum, capacitor manufacturer frequency-dependent ESR characteristic curve, recommended ambient temperature (T_o) and thermal resistance (R_{th}) supports estimation of the DC capacitor power loss (P_d), internal high temperature spot (T_x), and increase in DC capacitor internal temperature (ΔT_x) due to various grid configuration and load conditions as expressed by (19)-(21) in reference [22].

The lifetime (L_x) of a DC capacitor in hours is expressed by (4) using hot-spot temperature (T_x), acceleration factor (K), and load life rating (Lo) [26].

$$L_x = L_0 * 2^{\frac{(T_0 - T_x)}{10}} * 2^{\frac{(\Delta T_0 - \Delta T_x)}{K}} * \left(\frac{V_0}{V_x}\right)^{4.4} \quad (4)$$

Where Vo and Vx are the DC capacitor specified and actual voltage values. Figure 13 summarizes in detail the estimated DC capacitor lifetime with different grid configurations. It is observed that there is a significant lifetime reduction in hours of DC capacitor wherein lower grid impedance exists or a grid with 100 kA capacity. VFD without a built-in DC reactor, loaded to 250 kW and connected to the grid with 100 kA capacity is observed during simulation to have the lowest capacitor lifetime (5410 hours). Figure 13 provides insight into DC capacitor replacement timelines as per the manufacturer's recommendation [26].

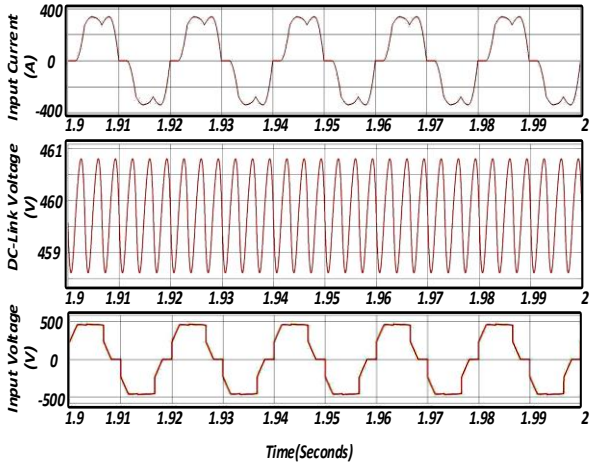

Figure 9. Simulation results: VFD input voltage and current, DC link voltage at 132 kW loading in test bay C (grid 6/300 kVA source)

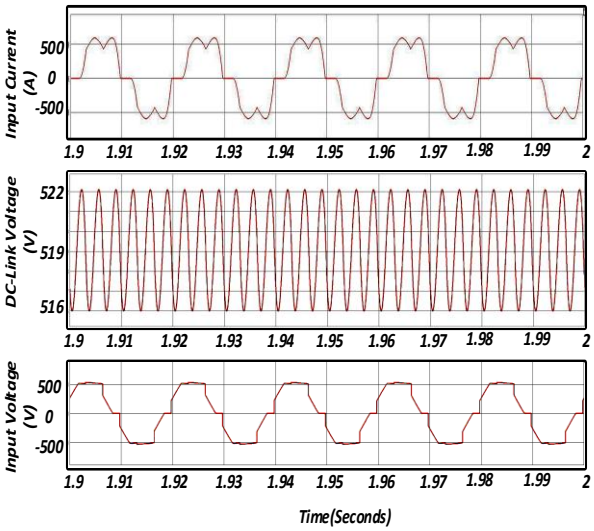

Figure 10. Simulation results: VFD input voltage and current, DC link voltage at 250 kW loading in test bay B (grid 4/12 pulse transformer source)

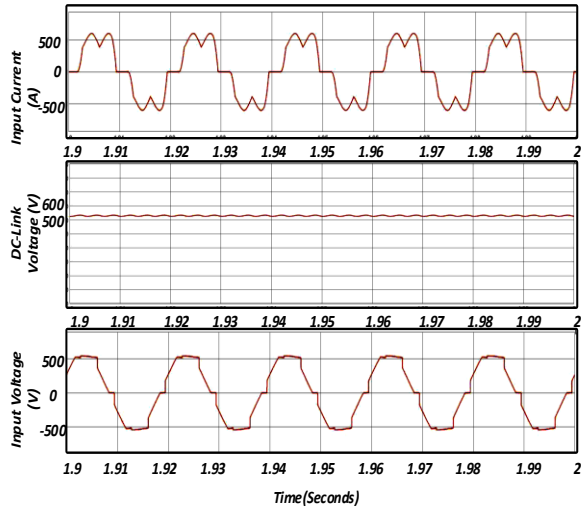

Figure 11. Simulation results: VFD input voltage and current, DC link voltage at 250 kW loading in test bay B (grid 3)

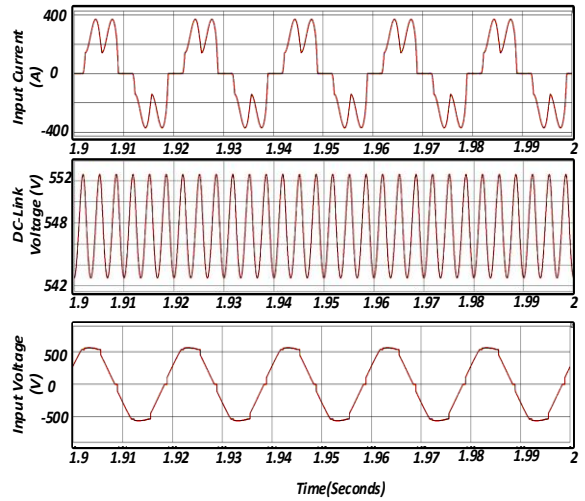

Figure 12. Simulation results: VFD input voltage and current, DC link voltage at 132 kW loading in test bay C (grid 5/direct source)

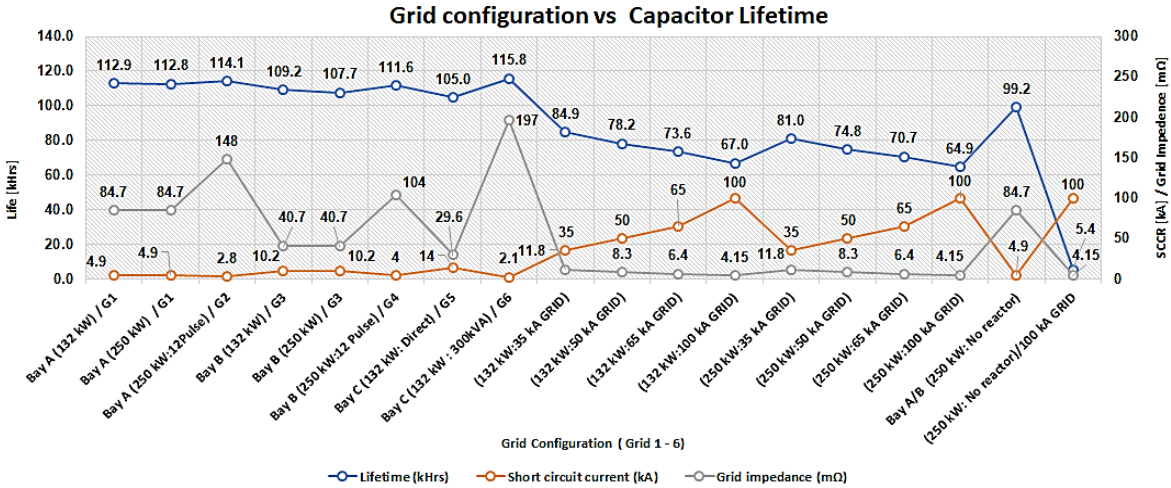

Figure 13. Capacitor lifetime for different grid configurations and short circuit current (kA)

4.5. Estimation of diode losses

VFD front end diode rectifier power dissipation is mainly contributed to its forward on-state conduction current. This mean forward power dissipation (P_{FAV}) is generally averaged over the entire operating cycle and is defined as a function of mean forward current (I_{FAV}) in [21] for different conduction angles. Power losses of the front-end rectifier diode estimated (1) under different grid configurations and operating conditions are consolidated in Table 6. It is observed that diode losses increase in proportion with input Max and RMS current value change. Diode losses are significant as the value of grid short circuit capacity increases (100 kA). Diode losses are observed to increase from 494 watts (bay A/grid 1/250 kW) to 893 watts (100 kA grid, 250 kW, no reactor).

Table 6. Estimated diode losses with different grid configuration

Grid configuration	Diode loss (watts)	Grid impedance (mΩ)	Input RMS (A)	Input max (A)
Bay A/G1 (132 kW)	242	84.7	204	339
Bay A/G1 (250 kW)	494	84.7	381	593
Bay A/G2 (250 kW: 12 P)	577	173	410	575
Bay B/G3 (132 kW)	240	40.7	213	367
Bay B/G3 (250 kW)	541	40.7	418	604
Bay B/G4 (250 kW:12 P)	550	104	424	582
Bay C/G5 (132 kW: D)	245	29.6	207	379
Bay C/G6 (132 kW: 300 kVA)	277	197	216	337
(132 kW: 35 kA)	263	11.8	240	448
(132 kW: 50 kA)	273	8.3	247	471
(132 kW: 65 kA)	278	6.4	251	487
(132 kW: 100 kA)	290	4.15	259	510
(250 kW: 35 kA)	541	11.8	420	691
(250 kW: 50 kA)	546	8.3	423	713
(250 kW: 65 kA)	552	6.4	426	727
(250 kW: 100 kA)	559	4.15	430	748
(250 kW: no reactor)	570	84.7	427	643
(250 kW: no reactor)/100 kA	893	4.15	601	1489

4.6. Estimation of DC inductor losses

DC Inductor current frequency spectrum constitutes DC and AC ripple components over the range of harmonic order. This has a significant impact on the core and winding reliability of the DC Inductor in a typical six-pulse diode bridge rectifier. High-frequency (2-9 kHz) performance is also estimated and losses are consolidated.

4.6.1. Core losses

The built-in inductor of six pulse VFD is designed to handle both fundamental frequency components and DC current. Grid impedance varies due to different configurations of test bays. VFD as connected load in such test bays experiences higher input peak current and increased current harmonics. This results in increased DC inductor current, speed reversals of flux and flux density [22]. Peak current increase is proportional to core loss. From the simulation results, DC inductor current (I_{pk}, I_{rms}, I_{dc}) and flux density (B_{pk}, B_{ac}, B_{dc}) along with other associated components are estimated through expressions (23)-(26) of reference [22] for individual harmonic order. The Power loss of XFlux toroid core (40 µ @ 50 kHz, Magnetics make, part no: 0078338A7) is expressed by (5) with performance curves provided by the manufacturer.

$$P_L = 151.44 * B^{1.58} * f^{1.09} \quad (5)$$

DC inductor core losses estimated through simulation are consolidated in Table 7. Total core loss is observed to be increased by 108%, 234%, 1%, and 1661% with test bays B and C as against bay A at 132 kW operating load from nominal grid short circuit capacity to 100 kA capability. Additionally, losses are increased by 130%, 957%, 1184%, 1346%, and 1590% respectively at 250 kW load from nominal grid capability to short circuit capacity in range of 35 kA to 100 kA. Core losses in (100-1500 Hz) and (2-9 kHz) range of frequency are observed having increased impact of 107%,133%, 237%, 1.1%, 1678%, 977%, 1208%, 1374%, 1622% and 50%, 20% respectively. Total losses of grid configuration with 12 pulse transformers are at 98.5%.

Table 7. DC inductor core and copper losses with different grid configuration

Grid configuration	Frequency range and total loss	Core losses (watts)/impact *	Copper losses (watts)/impact *
Bay A/G1 (132 kW)	DC current	-	40.00
	100-1500 Hz	0.91	1.91
	2-9 kHz	0.01	0.01
	Total loss	0.92	41.92
Bay A/G1 (250 kW)	DC current	-	130.60
	100-1500 Hz	1.00	2.02
	2-9 kHz	0.01	0.004
	Total loss	1.02	132.62
Bay A (12 P)/G2 (250 kW)	DC current	-	168.82
	100-1500 Hz	0.655	1.27
	2-9 kHz	0.009	0.004
	Total loss	0.67	170.1
Bay B/G3 (132 kW)	DC current	-	41.22/3%
	100-1500 Hz	1.90/107%	3.97/107%
	2-9 kHz	0.01	0.002
	Total loss	1.91/108%	45.2/7.8%
Bay B/G3 (250 kW)	DC current	-	146.54/12.2%
	100-1500 Hz	2.33/133%	4.82/138%
	2-9 kHz	0.015/50%	0.01/150%
	Total loss	2.35/130%	151.36/14.1%
Bay B/G4 (12 P) (250 kW)	DC current	-	173.40/2.7%
	100-1500 Hz	1.32/100%	2.66/109%
	2-9 kHz	0.01/11%	0.005/25%
	Total loss	1.33/98.5%	176.06/3.5%
Bay C/G5 (direct) (132 kW)	DC current	-	40.93/2.3%
	100-1500 Hz	3.07/237%	6.38/234%
	2-9 kHz	0.01	0.004
	Total loss	3.08/234%	47.3/12.8%
Bay C/G6 (300 kVA) (132 kW)	DC current	-	41.30/3.25%
	100-1500 Hz	0.92/1.1%	1.91
	2-9 kHz	0.01	0.02/100%
	Total loss	0.93/1.1%	43.2/3.1%
(132 kW) (100 kA)	DC current	-	40.20/1%
	100-1500 Hz	16.18/1678%	33.87/1673%
	2-9 kHz	0.006	0.003
	Total loss	16.20/1661%	74.07/76.7%
(250 kW) (35 kA)	DC current	-	133.81/2.45%
	100-1500 Hz	10.77/977%	22.39/1008%
	2-9 kHz	0.015/50%	0.006/50%
	Total loss	10.79/957%	156.21/17.7%
(250 kW) (50 kA)	DC current	-	132.73/1.63%
	100-1500 Hz	13.08/1208%	27.24/1248%
	2-9 kHz	0.012/20%	0.005/25%
	Total loss	13.10/1184%	159.77/20.5%
(250 kW) (65 kA)	DC Current	-	132.73/1.63%
	100 -1500 Hz	14.74/1374%	30.71/1420%
	2-9 kHz	0.01	0.004
	Total loss	14.75/1346%	163.44/23.2%
(250 kW) (100 kA)	DC current	-	132.73/1.63%
	100-1500 Hz	17.22/1622%	35.96/1680%
	2-9 kHz	0.008	0.003
	Total loss	17.24/1590%	168.69/27.2%

*Bay A is considered as a reference for impact estimation for all other bays/grid configurations under identical loading conditions

4.6.2. Copper losses

DC Inductor conductor carries DC and AC currents of different frequency orders. At higher frequency, current concentration is observed at the conductor surface whereas at low-frequency current is uniform throughout the conductor area. High-frequency influence is defined as the skin effect. Skin effect is expressed as AC to DC conductor resistance ratio in (6). Skin effect magnitude impacts the inductance of the DC inductor. Copper losses are estimated through the determination of flux density, DC and AC resistance, dc and ac current components, and skin effect [22].

$$\epsilon = \left(\frac{6.62}{\sqrt{f}}\right) * K[cm] \quad (6)$$

DC inductor copper and core losses estimated through simulation are consolidated in Table 7, along with their impact against similar reference conditions (bay A). Total copper loss is observed to be increased

by 8%, 13%, 3%, and 77% with test bays B and C as against Bay A at 132 kW operating load from nominal grid short circuit capacity to 100 kA capability. Additionally, losses are increased by 14%, 18%, 21%, 23%, and 27% respectively at 250 kW load from nominal grid capability to short circuit capacity in the range of 35 to 100 kA. Copper losses in (100-1500 Hz), (2-9 kHz) range of frequency are observed having positive impact of 107%,138%, 234%, 1673%, 1008%, 1248%, 1420%, 1688% and 150%, 25%, 100%, 50%, 25% respectively. Total copper losses of grid configuration with 12 pulse transformers are at 3.5%.

5. CONCLUSION

Grid impedance and its impact on the reliability of VFD front-end components is the main contribution of this research. Analytical estimation and measurements of grid impedance with different configurations were observed within close tolerance in this investigation. Practical testing and modeling of 250 kW capacity VFD with different grid configurations were done. Detailed analysis of the results revealed that there has been a considerable increase in current distortion and front-end rectifier peak current in proportion to the grid impedance increase observed with different configurations during testing. In addition, front-end diode losses, DC inductor core and copper losses, and capacitor lifetime is observed significantly impacted. The impact was also observed significantly with grid configuration having maximum short circuit current capability (100 kA). Capacitor lifetime is observed to be 5410 hours (250 kW at 100 kA grid capacity) as against 11285 hours (132 kW loading of Bay A). DC Inductor core and copper losses were studied with different grid configurations extensively and found to increase by 1590% (100 kA grid capacity) and 27% respectively. Under the low-frequency current range (100-1500 Hz) copper and core losses were observed to increase by 1622% (250 kW at 100 kA grid capacity) and 1680% respectively. DC inductor losses are increased by 50% in the (2-9 kHz) range of frequency (250 kW at 35 kA grid capacity) and 150% (bay B, 250 kW) respectively. Diode losses increased significantly to 893 watts (250 kW, no reactor, and 100 kA grid). Overall results of this investigation will serve as good inference to the design engineers for considering an adequate cushioning during the selection and sizing of VFD front end rectifier diode, DC Inductor, and capacitor when operating in grids with varying configurations, impedances, and short circuit current capability. Recommended VFD (Product and system level) standards for maximum current harmonic limits at different harmonic orders versus grid short circuit ratios are also verified during the investigation.

REFERENCES

[1] J. Ballingston, "IEEE recommended practice and requirements for harmonic control in electric power systems," *IEEE Std. 519-2014*, vol. 2014, p. 101, 2014, doi: 10.1109/IEEESTD.2014.6826459.

[2] "Electromagnetic Compatibility (EMC) – Part 3 – 2: Limits – Limits for harmonic current emissions (equipment input current ≤16A per phase)," *IEC 61000-3-2*, 2021.

[3] IEC, "IEC 61000-3-12 Electromagnetic compatibility (EMC) - Part 3-12: Limits - Limits for harmonic currents produced by equipment connected to public low-voltage systems with input current >16 A and <= 75 A per phase," 2011, [Online]. Available: http://www.iec-normen.de/217949/iec-61000-3-12-2011-05-ed-2-0-zweisprachig.html.

[4] J. Meyer, R. Stiegler, P. Schegner, I. Röder, and A. Belger, "Harmonic resonances in residential low-voltage networks caused by consumer electronics," *CIRED - Open Access Proceedings Journal*, vol. 2017, no. 1, pp. 672–676, 2017, doi: 10.1049/oap-cired.2017.0460.

[5] A. Grevener, J. Meyer, S. Rönnberg, M. Bollen, and J. Myrzik, "Survey of supraharmonic emission of household appliances," *CIRED - Open Access Proceedings Journal*, vol. 2017, no. 1, pp. 870–874, 2017, doi: 10.1049/oap-cired.2017.0458.

[6] J. P. Rhode, A. W. Kelley, and M. E. Baran, "Complete characterization of utilization-voltage power system impedance using wideband measurement," *IEEE Transactions on Industry Applications*, vol. 33, no. 6, pp. 1472–1479, 1997, doi: 10.1109/28.649958.

[7] A. Knop and F. W. Fuchs, "High frequency grid impedance analysis by current injection," *IECON Proceedings (Industrial Electronics Conference)*, pp. 536–541, 2009, doi: 10.1109/IECON.2009.5414978.

[8] S. Cobreces, E. J. Bueno, D. Pizarro, F. J. Rodriguez, and F. Huerta, "Grid impedance monitoring system for distributed power generation electronic interfaces," *IEEE Transactions on Instrumentation and Measurement*, vol. 58, no. 9, pp. 3112–3121, 2009, doi: 10.1109/TIM.2009.2016883.

[9] M. Jordan, H. Langkowski, T. Do Thanh, and D. Schulz, "Frequency dependent grid-impedance determination with pulse-width-modulation-signals," in *2011 7th International Conference-Workshop Compatibility and Power Electronics (CPE)*, Jun. 2011, pp. 131–136, doi: 10.1109/CPE.2011.5942220.

[10] L. Jessen, S. Gunter, F. W. Fuchs, M. Gottschalk, and H. J. Hinrichs, "Measurement results and performance analysis of the grid impedance in different low voltage grids for a wide frequency band to support grid integration of renewables," *2015 IEEE Energy Conversion Congress and Exposition, ECCE 2015*, pp. 1960–1967, 2015, doi: 10.1109/ECCE.2015.7309937.

[11] X. Wang, J. M. Guerrero, F. Blaabjerg, and Z. Chen, "A review of power electronics based microgrids," *Journal of Power Electronics*, vol. 12, no. 1, pp. 181–192, 2012, doi: 10.6113/JPE.2012.12.1.181.

[12] Z. Bin Ibrahim, M. L. Hossain, I. Bin Bugis, N. M. N. Mahadi, A. Shukri, and A. Hasim, "Simulation investigation of SPWM, THIPWM and SVPWM techniques for three phase voltage source inverter," *International Journal of Power Electronics and Drive Systems*, vol. 4, no. 2, pp. 223–232, 2014, doi: 10.11591/ijpeds.v4i2.5833.

[13] T. Zebbadji, S. Hadji, and R. Ibtiouen, "Line and grid impedance impact on the performances of a parallel connected modular inverter system," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 6, no. 1, pp. 100–108, Mar. 2015, doi: 10.11591/ijpeds.v6.i1.pp100-108.

[14] B. Hoseinzadeh, C. L. Bak, and F. Blaabjerg, "Impact of grid impedance variations on harmonic emission of grid-connected inverters," *2017 IEEE Manchester PowerTech, Powertech 2017*, 2017, doi: 10.1109/PTC.2017.7980873.
[15] X. Liang, Y. Luy, and D. O. Koval, "Investigation of input harmonic distortions of variable frequency drives," *Conference Record - Industrial and Commercial Power Systems Technical Conference*, 2007, doi: 10.1109/ICPS.2007.4292113.
[16] H. Wilken, M. Jordan, and D. Schulz, "Spectral grid impedance identification on the low-, medium- and high-voltage level - System design, realization and measurement results of grid impedance measurement devices," *Advances in Science, Technology and Engineering Systems*, vol. 4, no. 1, pp. 8–16, 2019, doi: 10.25046/aj040102.
[17] H. Langkowski, T. Do Thanh, K. D. Dettmann, and D. Schulz, "Grid impedance determination - Relevancy for grid integration of renewable energy systems," *IECON Proceedings (Industrial Electronics Conference)*, pp. 516–521, 2009, doi: 10.1109/IECON.2009.5414975.
[18] R. Stiegler, J. Meyer, P. Schegner, and D. Chakravorty, "Measurement of network harmonic impedance in presence of electronic equipment," *2015 IEEE International Workshop on Applied Measurements for Power Systems, AMPS 2015 - Proceedings*, 2015, doi: 10.1109/AMPS.2015.7312737.
[19] D. Chakravorty, J. Meyer, P. Schegner, S. Yanchenko, and M. Schocke, "Impact of modern electronic equipment on the assessment of network harmonic impedance," *IEEE Transactions on Smart Grid*, vol. 8, no. 1, pp. 382–390, 2017, doi: 10.1109/TSG.2016.2587120.
[20] A. Riccobono, M. Mirz, and A. Monti, "Noninvasive online parametric identification of three-phase AC power impedances to assess the stability of grid-tied power electronic inverters in LV networks," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 6, no. 2, pp. 629–647, 2018, doi: 10.1109/JESTPE.2017.2783042.
[21] "IXYS Inc." [Online]. Available: https://www.ptonline.com/articles/how-to-get-better-mfi-results.
[22] R. Pandurangan, P. Kaliannan, and P. Shanmugam, "Effects of current distortion on DC link inductor and capacitor lifetime in variable frequency drive connected to grid with active harmonic filter," *IEEE Transactions on Industry Applications*, vol. 57, no. 1, pp. 492–505, 2021, doi: 10.1109/TIA.2020.3028555.
[23] C. Bussmann, "Short-circuit calculations." [Online]. Available: https://www.eaton.com/content/dam/eaton/products/electrical-circuit-protection/fuses/solution-center/bus-ele-tech-lib-electrical-formulas.pdf.
[24] R. Pandurangan, P. Kaliannan, and P. Shanmugam, "Dynamic online grid impedance estimation and its effects on DC capacitor lifetime in variable frequency drive," *IEEE Access*, vol. 10, pp. 85243–85254, 2022, doi: 10.1109/ACCESS.2022.3197894.
[25] "METREL Euro Z800V MI3144 Manual." [Online]. Available: https://www.metrel.si/assets/Metrel/Navodila_instrumentov/Instruments/MI_3144_Euro_Z_800V/Ang/MI_3144_-_Euro_Z_800_V_ANG_Ver_1.3.3_20752881.pdf.
[26] "United Chemi-con.inc." [Online]. Available: https://chemi-con.com/capacitor-life/.

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