

Investigation of common mode voltages of single stage boost inverter for five phase induction motor drive

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ABSTRACT

In this manuscript, the single stage boost inverter is proposed to eliminate the common-mode voltage (CMV) and electromagnetic interference (EMI) in the motor drives. The proposed topology has the capability of eliminating the effects of intrinsic CMV without any additional filters, active or passive elements, and modified pulse width modulated (PWM) techniques. This topology is proposed with the rearrangement of filter components from ac side to mid place in such a way that the capacitor constantly clamped to the DC bus, and the inductor is placed at the mid-point of half-bridge module and supply to achieve the high gain. This arrangement is also eliminating the effect of switching natured common-mode voltage, which generally occurs in any conventional PWM inverter. Conventional PWM techniques can be implemented to this topology without any modification in the control strategy. The proposed topology is simulated in a MATLAB Simulink to verify the operation and CM reduction capabilities with the results of experimental prototype. In the manuscript, the proposed topology is compared with the traditional inverters and modulation schemes in terms of the CMV effect elimination to explain its effectiveness.

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1. INTRODUCTION

In recent years, multi-phase machine drives have gained significant interest within researchers because of its inbuilt benefits, which are provided by them in contrast to the five-phase counter parts [1], [2]. Minimizing the magnitude and enhancing the frequency of torque pulsation in the drive is achieved by implementing a multi-phase system. The reliability of the system enhances as the number of phases is increased because the motor drive can start and run even though one of the phases fails. Compared to five-phase motors, inverter-driven multi-phase motor drives have better electrical efficiency [3] and fault tolerance capability [4]. The latest advances in the field of multi-phase adjustable speed drives (ASD) have the following possible applications like electric-ship propulsion, grip of locomotives, electric and hybrid electric vehicles, more electric aircraft, and other high-power industries [5]. The aforementioned benefits and applications caused an interest in the development of multi-phase electrical drives, and these multi-phase drives are driven by the pulse width modulated inverter. Due to their high performance and simplicity of operation, the pulse width modulated (PWM) based inverter is employed in ASDs. One of the issues related to the PWM based inverter fed drives is common-mode voltage (CMV) generation because of different

switching state combinations [6]. As the technology of power semi-conductor continues to develop, the growing switching speed and switching frequency further intensify the problems associated with CMV [7]-[10]. This endangers the whole system reliability and security, which is necessary to be resolved, even in order to fulfil the electromagnetic compatibility (EMC) standards [11].

CMV can create issues like bearing current and shaft voltages, which are major causes for the failure of bearings [12]-[18], conducted and radiated electromagnetic interference (EMI) [19], ground leakage current, even mechanical vibrations [20]. Therefore, some strategies have been suggested in the literature for mitigation of CMV. CMV mitigating techniques may usually be divided into two types: software strategies and hardware strategies. The software strategy for the reduction of CMV is modifying the PWM techniques [21]-[30], which is more famous. Many of the CMV mitigating PWM techniques are based on the principle of SVPWM [21]-[24], which is implemented by choosing certain voltage space vectors (VSV) that give the minimum value or even zero CMV. Nevertheless, an analysis of the connection between the space vectors and the respective switching states can be a complicated task when the voltage levels or phase number is high.

In [25] and [26] numerous CMV suppressing CPWM techniques have been suggested that implements two modulating sinusoidal waveforms per phase leg. However, these techniques are applicable for five-level inverters, and the modulation index is restricted to lower than 0.87. For basic five-phase, voltage-source inverter (VSI), a phase-shifted sinusoidal pulse width modulation (PSSPWM) has been suggested in [27] with an interleaved SPWM, but it is not completely understood why the CMV is minimized. But in [6] it is extended for two level multi-phase inverters, an intersection-plotting technique is implemented to visually show how the waveform of CMV is produced and demonstrate clearly that the PSSPWM can significantly minimize the number of various overlap fields corresponding to unique combinations of switch states, thereby minimize the changes of the CMV [6]. The carrier peak position modulation (CPPM) strategy [28] overcomes a restriction of the modulation-index (MI). In the technique, a triangular carrier signal is adjusted (i.e., either by advancing or delaying) in order to prevent the occurrence of zero states. As an outcome, the maximum value of CMV is minimized for any modulation index. The aforementioned PWM schemes are capable of suppressing the CM current, but they cannot suppress EMI because they do not interact with the edges of switching, where the components of high-frequency are located. As well as, they will complicate the control scheme and raise the harmonics of current.

Hardware techniques comprise of methods with extra devices such as common mode choke [31], [32], active filters [33], and modified four-phase inverter topology [34]. In [25] and [35], a dual inverter topology is suggested to nullify the CMV in a motor drive. But, the overall count of devices doubles in this solution, and it will be difficult to synchronize between the two different inverters. Therefore, balanced inverter topography [36] is suggested for nullifying the CMV in inverter fed drives, which would be a better solution for all ASD, related CMV problems. In the suggested topology, the overall device rating is not increased, extra passive components are not at all required, and so it is economical and compact. Moreover, the standard PWM and control schemes can be applied to the five-phase balanced inverter without any alteration; as a result, it is simple to implement. So, this paper has put forward a “five phase balanced inverter topology” to gain the advantages of multi-phase system and balanced inverter topology.

2. CONVENTIONAL VSI AND CMV

Basic voltage source inverter comprises of five-phase legs; two semi-conductor switches are paired in series per leg. At the time of regular operation, in every phase leg, the voltage obtained at output terminals with respect to ground (viz., v_{ag} , v_{bg} , v_{cg} , v_{dg} , and v_{eg}) always varies between the negative and the positive DC bus voltage ($+V_{dc}/2$ and $-V_{dc}/2$ if the DC bus mid-point is considered as ground) because of PWM. As a result, based on the switching state, the inverter generated CMV changes, and it is expressed as (1). Fourier series representation of motor phase voltage is given by (2) to (6). Expression for common mode voltage in terms of fourier series is given by (7). The DC term is neglected for simplicity due to an artefact of the voltage definition. In (8) and (9) are common mode voltage root mean square (RMS) value with and without interleaving of carrier signal respectively.

$$V_{cmv} = \frac{(v_{ag}+v_{bg}+v_{cg}+v_{dg}+v_{eg})}{5} \quad (1)$$

$$V_{ag}(t) = \frac{V_{dc}}{2} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} (A_{mn} \cos(m\omega_c t + n\omega_o t)) + \sum_{n=1}^{\infty} (A_{on} \cos(n\omega_o t)) \quad (2)$$

$$V_{bg}(t) = \frac{V_{dc}}{2} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(A_{mn} \cos \left(m\omega_c t + n\omega_o t + \frac{2\pi}{5}(m+n) \right) \right) + \sum_{n=1}^{\infty} \left(A_{on} \cos \left(n\omega_o t + \frac{2n\pi}{5} \right) \right) \quad (3)$$

$$V_{cg}(t) = \frac{V_{dc}}{2} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(A_{mn} \cos \left(m\omega_c t + n\omega_o t + \frac{4\pi}{5}(m+n) \right) \right) + \sum_{n=1}^{\infty} \left(A_{on} \cos \left(n\omega_o t + \frac{4n\pi}{5} \right) \right) \quad (4)$$

$$V_{dg}(t) = \frac{V_{dc}}{2} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(A_{mn} \cos \left(m\omega_c t + n\omega_o t - \frac{4\pi}{5}(m+n) \right) \right) + \sum_{n=1}^{\infty} \left(A_{on} \cos \left(n\omega_o t - \frac{4n\pi}{5} \right) \right) \quad (5)$$

$$V_{eg}(t) = \frac{V_{dc}}{2} + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(A_{mn} \cos \left(m\omega_c t + n\omega_o t - \frac{2\pi}{5}(m+n) \right) \right) + \sum_{n=1}^{\infty} \left(A_{on} \cos \left(n\omega_o t - \frac{2n\pi}{5} \right) \right) \quad (6)$$

$$V_{cmv}(t) = \frac{V_{dc}}{2} + \frac{1}{5} \left[\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(A_{mn} \left(1 + 2 \cos \left(\frac{2\pi}{5}(m+n) \right) \right) \times \cos(m\omega_c t + n\omega_o t) \right) + \sum_{n=1}^{\infty} \left(A_{on} \left(1 + 2 \cos \left(\frac{2n\pi}{5} \right) \right) \times \cos \left(n\omega_o t + \frac{2n\pi}{5} \right) \right) \right] \quad (7)$$

$$V_{cmvr.m.s}(t) = \sqrt{\left[\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(\frac{A_{mn}}{5} \left(1 + 2 \cos \left(\frac{2\pi}{5}(m+n) \right) \right) \right)^2 + \sum_{n=1}^{\infty} \left(\frac{A_{mn}}{5} \left(1 + 2 \cos \left(\frac{2n\pi}{5} \right) \right) \right)^2 \right]} \quad (8)$$

$$V_{cmvnon-int r.m.s}(t) = \sqrt{\left[\sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} \left(\frac{A_{mn}}{5} \left(1 + 2 \cos \left(\frac{2n\pi}{5} \right) \right) \right)^2 + \sum_{n=1}^{\infty} \left(\frac{A_{mn}}{5} \left(1 + 2 \cos \left(\frac{2n\pi}{5} \right) \right) \right)^2 \right]} \quad (9)$$

The number of switching states in the five-phase inverter is 32 states, and the magnitude of CMV generated by the respective switching states is shown in Table 1. In the CM path, spurious grounding capacitances cause current pulses of high magnitude due to the varying CMV, which results in CM EMI and ground current. The coupling of CMV to the machine rotor results in bearing currents and voltage across the shaft.

3. PROPOSED INVERTER

3.1. Working principle

As similar to VSI with a passive filter, the capacitor clamped boost inverter (CCBI) topology is acknowledged with 10 switches and less passive parts (5 inductors and 5 capacitors) is as showed up in Figure 1. In recognize to different topologies, this topology assessed with the distinction in plan of circuit segments and adjustment as clarified in the accompanying segments. This sort of topological course of action of segments manages the cost of adaptability for both independent just as grid integrated applications when the necessary output AC voltage is more prominent than the supply voltage. This topology is created with no obstructing of reverse voltage switches. Consequently, it very well may be created by utilizing the comparative parts of any typical existing 5-phase VSI after re-organizing these segments (up-gradation highlight to profit the advantages of this topography) and varying the regulator, which decreases the load on manufacturing industries.

Each phase leg has a half-bridge module, which is clamped to supply voltage through a capacitor with an inductor positioned in between the midpoint of half bridge and positive terminal (p) of the supply voltage is as showed up in Figure 1. Loads (A/B/C/D/E) are tapped from the basic terminal of top switch and

capacitor in the particular phase. Capacitor voltages are regulated so that emphatically one-sided voltages of sine wave (with a bias voltage of V_{om}) are created across them utilizing tweaking signs and DC information voltage. These outcomes in emphatically one-sided $V_{AO}/V_{BO}/V_{CO}$ voltages in each phase load focuses (A, B, C, D, and E) w.r.t. the negative terminal of supply (o) with an inclination of $(V_{in}+V_{om})$ and relocation of 72° w.r.t. one another. The voltage perfectly forced on the terminals of (A or B or C or D or E) w.r.t. (o) comprises of two particular segments: i) DC segment (something very similar for each stage) and ii) AC segment (equivalent sufficiency for all stages with 72° phase displacement). It very well may be expressed as (10) and (11).

$$v_{ko}(t) = v_{kodc}(t) + v_{koac}(t) \quad (10)$$

$$k = A, B, C, D, E$$

$$\text{Here } V_{Aodc} = V_{Bodc} = V_{Codc} \text{ and } |V_{Aoac}| = |V_{Boac}| = |V_{Coac}| \quad (11)$$

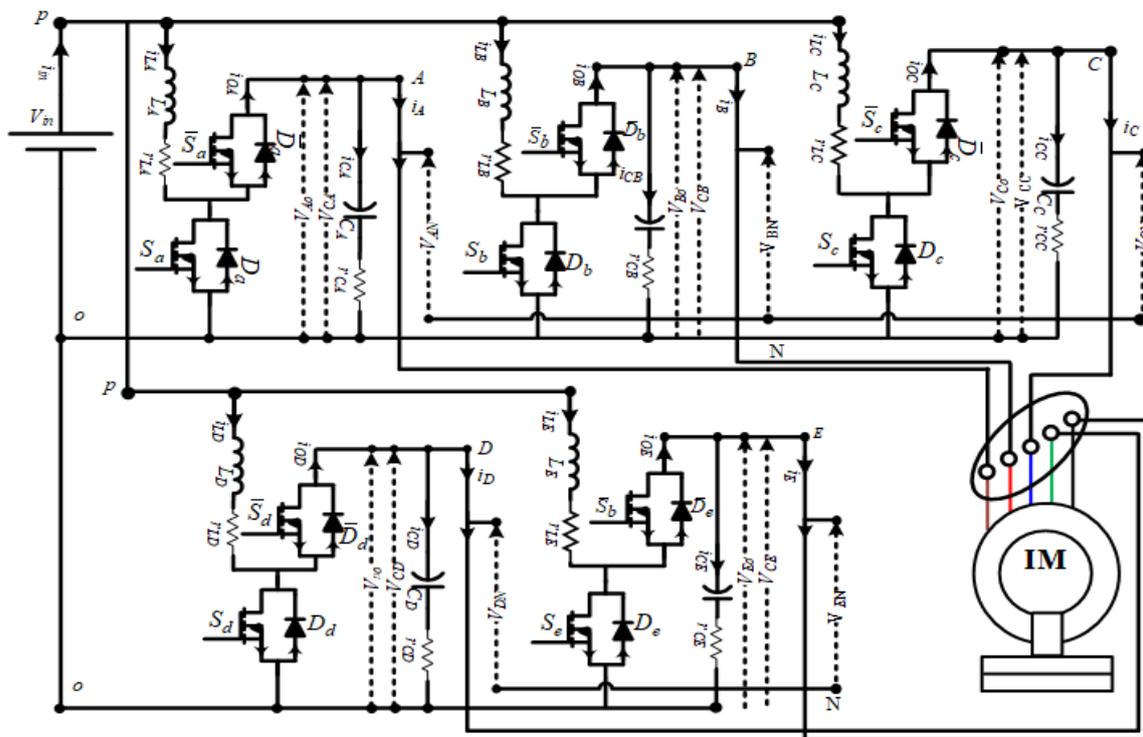


Figure 1. 5-phase proposed inverter topology

3.1.1. Numerical model

The method is able to break down utilizing two particular arrangements of conditions: the 1st depicts the input side and another portrays the output side. Both the sides of input and the output incorporate the segments of DC and AC. Equations on DC side: voltage equation at input side of the inverter can be composed as (12). The correlation between capacitor, source, and inductor currents can be represented as (13).

$$V_{in} = r_{Lk}i_{Lk} + L_k \frac{di_{Lk}}{dt} + p_k v_{ko} \quad k = A, B, C, D, E \quad (12)$$

$$\sum i_{Lk} = i_{in} - \sum i_{Ck} \quad (13)$$

Where V_{in} =input DC voltage, i_{in} =input current, $i_{LA}, i_{LB}, i_{LC}, i_{LD}$, and i_{LE} are currents L_A, L_B, L_C, L_D , and L_E are inductors and $i_{CA}, i_{CB}, i_{CC}, i_{CD}$, and i_{CE} are currents C_A, C_B, C_C, C_D , and C_E are capacitors respectively. Here $L_A = L_B = L_C = L_D = L_E = L$, resistance of the inductors $r_{LA} = r_{LB} = r_{LC} = r_{LD} = r_{LE} = r_L$, resistance of

the capacitors $r_{CA} = r_{CB} = r_{CC} = r_{CD} = r_{CE} = r_C$, $C_A = C_B = C_C = C_D = C_E = C$, and index 'k' represents the phase in all the equations. p_k and $\bar{p}_k (= 1 - p_k)$ are the discrete switching capacity related with the upper and lower switches individually and its worth can be either 0 or 1 based on the genuine state of the switch.

$$p_k = \begin{cases} 0 & \text{when } S_a \text{ off} \\ 1 & \text{when } S_a \text{ on} \end{cases} \tag{14}$$

AC side equations: the equation of output side load current can be represented as (15) and (16).

$$i_k = i_{Ok} + C_k \frac{dv_{Ck}}{dt} = C_k \frac{dv_{Ck}}{dt} + \bar{p}_k i_{Lk} \tag{15}$$

$$\begin{aligned} \therefore i_A + i_B + i_C + i_D + i_E &= (1 - p_A)i_{LA} + (1 - p_B)i_{LB} + (1 - p_C)i_{LC} + (1 - p_D)i_{LD} + \\ &(1 - p_E)i_{LE} + i_{CA} + i_{CB} + i_{CC} + i_{CD} + i_{CE} \\ \Rightarrow \sum i_k &= 0 (\because \sum i_{LA} + \sum i_{Ck} = i_{in}) \end{aligned} \tag{16}$$

Here $i_A, i_B, i_C, i_D,$ and i_E are the currents flowing all the way through the load terminals and $i_{OA}, i_{OB}, i_{OC}, i_{OD},$ and i_{OE} are the currents flowing through the upper switches of respective phases.

From (15), obviously inverter supplies capacity to the 3-phase load alike some former AC supply will do and inverter current on AC side submit to 5-phase basic rule. Along these lines, it very well may be utilized instead of some former DC-AC inverter. Further, a single-phase replica of the inverter is acquainted with examine the method in a superior and simple manner shown in Figure 2. Figures 3(a) and 3(b) shows single-phase equivalent circuit during on-mode and off-mode respectively.

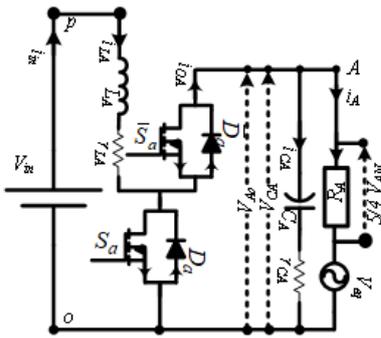


Figure 2. 1-Phase equivalent circuit

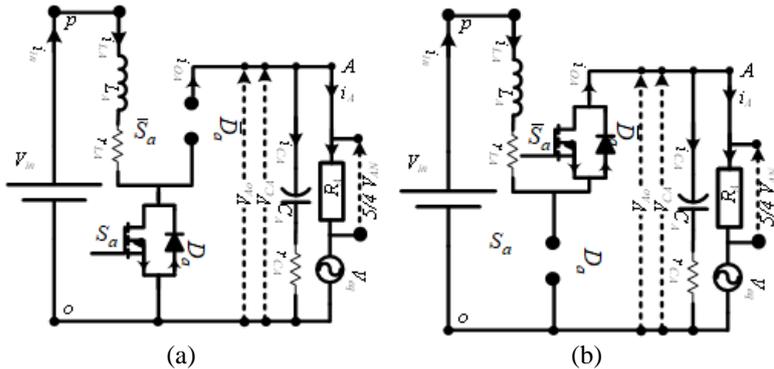


Figure 3. Equivalent circuit during (a) on- mode and (b) off-mode

3.2. Capacitor voltage profile

The key objective of this paper is reducing the peak voltage across the capacitor, and it can be calculated for the boost inverter as (18). Here $(V_{CO})_{DC} = (V_{AO})_{DC} - V_{in}$ and it can be calculated as $V_{CA} = V_{AO} - V_{in}$ expressed as (19).

$$\begin{aligned} V_{CA}(t) &= (V_{AO})_{DC} + (V_{AO})_{AC} \sin \omega t - V_{in} \\ \Rightarrow V_{CA} &= (V_{CO})_{DC} + (V_{CO})_{AC} \sin \omega t \end{aligned} \tag{18}$$

$$\Rightarrow V_{CA}(t) = \left(\frac{D_A(t)}{1 - D_A(t)} \right) V_{in} \tag{19}$$

In case of other topologies the capacitor voltages, it is higher owing to the requirement of higher DC-link voltage for the requisite DC-AC conversion. Capacitor voltage profiles for the DC-AC alteration of 1 to 1.8 in the proposed case and other similar impedance source inverters are shown in Figure 4, which depicts the reduction of voltage stress on the capacitor.

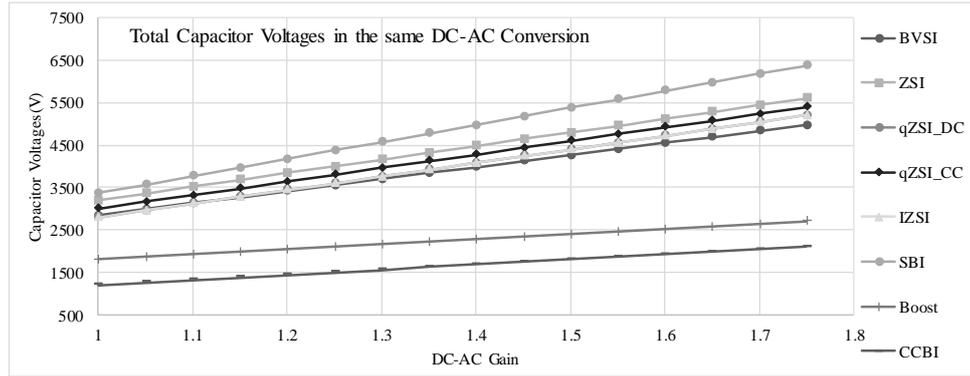


Figure 4. Capacitor voltage profiles

3.3. Common mode voltages

From the circuit shown in Figure 1, the common-mode can be considered as (20). Further simplifying using (21). Due to the variations in the space vector states and their dwell timings in the conventional two-level power converter topologies and impedance source topologies, the CMV will vary, as appeared in Figure 5. Preventing the utilization of the zero-states, the value of CMV is lowered to one-third of the voltage of DC-bus [34], [35]. The basic idea is utilizing the active voltage vectors, which are phase-shifted by 180° instead of a zero state, without influencing the linearity range. In contrast to the traditional PWM approaches, the value of CMV is restricted to one-third of the DC bus voltage instead of DC bus voltage. Besides, the number of switching per sampling period is varied method to method, as shown in Figure 5. From the Figures 5(f)-(i), unlike from conventional PWM techniques, it can be clear that there is no change in the CMV in the cases of RSPWM and proposed inverter with respect to switching per sampling period. Hence, there is no dv/dt effect due to switching action. From the Figures 5(a)-(k) except Figures 5(f)-(i), it can be clear that there is change in the CMV in the cases of non-RSPWM with respect to switching per sampling period. Hence, there is dv/dt effect due to switching action.

$$v_{cmv} = \frac{(v_{ag} + v_{bg} + v_{cg} + v_{dg} + v_{eg})}{5} \tag{20}$$

$$V_{cm} = V_{in} + V_m \tag{21}$$

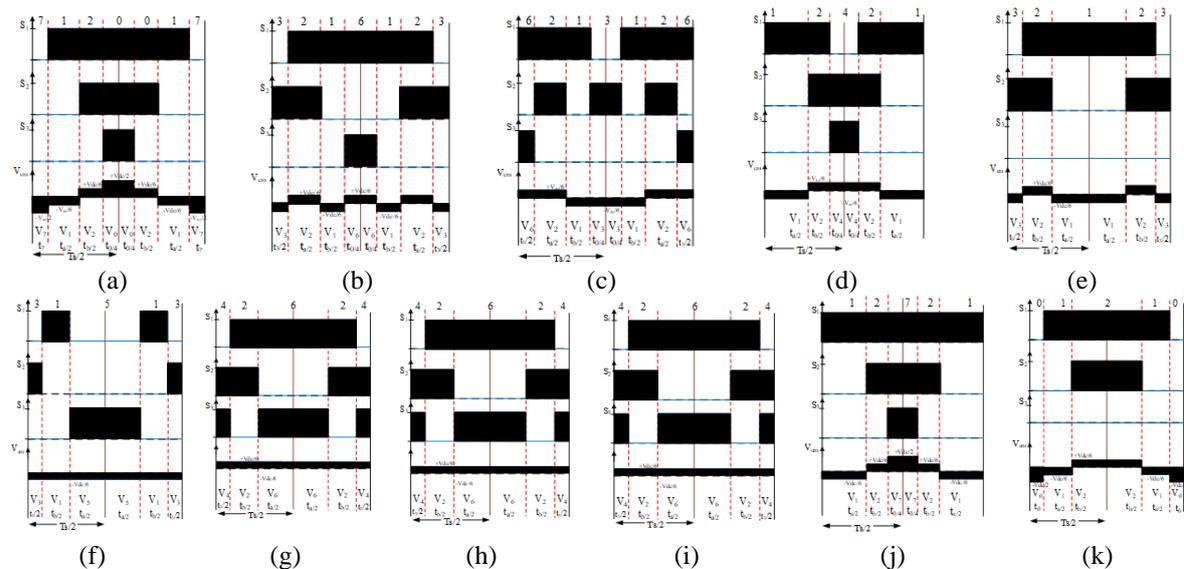


Figure 5. Space vector PWM techniques of (a) SVPWM, (b) AZSPWM1, (c) AZSPWM2, (d) AZSPWM3, (e) NSPWM, (f) RSPWM1, (g) RSPWM2A, (h) RSPWM2B, (i) RSPWM3, (j) DPWM (min), and (k) DPWM (max)

3.4. No. of components

As stated previously, by varying the configuration of impedance network, a variety of topologies were proposed, and hence each topology has a various number of components. Now, the number of components utilized for various topologies are listed in Table 1 and represented as the bar chart appeared in Figure 6. From this graph, it is very clear that the proposed boost-inverter needs less number of components when compared to the other topologies.

Table 1. Comparison table (peak DC-link voltages, voltages across capacitor, no. of components, and switching stresses)

Topology	Components				DC-AC Gain	D for required AC Gain	Peak DC-Link voltage	Capacitor Voltages (V_C)	Switch Voltages ($V_{S1}-V_{S6}$)	V_{LL} pattern	CMV Magnitude	CMV F_{sw}	Switching # per T_s
	S/D	DC L	DC C	DC L C									
B-VSI SPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
B-VSI SVPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
B-VSI DPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	4
B-VSI AZSPWM1	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	2-ph Bipolar	$1/5V_{DC}$ $2/5V_{DC}$	$3F_{sw}$	6
B-VSI AZSPWM2	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	2-ph Bipolar	$1/5V_{DC}$ $2/5V_{DC}$	F_{sw}	10
B-VSI AZSPWM3	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	2-ph Bipolar	$1/5V_{DC}$ $2/5V_{DC}$	F_{sw}	6
B-VSI RSPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	3-ph Bipolar	$1/5V_{DC}$ $2/5V_{DC}$	F_{sw}	8
B-VSI NSPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	Bipolar	$1/5V_{DC}$ $2/5V_{DC}$	F_{sw}	4
B-H7 MDPWM	8	1	1	3 3	$\frac{m}{(1-D_0)2}$	$\frac{2x-m}{2x}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	$\frac{V_{dc}}{1-D_0}$	Unipolar	$1/5V_{DC}$ V_{DC}	F_{sw}	6
ZSI	7	2	2	3 3	$\frac{(1-D_0)}{(1-2D_0)2}$	$\frac{1-2x}{1-4x}$	$\frac{V_{dc}}{1-2D_0}$	$\frac{(1-D_0)V_{dc}}{(1-2D_0)}$	$\frac{V_{dc}}{1-2D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
qZSI-DC	7	2	2	3 3	$\frac{(1-D_0)}{(1-2D_0)2}$	$\frac{1-2x}{1-4x}$	$\frac{V_{dc}}{1-2D_0}$	$\frac{D_0 V_{dc}}{(1-2D_0)}$	$\frac{V_{dc}}{1-2D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
qZSI-CC	7	2	2	3 3	$\frac{(1-D_0)}{(1-2D_0)2}$	$\frac{1-2x}{1-4x}$	$\frac{V_{dc}}{1-2D_0}$	$\frac{(1-D_0)V_{dc}}{(1-2D_0)}$	$\frac{V_{dc}}{1-2D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
IZSI	7	2	2	3 3	$\frac{(1-D_0)}{(1-2D_0)2}$	$\frac{1-2x}{1-4x}$	$\frac{V_{dc}}{1-2D_0}$	$\frac{D_0 V_{dc}}{(1-2D_0)}$	$\frac{V_{dc}}{1-2D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
SBI	7	1	1	3 3	$\frac{(1-D_0)^2}{(1-2D_0)2}$	$\frac{1-2x}{\sqrt{2x(2x-1)}}$	$\frac{(1-D_0)V_{dc}}{1-2D_0}$	$\frac{(1-D_0)V_{dc}}{(1-2D_0)}$	$\frac{(1-D_0)V_{dc}}{1-2D_0}$	Unipolar	$0-V_{DC}$	F_{sw}	6
CCBI	6	3	3	0 0	$\frac{1}{(1-D_0)2}$	$\frac{1}{1-2x}$	$2V_{om}$	$2V_{om}$	$2V_{om}$	Unipolar	V_{DC}	F_{sw}	6

*NA=not applicable

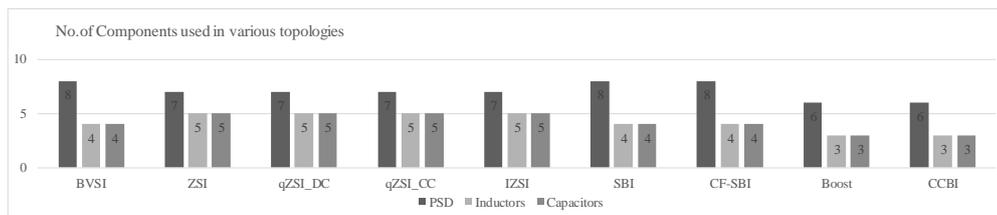


Figure 6. Bar chart showing number of components required in various topologies

3.5. Boost factors

As previously stated, as the impedance network configuration changes, the boost factors of every topology may differ from one another. Every topology has two boost factors. In theory, the greatest boost factor of any topology is infinite. Figure 7 depicts the boost factors necessary for the DC-AC conversion of 1 to 1.75, i.e., when 200 V DC is converted into 350 V AC to 600 V AC. This figure shows that the suggested converter can convert input DC into needed AC while maintaining a low boost factor as a referenced. Here the boost factors of every topology are listed in the Table 1.

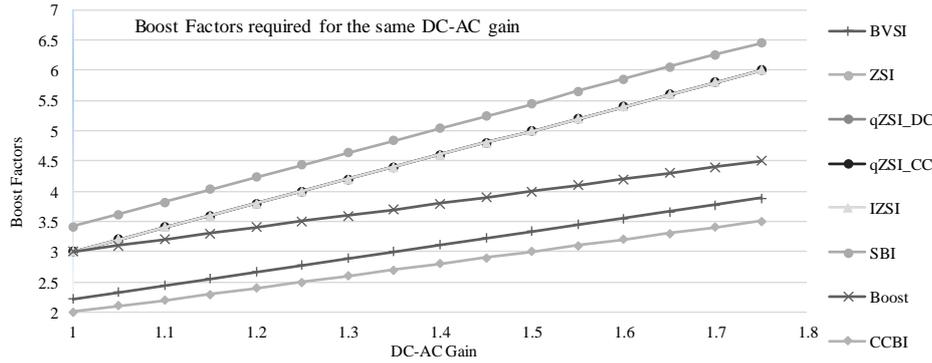


Figure 7. Boost factors required for DC-AC conversion of 1 to 1.75

3.6. Peak DC-link voltages

Peak dc link voltages in the same DC-AC inversion of various topologies are presented in Figure 8. DC links in each topology were varied in order to achieve a DC-AC conversion ratio of 1 to 1.75, i.e. 200 V DC is converted to 350 V AC to 600 V AC, as illustrated in Figure 8. This result demonstrates unequivocally that the DC connection voltage levels in the proposed scenario are low in comparison to others.

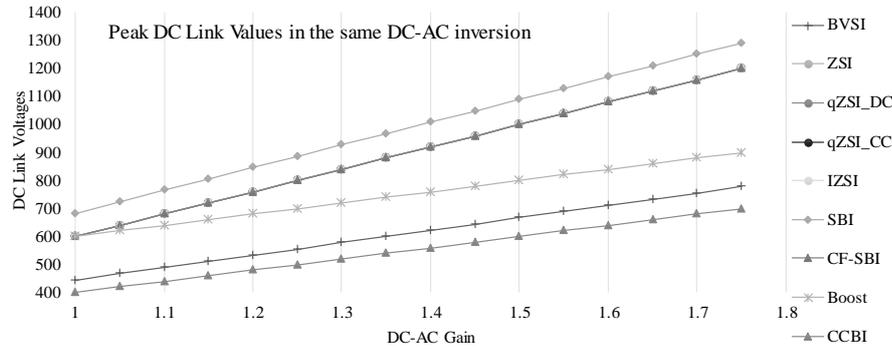


Figure 8. Peak DC link voltages of various topologies

4. RESULTS AND DISCUSSIONS

The proposed 5 – ϕ boost inverter has been effectively validated with the assist of simulations as well as experimental results. Environment utilized to carried out simulations is MATLAB/Simulink. Considered parameters for the simulations are listed in Table 2. System performance is assessed in both steady and transient states while feeding power to load under a variety of test environment. 200 V DC input is converted into 400 V (line to line) 5-phase AC sine voltages with 230 V (phase) and 4.33 A load current for a 3000 W resistive load.

Table 2. Parameters of the proposed converter

Parameter	Value
DC input voltage (V_{in})	200 V
Output Power	3000 W
Switching frequency ($\frac{1}{T_s}$)	10 KHz
Maximum converter output voltage ripple (% of $\Delta V_{A(max)}$)	32.65 V
Maximum inductor current ripple (peak-to-peak) ($\Delta i_{LA(max)}$)	10.45 A
Maximum duty cycle ($d_{(max)}$); $\frac{2d_{(max)}-1}{d_{(max)}(1-d_{(max)})} = \frac{\hat{V}_0}{V_{in}}$	0.7655
Inductor value ($L = \frac{V_{in}}{\Delta i_{LA(max)}} * d_{(max)} * T_s$)	600 μ H
Capacitor value ($C = \frac{1}{\Delta V_{A(max)}} * (\frac{V_A - V_B}{R}) * d_{(max)} * T_s$)	15 μ F
Approx. peak inductor current (valid in the linear region)	8.2 A
$i_{LA(max)} = \frac{1}{2} * \frac{1}{V_{in}} * \frac{V_0^2(RMS)}{R} + \frac{V_{A(max)} * \hat{V}_0}{V_{in} * R} + \frac{1}{2} * \Delta i_{LA(max)}$	

These load currents, line voltages, and phase voltage results are appeared in Figures 9(a), (b), and (c) respectively. This conversion is comparable to a 3.6 boost factor conversion in conventional switched-boost inverter (SBI), quasi-Z-source inverters (qZSI), and ZSI topologies. Unlike PWM natured voltages in voltage source and impedance source inverter topologies, nature of these output voltages are of sinusoidal even without any filter is placed on the AC side. Voltages across capacitor in each phase leg is appeared in Figure 10. Figure 11 showing common-mode voltages of the inverter. It very well may be seen from Figure 11 that the CMVs are steady in nature with an extent of 326 V alongside a 5% ripple. Though, PWM natured CMVs are created on account of any remaining reviewed topologies prompts leakage currents or ground currents. It additionally causes currents through bearings if there should arise an occurrence of drives and results in helpless efficiency and lifetime. Nonetheless, in proposed item, constant natured common-mode voltages don't result in any kind of leakage currents/ground currents.

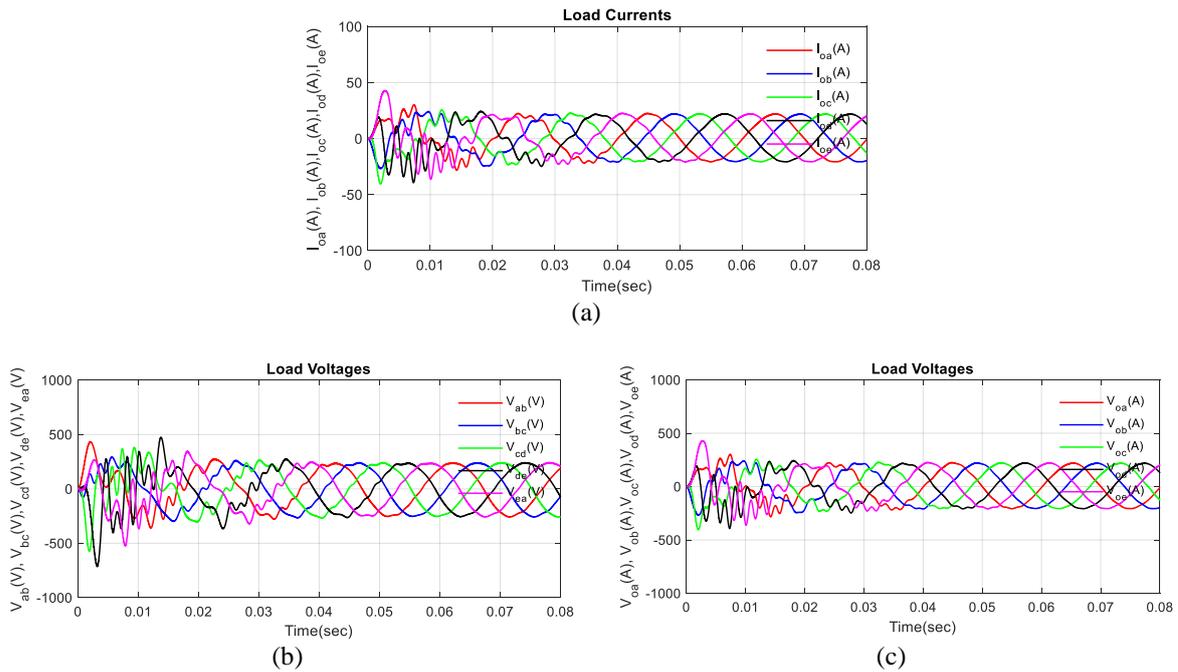


Figure 9. Inverter outputs with 200V DC-link for (a) load currents, (b) line voltage, and (c) phase voltage

For the basic assessment, the harmonic content of line voltage and load currents are captured and introduced in Figures 12(a) and (b) respectively. From these outcomes, it tends to be perceived that this inverter offers good quality of AC output (line to line voltage total harmonic distortion (THD) of 3.6% and current THD of 3.59%) without at all lower order harmonics surpassing 3% of fundamental with resistive load. It ought to be noticed that there is no filter on the AC side.

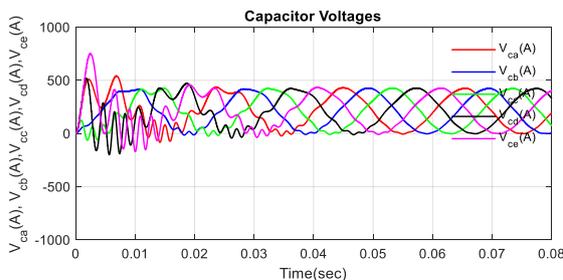


Figure 10. Capacitor voltages during steady-state conditions

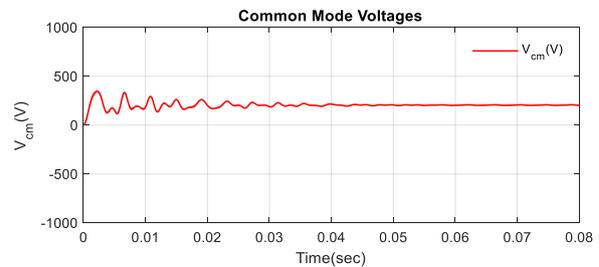


Figure 11. Common-mode capacitor voltage

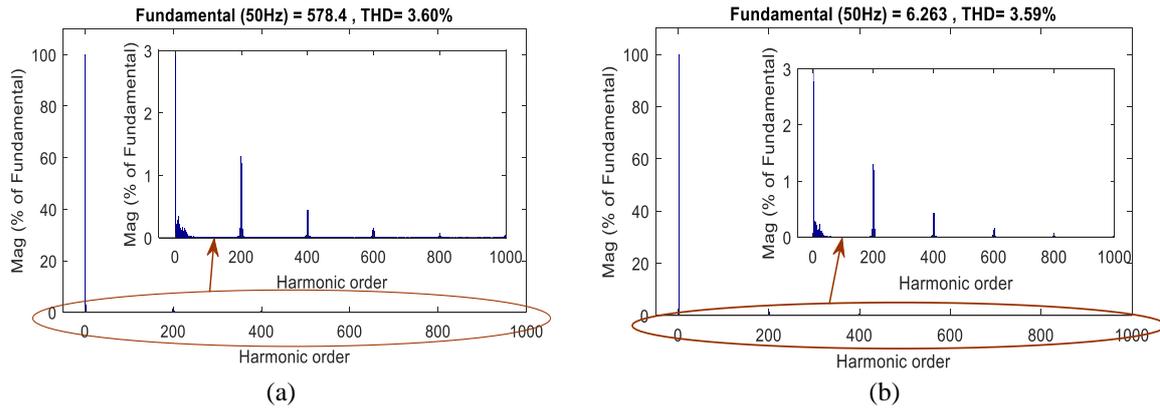


Figure 12. Total harmonic distortion waveform of (a) line voltage and (b) load current

5. EXPERIMENTATION RESULTS

For the experimental validations, a laboratory-scale model has been built which is appeared in Figure 13. It mainly consists of six IRF460 MOSFETs (500 V, 16 A) driven by a TLP25 optically-isolated driver circuit, three EZPE50506MTA capacitors (15 μ F) and five inductors (0.6 mH). Capacitor voltages and inductor currents are sensed by TELCON-25 and AD202JN signal measurement and conditioning circuits.

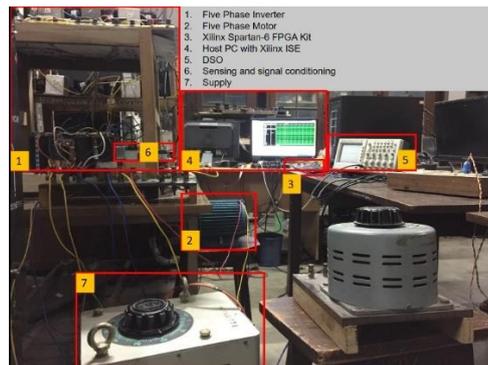


Figure 13. The prototype of boost inverter

Quantities are detected by these sensors-based resistor networks, associated with filtering, amplifying, and biasing circuits, and afterward applied to the corresponding multiplexer (HEF4052B) input terminals. All sensed parameters are fed to the FPGA Spartan-3E kit over a multiplexer circuit. Two 2-channel multiplexers are intended to handle the inductor currents and capacitor voltages independently with time-division multiplexing. Time-division multiplexed currents through inductor at channel-1 and voltages across capacitor at channel-2 are given to locally available ADC (LTC1407A) of the FPGA kit. These signs are isolated inside utilizing a demultiplexer executed through VHDL code. VHDL programmed sliding mode regulator make gate pulses to inverter switches by utilizing demultiplexed inductor currents and capacitor voltages.

To display the step-up capacities of the proposed inverter, the prototype is tried with 150 V DC supply and noticed the outcomes in a manner of closed-loop, in which the control logic is carried out in FPGA Sparta-3e XC3S500e board. The proposed converter, converts 150 V DC into 3-phase AC with a 282 V peak value. Pole voltages and 4.89 A (peak) phase currents are appeared in Figure 14 and Figure 16. Figure 15 addresses CMV, and its dc esteem is 320 V. Though, Figure 10 depict the capacitor voltages. These outcomes prompt that proposed converter performance is coordinated by the simulation results.

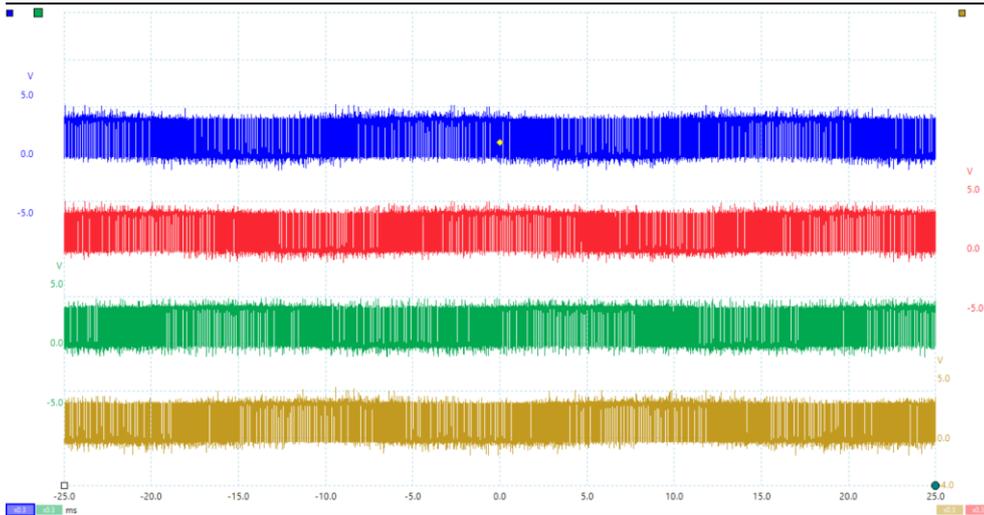


Figure 14. Pole voltage (100 V/div*3.2=320 V/div)

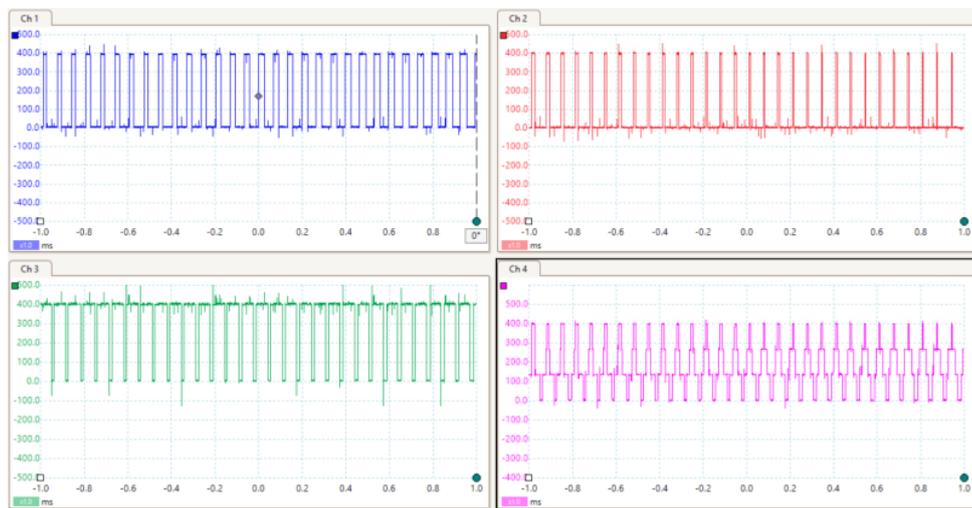


Figure 15. Common-mode voltage (500 V/div)

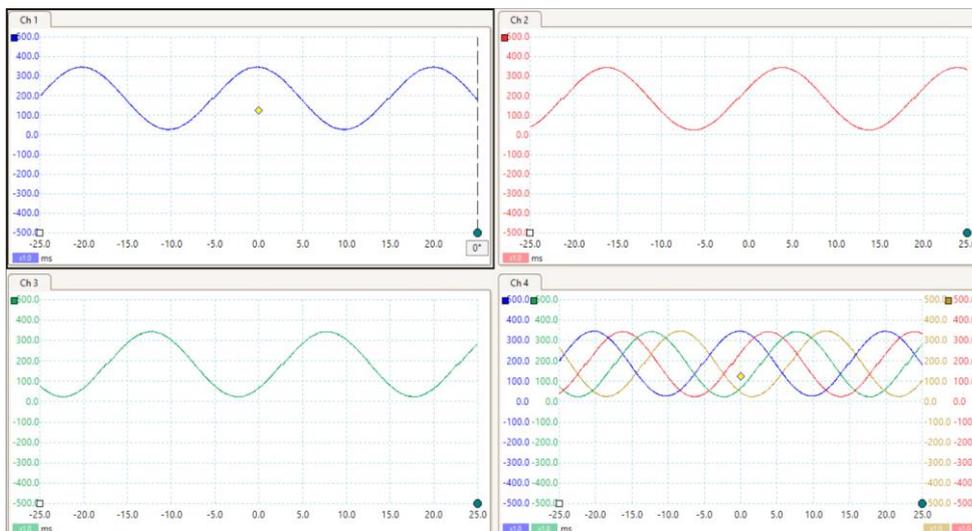


Figure 16. Load current (10 A/div)

6. CONCLUSION

This paper successfully validated the proposed single stage DC-AC converter with inherent step-up nature with the help of both simulations based and experimental based results. Results have proven that common-mode voltages produced by this inverter are constant natured instead of PWM natured in conventional inverter. Both hardware and simulation results validated that capacitor operating voltages are diminished, which results to enhance in the life and reliability of the capacitors as well as a converter. In addition to these, results have confirmed that the proposed inverter requires less boosting factor for the required DC-AC conversion, which can offer the lower DC-link voltage requirement. This feature offers the high side gate isolation voltage requirement when compared to other impedance source converters for the same DC-AC conversion. Another improvement of proposed topology is, it does not require any reverse voltage blocking capable switches and bulky passive elements.

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