International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 13, No. 3, September 2022, pp. 1469~1477
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v13.i3.pp1469-1477

Development of performance characterization in VSI fed induction motor drives using random PWM

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Article Info

Article history:

Received Mar 26, 2022
Revised Jun 3, 2022
Accepted Jun 20, 2022

Keywords:

Analysis multicarrier RPWM
Harmonics spreading
Mitigation acoustic noise reduction
Space vector PWM

ABSTRACT

Any industrial or power sector application requires a pulse width modulation (PWM) inverter. Industrial drives in particular are highly concerned with industrial standards. To satisfy the voltage source inverter (VSI) drives objects, a variety of PWM approaches are used, including inverter DC input voltage utilizations, suppression of higher and lower order of harmonics, as well as spreading harmonics, acoustic noise reduction, among others PWMs. One of the better approaches for minimizing noise on voltage source three-phase inverter fed drives is random pulse width modulation PWM random pulse width modulation (RPWM). Despite the fact that these described RPWM approaches are superior in terms of harmonic spreading and mitigation, these methods are unable to achieve the target DC-link utilizations. As a result, the focus of this paper is on combining multicarrier RPWM principles with space vector PWM space vector pulse width modulation (SVPWM) to produce multi-carrier random SVPWM (MCRSVPWM). The suggested PWM generates random unsystematic triangle carrier (5 kHz, 2.5 kHz, 1.25 kHz, 1 kHz) based pulses, whereas the traditional random PWM techniques are uses a fixed frequency triangular carrier to generate random pulse positions. Asynchronous induction motor driving simulation is carried out using MATLAB/Simulink. The proposed MCRSVPWM is put to the test with a 2kW six-switch VSI-fed induction motor drive system.

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1. INTRODUCTION

Voltage source inverter (VSI) based on pulse width modulation (PWM) are an unavoidable element of industrial drive systems. Voltage harmonics rejection, DC-link voltage usage, common-mode voltage (CMV) elimination, bearing current mitigations, and acoustic-noise eliminations, are all benefits of these voltage source inverter VSIs. To address the above needs, various types of PWM schemes have been developed in VSI [1]-[3]. Nonetheless, certain PWM techniques fail to reduce acoustic noise, which is a critical consideration for VSI-based motors [4]-[6]. Another standard for any PWM is the utilization of the DC-link to meet the drive needs. As a result, the power electronics researcher created real-time pulse width modulation (RPWM) random carrier PWM. Unlike sine PWM space vector pulse width modulation (SPWM), this PWM compares sinusoidal signals with random carriers to arrive pulse at the final result [5]. In various attempts to

minimise AC drives, PWM and external noise reduction filters have been suggested [7]-[12]. The RPWM is accomplished by altering the carrier wave's slope at random. Random carrier frequency PWM (RCFPWM) [13], random switching PWM (RSPWM) [14], and random pulse-position PWM (RPPPWM) [15] are the three main kinds of RPWM. The researcher changes the angle of the PWM carrier otherwise the voltage reference signal angle in RCFPWM to modify the carrier. RPWM can be incorporated using space vector PWM (SVPWM). The random signal is employed in RSPWM as a substitute of the carrier wave modification to provide the switching pulse width. In paper [16] used a digital logical circuit with gates to build the RPPPWM. To reduce electromagnetic interference (EMI) in electric motor systems, In paper [17] presented a chaotic pulse generation approach. Here motor current spectrum uses discrete components, it includes the circuit to choose their own needed carrier frequency [18], [19]. New-fangled constant carrier frequency quasi-random PWM approach is presented to eliminate harmonics by improving the drive without stimulating mechanical resonance [12]. More diverse states are necessary to generate a random bit number, which needs a higher number of successive digital states. However, as the number of digital circuits increases, so does the cost and difficulty of putting them together. As a result, the researcher advised that to boost randomization, a direct response shift register using linear feedback shift registers LFS register is used [19]. The size of the linear feedback shift register (LFSR) and the clock frequency existent influence the quantity of repetition. The sinusoidal reference is related to the engaging carrier triangle cycle to attain the pulses [20], [21]. To meet out these demand from the PWM, the paper proposed a hybrid PWM combining conventional RPWM with ramdom carrier and SVPWM [22] Few work is persented in PWMs gerneration spreading harmonics reduction to improve the the system's harmonic effects. Nevertheless, those methods ignore the acoustic noise effects and maximum possbile DC-link volatge utilizations [23]-[26]. Random space vector pulse width modulation for noise reduction in VSI fed induction motor cloud system model incoprated [27]. Random space vector PWM techniquies used for noise reduction in induction motor [28]. Hence the acoustic noise effects and maximum possbile DC-link volatge unitizations can be easly addressed.

The field programmable gate array FPGA used to buid the 8 bit and 16 bit PRBS to generate the discontinous random binary bits. The space vector PWM refence signal is associated with random carrier generator and PRBS binary selector block are organized by the same FPGA. A three-phase VSI linked 2.5kW 3-phase induction motor drive is simulated using the MATLAB/Simulink software package 2016. Different RPPWM, including the suggested MCRSVPWM, are studied in the inverter. The suggested approach uses switching frequencies of 1.25 kHz, 1 kHz, 5 kHz and, 2.5 kHz for random carriers. Test the experimental validity of the proposed MCRSVPWM is validated using lab scale setup of a 2-kW power capacity 3–phase VSI fed induction motor drive.

2. START OF THE ART OF RPWM

The main difference among traditional and random PWM is pulse signal width is no longer constrained to the operating frequency. The modulated signal and the switching frequency (carrier frequency) regulate relay [7]. Figure 1(a) shows the VSI, which uses 3 legs and 6 switches to synthesize 3-phase VSI output voltage. The structure of three Phase Induction motor is shown in Figure 1. The Figure 1(a) shows the 3-phase induction motor drive VSI. The Figure 1(b) shows the conventional RPWM PRBS, and Figure 1(c) shows the RPWM pattern generation. The randomization is achieved here using the PRBS binary digital assignment method. In the common PWM generation processes, the carrier wave generation is flowing to the fixed frequency carrier, whereas random PWM the carrier is handled by a multiplexer and a shift register. The triangle carrier 'Cr' (in fixed frequency) is providing via MUX (multiplexer) in the 'Cr' and 'Cr*-' sequences, as shown in Figure 1(c).

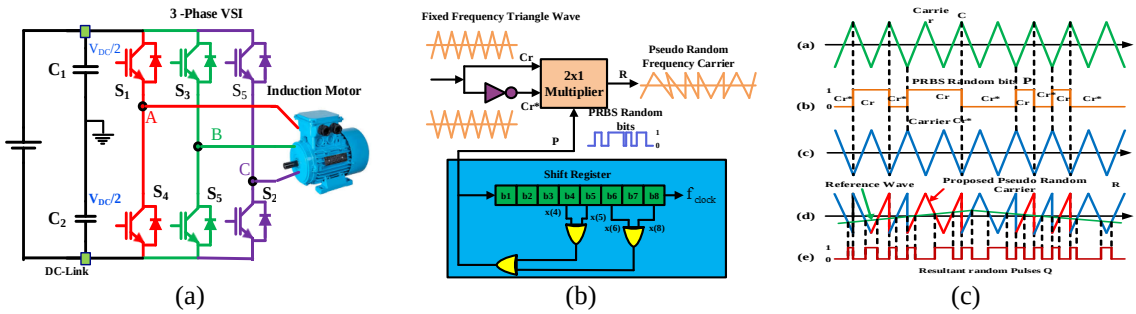


Figure 1. Structure of three phase induction motor drive: (a) 3-phase induction motor drive VSI, (b) conventional RPWM PRBS, and (c) RPWM pattern generation

The 'Cr*' is the inverse phase of the 'Cr' obtained using the 'NOT' gate. The constant frequency carriers 'Cr*' and opposed phase carriers 'Cr' are specified by the designated signal (S) of the multiplexer, and the 'Cr' and 'Cr*' are chosen at random. The MUX receives their chosen signal via a PRBS shift register. The exclusive or (XOR) gate is values of specific bits.

3. PROPOSED MCRSVPWM

RCPWM is essentially the same as regular SPWM, except with different carrier frequencies. To generate randomization on the resultant carrier, two necessary triangular carriers with 180° phase-shift is utilized. To begin, the proposed MCRSVPWM generated with the mixer of conventional random PWM and space vector PWM. Pulse width modulation scheme is shown in Figures 2(a), depicts the MCRSVPWM structure.

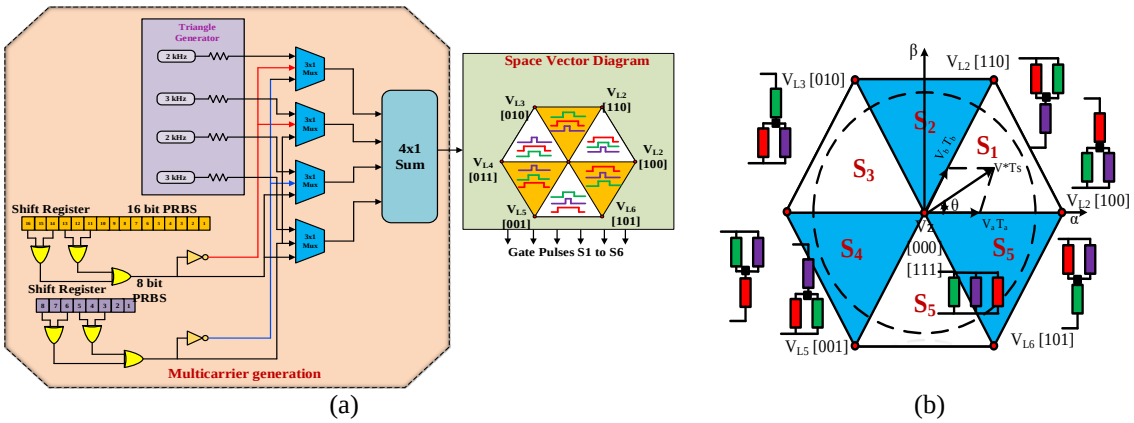
The randomization carrier is generated using four carrier signals with various frequencies of 1.25 kHz, 1 kHz, 5 kHz and, 2.5 kHz. Four multiplexers (MUX) are used to combine these random carrier signals, and the MUX output is then supplied to a 4×1 multiplexer. The PRBS generators with 16-bit and 8-bit to produce random manner arrangements '0' and'1', that modify the random mix of four carrier frequency signals. In the logic that one section significance in a series is not reliant on any extra sequence; hence the output is received in random manner. The multiplexers as well as random binary sequence are used to choose each carrier signal. The output of the 1st bit (bit 0) and 3rd bit D flip flop of the shift register (three-bit) are used to create PRBS in the example below. The same clock signal triggers all three D- flip-flops in the 3-bit shift register. The LFSR input is created by XORing the shift register's bit 0 and bit 2. The data shifting function is the only usage for the remaining D- flip-flop outputs. The pattern or sequence of bits created is the consequence of the combined effect of XOR's output and the inputs chosen by XOR.

With the support of a random frequency carrier signal and shift register the constant frequency clock (fc) is created. A pseudo-random carrier approach is used to generate a random choice of triangle carrier-waves with frequency (discrete in nature). Figure 2 shows the PWM scheme, Figure 2(a) depicts the 8-bit and 16-bit PRBS generation and Figure 2(b) shows the Space vector diagram. The output from the random bits generator's PRBS bits can be found in (1) and (2).

$$OPRBS - 8bit = B4 \oplus B5 \oplus B6 \oplus B8 \quad (1)$$

$$OPRBS - 16bit = B11 \oplus B13 \oplus B14 \oplus B16 \quad (2)$$

Where B_{xx} is the n-bit shift register's xth output bit and XOR. At what time of outputs is 8-bit and 16-bit PRBS generators are become zero, then the carrier with a frequency of 2 kHz is chosen. The frequency carrier wave 3 kHz is picked, once the 16-bit PRBS output 8-bit PRBS generator output are zero and unity respectively. The 3.5 kHz wave is picked, once the 16-bit PRBS generator output and the 8-bit PRBS generators are turn out to be one and zero. Figure 2(a) depicts the planned MCBRCPWM scheme.



(a) (b)

Figure 2. Pulse width modulation scheme: (a) proposed MCRSVPWM scheme and (b) space vector diagram

The multi-frequency carrier random signal is sent to the SVPWM reference signal generation block once after the random signal has been created. In the Figure 2(b) the planned SVPWM is notified in this case for adjusting random signals. Motor quantities (such as voltages, currents, magnetic flux, and so on) can be

sent into the SVPWM reference generator, which calculates the phase angle and magnitude of the SVD [22]. Every SVD sector remains an equilateral triangle with height; the height of a sector equals h (= 3/2). There are two sorts of voltage vectors: large vectors (LV) and zero vectors (ZV). The active vectors V_1 to V_6 are (1-11), (-1-11), (-111), (-11-1), (11-1), (1-1-1), whereas the zero vectors V_0 and V_7 are (000) and (111) respectively. For example, Figure 2(b) indicates that V* is located in sector-1, which is bordered by vector V_1. T_S is the switching sampling period (= $1/f_S$). From time t_0, V^* travels to t_1 as well as the association with the time-integral is specified as:

$$\int_{t_0}^{t_1} V^* = T_a V_1 + T_b V_1 \quad (3)$$

$$T_s = T_a + T_b + T_0 \quad (4)$$

Thus, the time expended by the zero vectors V_0 can be written as,

$$T_0 = T_s - T_a - T_b \quad (5)$$

Here, T_a and T_b is pulse width of the on-time pulse SVPWM.

4. SIMULATIONS

A three-phase VSI linked 2.5 kW 3-phase asynchronous induction motor drive is simulated using the MATLAB/Simulink software package (2016.b). Different RPPWM, including the suggested MCRSVPWM, are studied in the inverter. The suggested approach uses switching frequencies of 1.25 kHz, 1 kHz, 5 kHz and, 2.5 kHz for random carriers. Throughout the simulation, the VSI's DC-link voltage has been maintained at 400V, and the inverter has been operated in the modulation index range of 0.1 to 0.9 Ma. The Figure 3 shows Inverter line-voltage and corresponding voltage THD of MCRSVPWM for inverter modulation indices Figure 3(a) show the measured line voltage Ma=0.7. The voltage and its related harmonics spectra with M_a=0.7 are shown in Figure 3(b), Figure 3(c) show the measured inverter line voltage at Ma=0.9. The voltage and its related harmonics spectra with M_a=0.9 is shown in Figure 3(d). The basic voltage was archived linearly by altering modulation index, and the harmonics spectra (percentage VTHD) was validated as 47.790% and 52.890% respectively, which is smaller than all previous reported RPWM. As a result, when the inverter operates at a lower modulation, the Ma (low speed) operating zone decreases the VTHD and increases the ITHD. Table 1 displays all of the associated results for each operating zone. It is clear from the data that the inverter not only reduces THD but also maintains DC-link utilisation.

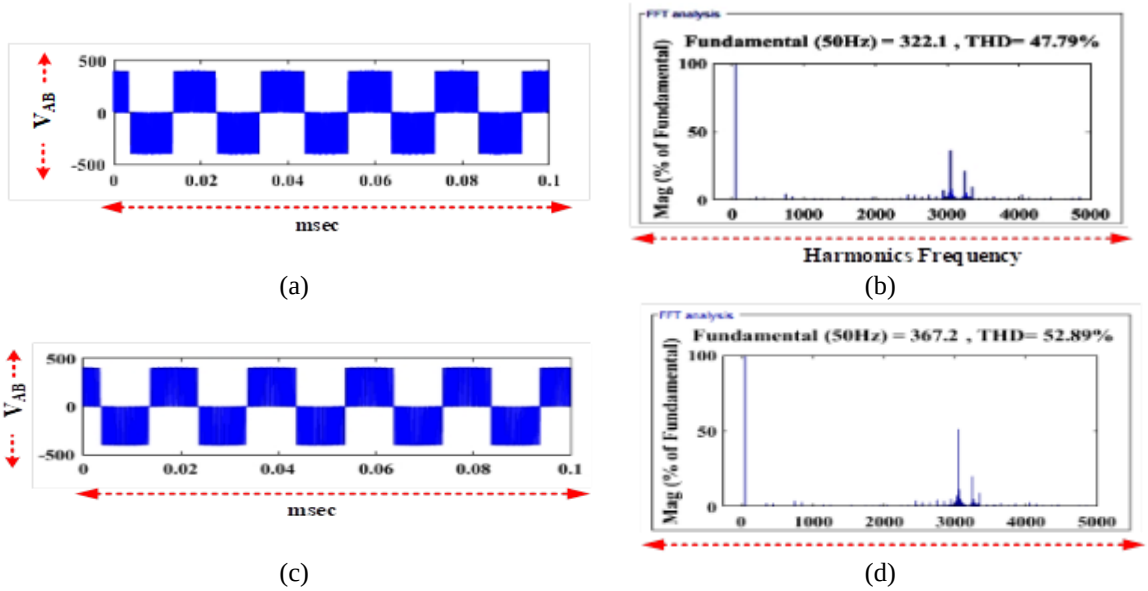


Figure 3. Inverter line-voltage and corresponding voltage THD of MCRSVPWM for inverter modulation indices, (a) inverter line -voltage Ma=0.7, (b) harmonics spectra for Ma=0.7, (c) inverter line-voltage Ma=0.9, and (d) harmonics spectra for Ma=0.9

The voltage and current spectra HSF noise is calculated by using [8] as follows,

$$HSF=\sqrt{\frac{1}{N}\sum_{j>1}^{N}(H_j - H_0)^2} \quad (6)$$

$$H_o=\frac{1}{N}\sum_{j>1}^{N}(H_j) \quad (7)$$

Here, H_j= harmonics amplitude and h_o = harmonic orders average value.

The white noise is zero when HSF is near zero. However, bringing the HSF to zero is only partially able. On the other hand, dealing with HSF should be small for better harmonic spread. As a result, the proposed PWM coin the lower HSF using a simple technique. Table 2 compares the simulated values of several PWM systems, including the proposed MCRSVPWM. The inverter operation voltage and current, as well as voltage THD and HSF, are all highlighted in the table. When compared to the other five situations, the proposed MCRSVPWM shows its superiority in terms of inverter operating range. When Ma = 0.8, RPWM and SPWM produce roughly 42.12% HSF reduction, chaotic PWM achieves 36.04% reduction, AMTCPWM achieves 14.03% reduction, and RCPWM achieves 21.05% reduction.

The Figure 4 shows the acoustic noise results of MCRSVPWM, Figure 4(a) shows acoustic noise results of MCRSVPWM with modulation index of 0.2, Figure 4(b) shows for Ma=0.5, Figure 4(c) shows for Ma=0.7 and Figure 4(d) shows Ma=0.9. While experiences the proposed RSVPWM with different motor speed, at low range speed the RSVPWM shown better response and disappearing the discrete frequency-component like RSWM. The other surrounded frequencies the discrete components are still present. When the motor operated at high and medium speed range, the proposed PWM is completely eliminated the discrete frequency-components. The suggested PWM eliminates all discrete components voltage as well as current spectrum frequency, which is not certainly abolished by a simple filter. The HSF for all recorded RPWM is compared to the proposed MCRSVPWM in Table-2. The MCRSVPWM has less HSF thought out the inverter operation, as can be seen in the table. The reason behind this is that spreading the carrier frequency reduces the dominating frequency component significantly, allowing the non-fundamental power to be spread out over a much larger frequency range, which helps to reduce acoustic noise.

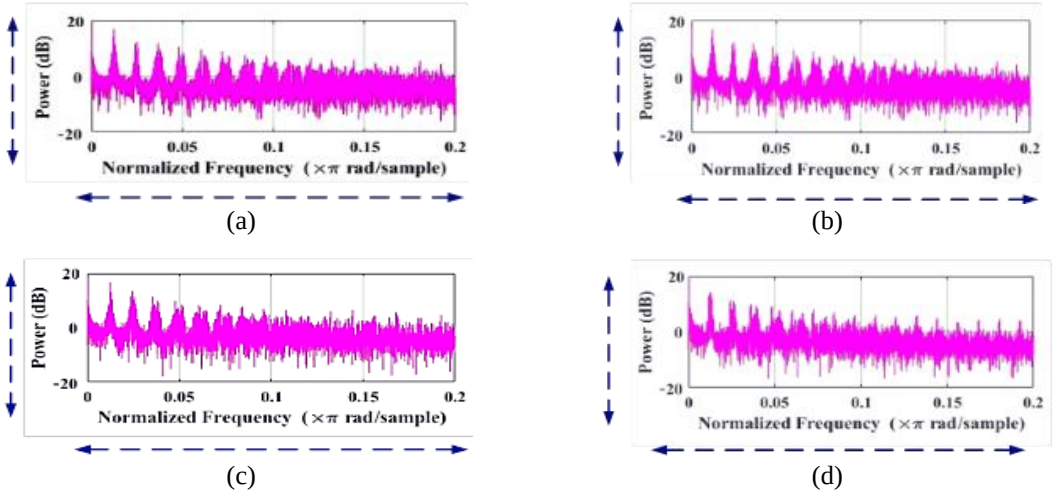


Figure 4. Acoustic noise results of MCRSVPWM with different modulation indies, (a) 0.2, (b) 0.5, (c) 0.7, and (d) 0.9

Table 1. Harmonics acoustic noise results MCRSVPWM with other methods

M_a	SPWM	RPWM	CPWM	RCRPWM	MRCRPWM	MCRSVPWM
0.2	8.310	8.110	6.090	6.267	4.128	4.032
0.3	7.562	7.420	6.020	6.127	4.01/	3.894
0.5	6.893	6.560	5.000	5.195	3.912	3.656
0.7	5.695	5.120	4.210	4.565	3.430	3.290
0.8	5.571	5.070	3.955	4.251	3.235	3.005
0.9	5.161	4.980	3.255	3.561	3.022	2.862

Table 2. Line voltage and harmonics simulation results MCRSVPWM with other methods

Ma	SPWM		RPWM		CPWM		RC-RPWM		MRCR-PWM		MCRSVPWM	
	V1	%VTHD	V1	%VTHD	V1	%VTHD	V1	%VTHD	V1	%VTHD	V1	%VTHD
0.2	55	54.82	43	49.82	56	51.84	56	54.42	58	47.49	59	46.87
0.3	81	53.21	62	47.21	83	52.54	83	53.01	89	45.67	90	44.51
0.5	139	46.06	112	51.06	142	50.35	142	45.52	146	49..25	149	47..98
0.7	194	54.41	156	54.41	189	56.21	197	54.41	204	52.06	207	51.04
0.9	248	59.45	215	56.454	253	56.18	257	58.43	263	53.54	267	52.89

5. EXPERIMENTAL VALIDATION

A VSI fed 3 Phase induction motor is used to test the experimental validity of the suggested RPWM. Figure 5 depicts the lab scale setup of a 2 kW power capacity 3–phase voltage source fed drive (induction motor) as well as the design flow of the MCRSVPWM FPGA implementation. The experiment uses a SCH2080KE MOSFET based VSI stack module. To achieve a maximum RMS AC voltage output of 400V, the VSI input DC-link capacitor 3400microF is used. The input DC link voltage bus maintains 550V. The switching frequency of the inverter is retained at 5 kHz. The suggested approach uses switching frequencies of 1.25 kHz, 1 kHz, 5 kHz and, 2.5 kHz with random carriers. The random carriers are generated via PRPS bit generator via FPGA (Spartan-6). Using the MATLAB Xilinx system generation implementation, the random carrier and SVPWM are created, and the bit file is generated by FPGA-controller. The multi-carrier 5 kHz, 2.5 kHz, 1.25 kHz, 1 kHz signals are created and stored with an FPGA look-up-table [22]. The various switching/carrier frequencies are combined using PRBS to generate binary in random manner and then fed into the SVPWM block for the final pulse generation. For an inverter leg, the dead-time is set to 6 micro-seconds. The VSI drive is put through its phases with various frequency combinations in order to change the mixer's carrier frequency sequence. The SVPWM allows the inverter operating modulation indices from 0 to 0.9.

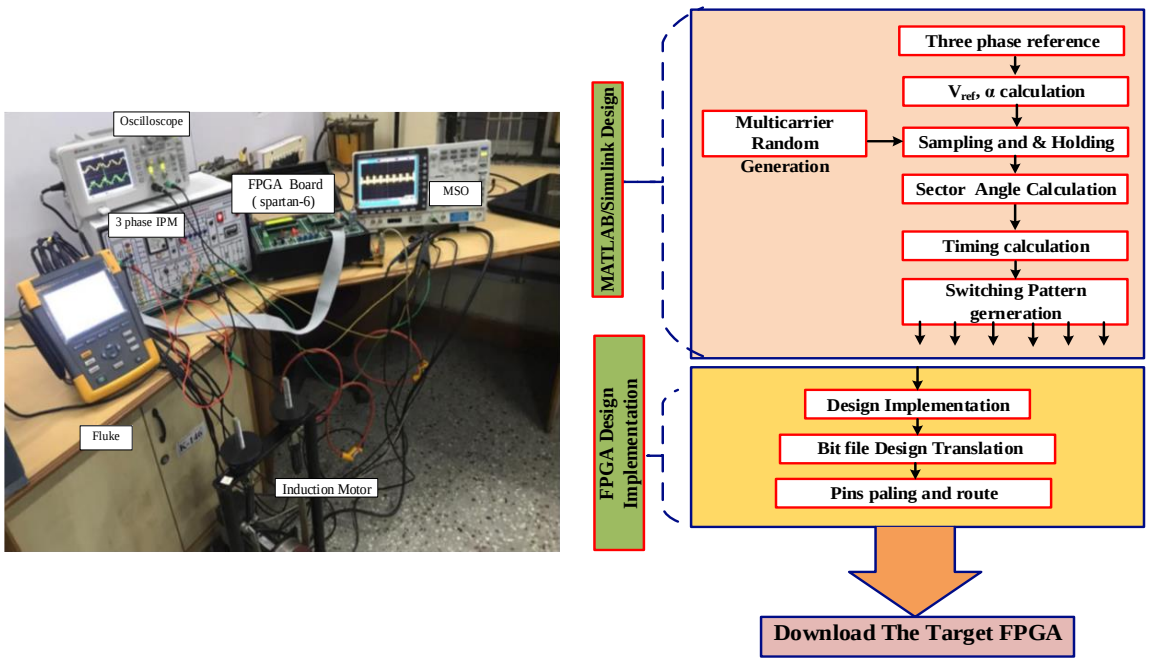
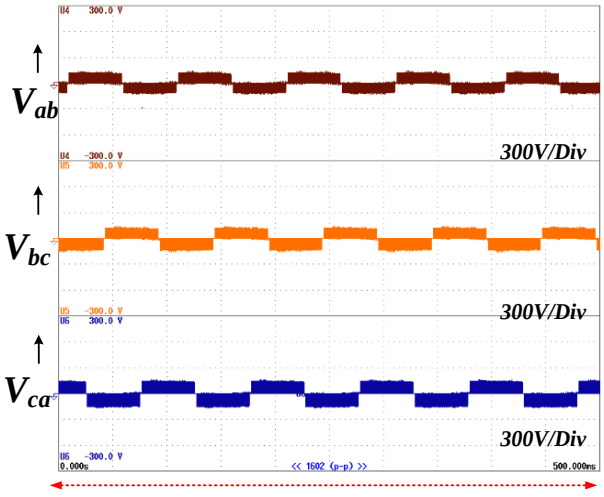
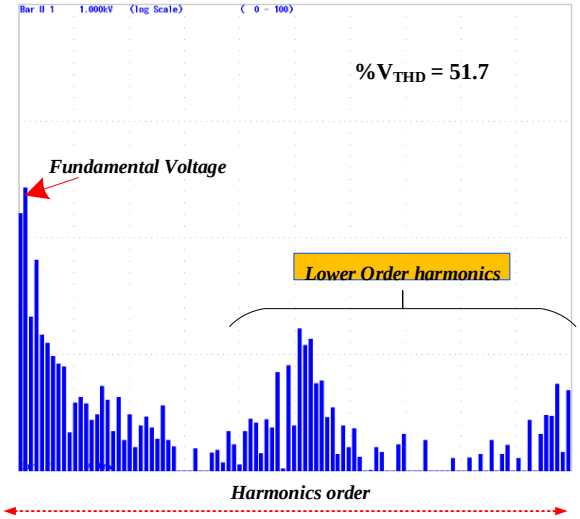


Figure 5. Experimental setup and implementation and design of MCRSVPWM implementation in FPGA

To begin with, the VSI is evaluated with different frequencies as fc1=5 kHz, fc1=2.5 kHz, fc1=1.25 kHz, fc1=1 kHz without floating combinations. The inverter voltage (VLL) of VAB and corresponding percentage voltage THD of 0.9 Ma are shown in Figures 6(a) and 6(b). The inverter voltage (VLL), VAB, increased to 263.5V, and the VTHD was found to be 51.70%. The analysis confirmed that while the induction motor is working at intermediate speed range (at Ma=0.6), the line voltage VAB as well as voltage THD are 123.5V and 53.80% respectively, under modulation. As a result of these findings, it is clear that the suggested MCRSVPWM maintains harmonics and inverter DC-link voltage at full inverter range of operations. The experimentation results confirmed the MATLAB simulation results.



(a)



(b)

Figure 6. Proposed MCRSVPWM results (experimental): (a) VLL for Ma=0.9 and (b) VLL voltage for Ma=0.9

6. CONCLUSION

The multi random carrier space vector PWM for 3-phase voltage source inverter fed induction motor drive is suggested in this paper to minimize the spreading harmonics acoustic noise. The proposed MCRSVPWM is proposed by using random-binary bits. The recommended PWM is associated with SVPWM, hence the with reduction of harmonics motor acoustic-noise in addition to the inverter DC–link utilization. Including the proposed MCRSVPWM other RPWM and SVPWM is simulated and compared. The Experimentations is build and validated through FPGA. The results are justifying the proposed RPWM performances associations with SVPWM by reducing harmonics acoustic noise with better DC–link utilization. This method can be recommended for the AC drives applications.

ACKNOWLEDGEMENT

This paper work is partially supported by Department of Science and Technology, Govt of India DST PURSE project. Project file number: DST/PURSE/2021/65.

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