Improved space vector modulation algorithm of 5-level threephase z-source based cascaded inverter

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ABSTRACT

The integration of a Z-source network with a 5-Level three-phase inverter based cascaded to provide voltage step-up function is proposed in this paper. The system is controlling by an improved space vector modulation (SVM) the implantation of algorithm and innovative virtual automated solutions can be considered, very fast and very simple. The main objective of the proposed system is to achieve an output voltage twice the applied input voltage, and to eliminate the largest amount of excess harmonic. This proposed model is characterized by the ease of boosting the output voltage twice the input voltage, depending on the characteristics of the Z-source network without the need for a DC-DC rectifier. Furthermore, the proposed algorithm for this system is characterized by improving the output voltage and eliminating a large number of harmonics while greatly simplifying the calculations compared to its conventional SVM. This makes the proposed system and its algorithm an interesting alternative to classical systems and algorithms. The simulation was processed using MATLAB/Simulink. The results obtained prove and verify the effectiveness of the proposed system. From the results, of the output current total harmonic distortion (THD), it was reduced to 1.05% which is very low compared to the other algorithms in the literature.

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1. INTRODUCTION

The use of inverters in industry has become a very wide field, especially multi-level inverters because they give a noticeable improvement in the spectral quality of the signal curve generated compared to conventional inverters therefore, it has attracted great interest from researchers, Especially on the part of developing control strategy, as industrial equipment increasingly uses variable speed motors, these inverters are especially widely used to control alternative current and the unbroken supply of energy [1]. Inverters are is being fed by a direct voltage source DC, or Z-source or PV+ rectifier DC-DC where we find that the Z-source inverters is one of the most apparent structures in the field of power electronics, as it has a wide range of applications for example its use in special power supplies and variable speed engines of hybrid electric vehicles and many more. The conventional Z-source consists of capacitors C1 and C2 and inductors L1 and L2 connected in on X shape to the power source with the main circuit of the inverter, various configuration of the Z-source network can also be made with the addition of nonlinear components such as diode or switches in the impedance network [2], [3].

This research relies on a group of previous studies in this field, to be a useful factor, the most important of which are Sanjay *et al.* [1] multi-level streak H-bridge inverter using multi-carrier SPWM technology. Subash [2], simulation and performance analysis of a Z-source inverter fed induction motor drive. Peng *et al.* [4] the new and innovative Algorithm virtual automated solutions are very fast and very simple in their implementation (A novel SVM algorithm for). Palanisamy *et al.* [5] simulation of the 5-level z-source based cascaded inverter use technology to control it sinusoidal pulse width modulation (SPWM). Bolaghi *et al.* [6] treat some topology for ZSI and compare it with some other topology. El-Hosainy *et al.* [7] review of the topology of the multi-level inverter, Control techniques and applications. Effah *et al.* [8] presented SVM three-level inverters with a single Z-Source network. Attique *et al.* [9], study on space vector pulse width modulation For multi-level inverters. Hanif *et al.* [10] presented Z-source inverter (ZSI) is proposed with buck-boost ability. Ghazali *et al.* [11] presented a new family of dc-dc converters with reduced passive components for PV systems (Z-source/quasi-Z-source topology). Novel circuit realization of the three-level space-vector pulse-width modulation (SVPWM) strategy [12].

In this paper, a Z-source inverter 5-level type cascade H-bridge is simulated, to highlight the properties of the Z-source network. Moreover, the research was expanded to include controlling the system by means of a developed SVM technology to facilitate and simplify the calculations and to obtain the least distortion in the output current. Also, the proposed system (topology + developed SVM technology) was compared with other existing control systems to highlight the advantages of this proposed algorithm. This paper includes the following elements: in the section 2, the characteristics and features of the z-source network were explained, in the section 4. Control algorithms discussed, in section 5 the simulation was implemented. And explain the results obtained. Finally, in section 6 a conclusion is presented that summarizes the goals we reached in this study.

2. Z-SOURCE NETWORK

2.1. Conventional z-source VSI network

Z-source is a system consisting of a mixture of 02 inductors and 02 capacitors and it works as a storage device for power, as it is more efficient in reducing the value of voltage and wave current in the circuit and the value of the inductor and capacitor determines how much power is stored and the value of the output voltage where Figure 1 represents the conventional network of a Z source circle [13]. The cutter of Figure 1 is five times the cut of frequency of a conventional inverter which requires a combination of L-C in the system network.



Figure 1. Conventionnel z-source VSI network

From Figure 1, the voltage equations can be written as:

$$V_{1n} = V_{L1} \tag{1}$$

$$V_{1n} = V_{L1} + V_{c2} \tag{2}$$

$$V_{aut} = V_{c2} - V_{L2}$$
(3)

When placing three signals, so that the first signal is larger than the rest of the two, and the third is opposite to the second is the signal, and when the first signal is smaller than the third, all switches in the leg are turned

on, a short circuit will occur so during this case the amount of voltage stored in the specific inductor and capacitor begins to charge, which produces additional stored power with applied input voltage. Figure 2 shows the controller for Z-source inverter.

$$a = 1/2 * Te;$$

$$F = 2 * (((t - a/4)/a) - floor((t - a/4)/a)) - 1;$$

$$vb = 2 * abs(F) - 1;$$

$$vp = .727;$$

$$vn = -.727;$$

$$if P \ge vp || P \le vn$$

Give the value 1 for each control signal in the system.



Figure 2. Controller for z-source inverter

2.2. Three phase 5-level z-source cascaded type h-bridge inverter

The use of the multi-level inverter helps eliminate a large part of the harmonics and reduces the voltage pressure on all switching devices as well, to produce better output voltage and improve current control, and adding a network Z-source in front of a system CHBI can improve the output voltage value two times greater than the conventional system [14], [15]. Voltage in capacitors C1 and C2,

$$v_{c1} = v_{c2} = \left(\frac{\frac{T-T_a}{T}}{\frac{T-2T_a}{T}}\right) \times V_{aut}$$

$$\tag{4}$$

and from it, the reinforcement factor is derived from the (4):

$$G = \frac{1}{\frac{T - 2Ta}{T}} \tag{5}$$

When G: boosting factor, T_a : turns on time period, and T: total time period.

The group L-C is required to equal C2=C1 and L1=L2 and based on these values the amount of voltage produced by the system is determined. In this system to produce 5-level of output voltage we connect in sequence two cells with a network and a direct current source, and based on this new system, the generated output is twice as large as the applied voltage and much larger. Figure 3 shows three-phase 5 level z-source cascaded type h-bridge inverter.



Figure 3. Three-phase 5 level z-source cascaded type h-bridge inverter

3. SOME MULTI-LEVEL INVERTER CONTROL ALGORITHMS

3.1. Conventional SVM

Most of the conventional SVM algorithm depends on the number of levels, this means that when the number of levels changes, the SVM algorithm changes as well. Here we will look at the five-level SVM algorithm, Projection of the vectors on $\alpha\beta$ coordinates forms a four-layer hexagon centered at the origin of the $\alpha\beta$ plane as shown in Figure 4, and zero-voltage vectors are located at the origin of the plane. Where we find that it contains 125 switching-state vectors results in 61 voltage space vectors. And by passing to the N-level, the relationship becomes:

$$n_{switching-state} = N^3 \tag{6}$$

$$N_{vectors} = 1 + 6\sum_{i=1}^{N-1} i$$
(7)



Figure 4. Space voltage vectors for a five-level inverter

3.2. Definition of the space vector place

The space vector place is defined in two steps [16]–[25]: The first step defines the sector number of where the vector lies. The second step defines the triangle in which the vector lies. Finally, we apply simple calculations to derive the final control signal, depending on the type of topology used.

3.3. Improved algorithm of vector modulation principle

Since the operation of each phase can be represented by a single pole and N switch states, it is clear that the switching states (combination of phase switches) represented by a single vector, produce single three phase, phase to phase voltages defined by formula (15) these can be represented by victors in three-dimensional Euclidean space:

$$V_{\rm S} = \begin{bmatrix} V_{ab} & V_{bc} & V_{ca} \end{bmatrix}^{\prime} \tag{8}$$

The switchers of phases a, b and care linked respectively to the, output states i, j and k, where $i, j, k \in [0, N - 1]$. Communication vectors \vec{v}_s of which modifications are produced during changes in the different possible state. Configurations, it is given by the following general expression formula:

$$\vec{v}_{s}(ijk) = U \cdot [i-j \quad j-k \quad k-i]^{T}$$
(9)

For example, switch states (214, 103) for a 5-level inverter produce the same space vector (switching vector)

$$\vec{v}_s(214) = U \cdot [2 - 1 \quad 1 - 4 \quad 4 - 2]^T = U \cdot [-1 \quad -3 \quad 2]^T$$
(10)

$$\vec{v}_s(103) = U \cdot [1 - 0 \quad 0 - 3 \quad 3 - 1]^T = U \cdot [-1 \quad -3 \quad 2]^T \tag{11}$$

This multi-level inverter control algorithm depends on the coordinates between phases j_a , j_b and j_c in (12) as shown in Figure 5. We note that the representation of the switching vectors in the coordinates between phases is simple and general to represent the hexagonal structure of any multi-level inverter, and we were working with the two-level inverter. With this algorithm the calculation of the switching vector and the conduction times of vectors will be simpler than those of the conventional method.

$$\begin{cases} U_{ja} = U_{a} - U_{b} \\ U_{jb} = U_{b} - U_{c} \\ U_{jc} = U_{c} - U_{a} \end{cases}$$
(12)



Figure 5. Inverter model in the coordinate between phases

3.4. Algorithm step

Coordinate transformation:

The first step in the algorithm is to transform the reference vector V_{ref} into the coordinate between Phases $(V_{ab} \quad V_{bc} \quad V_{ca})$ and we multiply by (13).

$$\frac{N-1}{sqrt(3)}$$
(13)

With:

$$V_{ref} = \begin{bmatrix} V_{an} \\ V_{bn} \\ V_{cn} \end{bmatrix} = M \begin{bmatrix} \sin(\omega t) \\ \sin(\omega t - 2\pi/3) \\ \sin(\omega t + 2\pi/3) \end{bmatrix}$$
(14)
$$M \in \begin{bmatrix} 0 & 1 \end{bmatrix}$$
(15)

Since the work is done in an open circuit, we choose M = 1

Detection of the three closest vectors and calculation of switch switching times:

Switch vectors have integer coordinates: The vectors closest to the reference vector can be identified quite simply, their coordinates are combinations of rounded values greater and less than the number of the reference vector.

$$f_{ab} = floor(V_{rab}) \qquad c_{ab} = ceil(V_{rab})$$

$$f_{bc} = floor(V_{rbc}) \qquad c_{bc} = ceil(V_{rbc})$$

$$f_{ca} = floor(V_{rca}) \qquad c_{ca} = ceil(V_{rca})$$
(16)

With: Floor: indicates the lower rounded value of V_{ref} ; and Ceil: indicates the upper rounded value of V_{ref} . The closest vectors can be found by evaluating the value of the expression:

$$f_{ab} + f_{bc} + f_{ca} \tag{17}$$

Once the three closest vectors are identified, the switching times of the switches (d1, d2 and d3) can be found by solving the following two equations.

$$V_{ref} = d_1 \cdot V_1 + d_2 \cdot V_2 + d_3 \cdot V_3 \tag{18}$$

$$d_1 + d_2 + d_3 = 1 \tag{19}$$

Si
$$f_{ab} + f_{bc} + f_{ca} = -1$$

 $V_1 = V_{ffc} = (f_{ab} \quad f_{bc} \quad c_{ca})^T$
 $V_2 = V_{cff} = (c_{ab} \quad f_{bc} \quad f_{ca})^T$
 $d_1 = V_{rca} - f_{ca}$
 $d_2 = V_{rab} - f_{ab}$
 $V_3 = V_{fcf} = (f_{ab} \quad c_{bc} \quad f_{ca})^T$
 $d_3 = V_{rbc} - f_{bc}$
(20)

Si
$$f_{ab} + f_{bc} + f_{ca} \neq -1$$

 $V_1 = V_{fcc} = (f_{ab} \quad c_{bc} \quad c_{ca})^T$
 $V_2 = V_{ccf} = (c_{ab} \quad c_{bc} \quad f_{ca})^T$
 $d_1 = f_{ab} - V_{rab}$
 $d_2 = f_{ca} - V_{rca}$
 $V_3 = V_{cfc} = (c_{ab} \quad f_{bc} \quad c_{ca})^T$
 $d_3 = c_{bc} - V_{rbc}$
(21)

Determination of switching states: This step requires the conversion from the two-dimensional coordinates" the coordinate between Phases" to the three-dimensional coordinates, meaning obtaining the original coordinates from which the ray was generated. All switching states of a switching vector will satisfy the expression: For example, $\vec{V} = [f_{ab} \quad c_{bc} \quad f_{ca}]$ To find out the number of switching vector resulting from the switching vector \vec{V} , we apply the relationship:

$$\begin{aligned} a_s &= N - max(abs(f_{ab}), abs(c_{bc}), abs(f_{ca})) \\ N: number of levels \\ a_s: The number of switching states \\ a_s &\in [0, N-1] \end{aligned}$$
(22)

From a_s , we deduce the voltage level of phase-leg a. For example, When the voltage level of phase-leg a of switching vector \vec{V} is a_s , the voltage level of phase-leg b is, $b_s = a_s - f_{ab}$, the voltage level of phase-leg c is $c_s = a_s + f_{ca}$. For example, the switching vector $\begin{bmatrix} 0 & 3 & -3 \end{bmatrix}$ of 5-level inverter, when applying the relationship (5), we find, $a_s = 2$ By applying some simple calculations, we find the voltage level of phase - leg a = 4. The switching states for $\begin{bmatrix} 0 & 3 & -3 \end{bmatrix}$ are $\begin{bmatrix} 4 & 4 & 1 \end{bmatrix}$ and $\begin{bmatrix} 3 & 0 \end{bmatrix}$ to check. Thus, we have determined the triangle in which V is located and the times of each ray.

5. RESULTS AND DISCUSSION

The MATLAB simulations verify the effectiveness of the proposed structure and control. The results for various control algorithms are displayed and compared. System information is displayed in the Table 1. The study was conducted on two types of control techniques, SPWM and improved SVM, shown in Figure 6, and Figure 7 respectively. The Z-source network output gave almost twice the voltage of the input. In terms of the output current THD, it was reduced to 1.05% compared to the current methods with a THD level of 1.89% for SPWM technology and a level of THD of 1.59% after we added it to the Z-source network. As for the calculations, it has been simplified compared to the conventional SVM. Figure 8 shows a comparison between the proposed system and the conventional system.



Figure 6. Technique control (SPWM), (a) the intensity of the output voltage between the two ends of a Z-source network in two solutions (shoot through and non-shoot through), (b) output current, and (c) total harmonic distortion (THD) analysis output current



Figure 7. Technique control conventional SVM, (a) the intensity of the output voltage between the two ends of a Z-source network in two solutions (shoot through and non-shoot through), (b) output current, and (c) THD analysis output current



Figure 8. Comparison between the proposed system and the conventional system

6. CONCLUSION

This paper demonstrates simulation results of a five-level Z-source inverter using an improved algorithm SVM. He was examining this system and its results. The efficiency and shape of the signal has been improved by applying the improved algorithm SVM. The new algorithm SVM simplifies calculations

and makes handling the multi-level inverter as easy as working with the two-level inverter. System as a group, multi-level Z-source inverter and improved algorithm SVM for controlling the power switches of the system, gives output voltage twice the constant voltage applied at the input and the harmonic content level in the system also reduce, and voltage stress in the power switches also abridged. The work done achieved THD for the output current of 1.05% it meets IEEE standard. This will extend the work by implementing this work as a real-world experiment and the development of the algorithm and applying the improved algorithm to modular multi-level converter (MMC).

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