International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 13, No. 4, December 2022, pp. 2181~2189
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v13.i4.pp2181-2189

A synchronization technique for single-phase grid applications

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Article Info

Article history:

Received Jun 26, 2022
Revised Aug 23, 2022
Accepted Sep 15, 2022

Keywords:

DC offset rejection
Harmonic rejection
Orthogonal signal generation
Phase-locked loop
Time-delay phase locked loop

ABSTRACT

The utility grid disturbances like DC offset and harmonic components can severely affect the estimated variables from the phase-locked loop (PLL), resulting in poor performance of the system relying on it. Therefore, there is an emerging need for well-designed PLL algorithms ensuring robust response against different operating conditions. This paper proposes a simple single-phase PLL algorithm with inherent DC offset and specific harmonic orders rejection capability. Utilizing adaptive time-delay fictitious signal generation. A full mathematical model of the proposed PLL has been provided. The proposed PLL is compared with other filter-based single-phase PLLs, to validate its simplicity and excellent performance.

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1. INTRODUCTION

The major improvements in the power electronics field have brought new applications in power generation and storing technologies, reshaping the conventional utility power grid. Traditionally the power grid was a hierarchical unidirectional system; composed of bulk generation units, feeding distributed loads passively [1]. Nowadays, distributed generation units (DGs) and smart grids (SGs) are rapidly taking place in the power grid, as they maximize the benefits of the renewable energy-based generation systems (RESs) and allow active operation and management of power resources [2].

However, there are serious technical challenges to the reliable and efficient operation of the described active grid; these challenges arise from the fluctuated nature of RESs and the conditions of the grid signal, which can affect the power quality and the dynamic stability of the overall system. Consequently, there is a need for well-designed control systems to ensure smooth operation under different scenarios [3]–[5]. An essential part of any control scheme is the synchronization system, responsible for detecting the grid signal parameters (amplitude, frequency, and phase) to be used in the control process. For this purpose, there are different techniques discussed in the literature which can be classified into; filtering based techniques (such as, Fourier transform filter, Kalman filter, moving average filter (MAF), and notch filters), zero-crossing detection based -techniques (ZCD), frequency-locked loop (FLL), and phase-locked loop (PLL) [4]–[15].

The PLL is the most commonly used technique because of its simple implementation and superior dynamic performance over the other techniques. In general, the PLL is a non-linear system composed of three main parts; a phase detector (PD) which is responsible for generating the error signal that is proportional to the signal's frequency, loop filter (LF) commonly a PID controller, used to minimize the error and determines the dynamics of the PLL, and a voltage-controlled oscillator which reproduces the estimated signal [16].

In three-phase applications, the synchronous reference frame PLL (SRF-PLL) is considered the prevalent type, where the PD is a simple Park transformation that generates an error signal (phase difference), then a PID controller forces this error to zero resulting in phase locking between the input signal and the direct component (d-axes). In single-phase applications, there are two main classes distinguished by their phase detectors, the first class is power based PLLs (p-PLLs); which have product type phase detector, and the second class is quadrature signal generation PLLs (QSG-PLLs), which employs the conventional SRF-PLL by producing fictitious orthogonal signal along with Clark transformation [17]. The latter has the advantage of a flexible phase detector which can be modeled mathematically in many ways to deal with different operation conditions. A well-known example is the conventional time delay PLL (TD-PLL), where a delay operator (of Tn/4, Tn: fundamental period) is used to generate the fictitious signal, followed by the Clark transformation block, then the output enters the conventional SRF-PLL, in this type of PLL the signal is assumed to be a pure signal with no disturbances [18]. In practice, disturbances (harmonics, DC injections) in utility grid voltage signals are inevitable; it is a byproduct of the expanding use of renewable energy sources and associated power converter interfaces. The DC components are imposed in the signal by grid faults [19], (A/D) conversions [20], measurement devices [21], DC injections from DGs [22], and half-wave rectification [23]; moreover, the harmonic components are mainly brought to the grid voltage signal by the power converter (PC) interfaces. As a result, fundamental frequency oscillations and offset errors appear on PLL output [24], leading to instability issues in the control system of the PCs and violations of the standard recommended injected current [25], determined by IEC 61727-2004 [26] and IEE 1547-2004 [27] standards.

Extensive work has been done in the literature to eliminate the disturbances imposed on the grid signal. There are mainly two approaches to achieve good elimination capability, the first, using pre-loop and in-loop filters. Golestan *et al.* [28] modified the conventional TD-PLL discussed in Golestan *et al.* [29] by applying a pre-loop MAF filter, which can eliminate the DC-injection and higher order harmonics with proper tuning of the MAF window length. However, due to complex frequency-adaptive implementation, this approach suffers from complexity when frequency drifts occur. Gautam *et al.* [30] presented an improvement on the same idea; this time, two in-loop MAFs have been used along with a phase lead compensator (PLC); the resultant comb-filter has the advantages of an excellent elimination capability and overcomes the problem of slow dynamic performance of the original MAF based technique. Liu *et al.* [31] presented a single-phase PLL based on second order generalized integrator (SOGI) along with all-pass filter. Despite the excellent rejection capability, this structure has a slow dynamic response. The second approach to deal with the impurities of the grid signal, using the delay signal cancellation (DSC) concept. A delayed version of the contaminated signal is produced, then the DC-injection can be removed by simple subtraction. Smadi and Fawaz [32] presented a simple single-phase PLL structure, with the same idea, using two delay operators; one of arbitrary length used to remove the DC offset before entering the loop, the other is of one fourth the nominal grid period to generate the orthogonal signal needed for Park's transformation.

This paper proposes a simple single-phase PLL with inherent DC offset rejection capability. The idea of a balanced three phase set is used to estimate the DC-injection, then remove it using simple subtraction. Besides, the proposed structure has the advantage of modularity with the conventional harmonics elimination techniques developed in the three-phase PLLs. The structure of the paper is as follows: section 2 introduces a full analysis of the proposed method. In section 3, simulation results and performance comparison with other single-phase PLL have been proposed. Finally, the concluding remarks are summarized in section 4.

2. THE PROPOSED PLL STRUCTURE

2.1. Mathematical model of the proposed PLL

Figure 1 shows a schematic diagram for the proposed technique. The grid voltage signal is assumed to be contaminated with DC offset. The DC offset elimination block comprises two-time delay operators with ($T/3$ and $2T/3$) lengths estimated from the loop PLL. Here, the time delay lengths are restricted to these values as the DC offset estimation essentially depends on creating a set of balanced three phasors. The mathematical representation of the DC offset elimination block can be given by (1).

$$\begin{aligned} v_a &= v_g = v_m \cos(\omega_g t + \phi) + V_{dc} \\ v_b &= v_g(t - \tau_B) = v_m \cos(\omega_g (t - \tau_B) + \phi) + V_{dc} \\ v_c &= v_g(t - \tau_C) = v_m \cos(\omega_g (t - \tau_C) + \phi) + V_{dc} \end{aligned} \quad (1)$$

where v_m is the voltage magnitude, V_{dc} is the DC offset imposed on the signal, ($\omega_g = 2\pi f_g$) is the nominal angular frequency, ϕ is the phase angle, ($\theta = \omega_g t + \phi$), and ($\tau_B$ and τ_C) are adaptively extracted time delay lengths. At steady-state, (1) represents a set of balanced three phasors, then the estimated DC offset value can be represented as:

$$\hat{V}_{dc} = \frac{v_m}{3}\underbrace{\left(\cos(\theta) + \cos\left(\theta - \frac{2\pi}{3}\frac{\hat{T}}{T_n}\right) + \cos\left(\theta - \frac{4\pi}{3}\frac{\hat{T}}{T_n}\right)\right)}_{=0} + \frac{3V_{dc}}{3} \quad (2)$$

where $\hat{T}$, is the estimated time period from the loop, and T_n is the nominal period of the grid signal. The first term in (2) will diminish to zero, leaving the estimated DC offset equal to the real one. A simple subtraction is then used to eliminate the DC value from the original three-phase set before entering the PLL, resulting in:

$$\begin{aligned}
\hat{v}_a &= v_a - \hat{v}_{dc} = \frac{v_m}{3}\left(2\cos(\theta) - \cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g\tau_C\right)\right) \\
\hat{v}_b &= v_b - \hat{v}_{dc} = \frac{v_m}{3}\left(-\cos(\theta) + 2\cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g\tau_C\right)\right) \\
\hat{v}_c &= v_c - \hat{v}_{dc} = \frac{v_m}{3}\left(-\cos(\theta) - \cos\left(\theta - \omega_g\tau_B\right) + 2\cos\left(\theta - \omega_g\tau_C\right)\right)
\end{aligned} \quad (3)$$

Before entering the PLL, Clark's and Park's transformations are applied, and the general form for both are given in the following equations:

$$\begin{bmatrix}\hat{v}_\alpha \\ \hat{v}_\beta\end{bmatrix} = \begin{bmatrix}\frac{2}{3} & -\frac{1}{3} & -\frac{1}{3} \\ 0 & \frac{1}{\sqrt{3}} & -\frac{1}{\sqrt{3}}\end{bmatrix}\begin{bmatrix}\hat{v}_a \\ \hat{v}_b \\ \hat{v}_c\end{bmatrix} \quad (4)$$

$$\begin{bmatrix}\hat{v}_d \\ \hat{v}_q\end{bmatrix} = \begin{bmatrix}\cos(\hat{\theta}) & \sin(\hat{\theta}) \\ -\sin(\hat{\theta}) & \cos(\hat{\theta})\end{bmatrix}\begin{bmatrix}\hat{v}_\alpha \\ \hat{v}_\beta\end{bmatrix} \quad (5)$$

$$\begin{aligned}
\hat{v}_d = {} & \frac{v_m}{3}\cos(\hat{\theta})\left(2\cos(\theta) - \cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g\tau_C\right)\right) \\
& + \frac{v_m}{\sqrt{3}}\sin(\hat{\theta})\left(\cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g.\tau_C\right)\right)
\end{aligned} \quad (6)$$

$$\begin{aligned}
\hat{v}_q = {} & -\frac{v_m}{3}\sin(\hat{\theta})\left(2\cos(\theta) - \cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g\tau_C\right)\right) \\
& + \frac{v_m}{\sqrt{3}}\cos(\hat{\theta})\left(\cos\left(\theta - \omega_g\tau_B\right) - \cos\left(\theta - \omega_g\tau_C\right)\right)
\end{aligned} \quad (7)$$

where, ($\hat{v}_\alpha$, $\hat{v}_\beta$) are the resultant fixed frame components, ($\hat{v}_d$, $\hat{v}_q$) are the resultant rotating reference frame components. (θ,$\hat{\theta}$) are the actual and estimated angles, respectively.

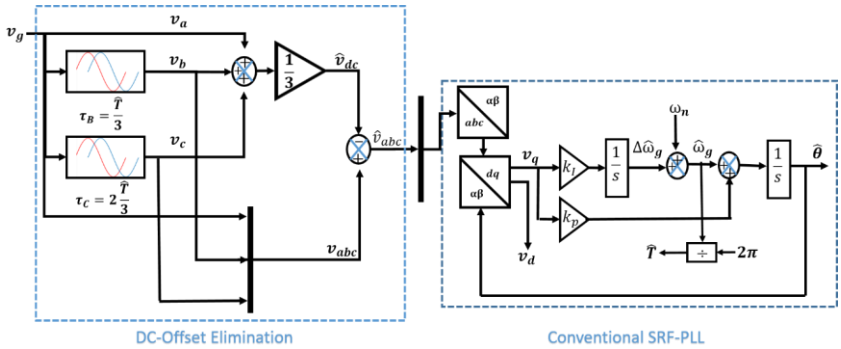

Figure 1. The proposed single-phase PLL

The last two equations can be used to extract the small-signal model of the proposed structure, which helps in designing the loop-filter gains used in the PLL. For this purpose, first we apply the trigonometric identities in (8) when necessary to simplify the equations, then linearize the non-linear terms, following the linear approximation assumptions for the (cos, sin) functions; $\cos(\Delta) \cong 1$, and $\sin(\Delta) \cong \Delta$, and Taylor's series expansion for the non-linear terms ($\omega_g\tau_B$), and ($\omega_g\tau_C$) in [33].

$$\begin{aligned}
&\sin(a)\cos(b) = \frac{1}{2}(\sin(a+b) + \sin(a-b)) \\
&\cos(a)\cos(b) = \frac{1}{2}(\cos(a+b) + \cos(a-b)) \\
&\sin(a+b) = \sin(a)\cos(b) + \cos(a)\sin(b) \\
&\sin(a-b) = \sin(a)\cos(b) - \cos(a)\sin(b)
\end{aligned}$$

$$\cos(a+b) = \cos(a)\cos(b) - \sin(a)\sin(b)$$
$$\cos(a-b) = \cos(a)\cos(b) + \sin(a)\sin(b) \quad (8)$$

The resulting equations can be given as:

$$\hat{v}_d = v_m \overbrace{\left(-\sin(\hat{\theta}+\theta)\left[\frac{T}{6}(\Delta\omega_g - \Delta\hat{\omega}_g)\right] - \cos(\hat{\theta}+\theta)\left[\frac{\sqrt{3}T}{18}(\Delta\omega_g - \Delta\hat{\omega}_g)\right]\right)}^{D(t)}$$
$$+v_m \overbrace{-\frac{Tv_m}{3}(\Delta\omega_g - \Delta\hat{\omega}_g)(\Delta\hat{\theta} - \Delta\theta)}^{N(t)} \quad (9)$$
$$\hat{v}_q = v_m \overbrace{\left(\sin(\hat{\theta}+\theta)\left[\frac{\sqrt{3}}{6}.\frac{T}{3}(\Delta\omega_g - \Delta\hat{\omega}_g)\right]\right) - \cos(\hat{\theta}+\theta)\left[\frac{T}{6}(\Delta\omega_g - \Delta\hat{\omega}_g)\right]}^{D(t)}$$
$$-v_m\left(\frac{T}{3}(\Delta\omega_g - \Delta\hat{\omega}_g) - (\Delta\hat{\theta} - \Delta\theta)\right)$$

where ($\Delta\omega_g$, $\Delta\hat{\omega}_g$) are the actual and estimated frequency variations. The double frequency term appearing in both components will diminish to zero as the steady-state occurs, where ($\Delta\omega_g = \Delta\hat{\omega}_g$), so it can be dropped from the equations. For the direct component $(N(t))$, will also reach zero in steady-state. The steady-state representation can then be approximated to:

$$\hat{v}_d = v_m$$
$$\hat{v}_q = -v_m\left(\frac{T}{3}(\Delta\omega_g - \Delta\hat{\omega}_g) - (\Delta\hat{\theta} - \Delta\theta)\right) \quad (10)$$

The small-signal model can be deduced from the quadrature component as follows:

$$\hat{v}_q = v_m\left(\frac{3\Delta\theta - \Delta\omega_g T}{3} - \Delta\hat{\theta} - \frac{\Delta\hat{\omega}_g T}{3}\right)$$
$$\overrightarrow{Laplace\ Transfrom}: \hat{v}_q(s) = v_m\left(\frac{(2+e^{-Ts})}{3}\Delta\theta\right) - \Delta\hat{\theta}(s) + \Delta\hat{\omega}_g(s)\frac{T}{3} \quad (11)$$

Figure 2 shows a block-diagram of the small-signal model presented in (11). From the last figure, the closed-loop transfer function can be given as:

$$\frac{\Delta\hat{\theta}}{\Delta\theta}(s) = \frac{2+e^{-TS}}{3}\frac{K_p s + K_i}{s^2 + v_m\left(K_p - K_i\frac{T}{3}\right)s + v_m K_i} \quad (12)$$

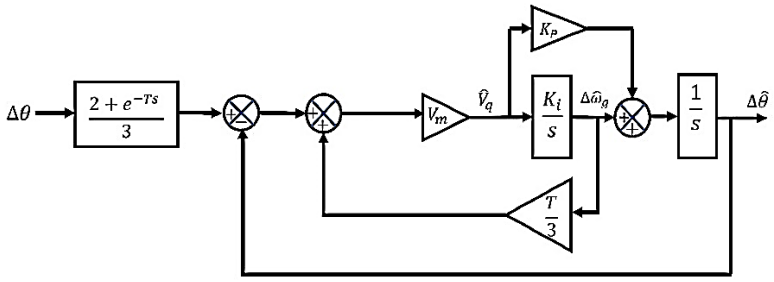

Figure 2. Small-signal model of the proposed structure

This transfer function has a second-order characteristic equation so that the loop gains can be tuned by proper selection of the natural frequency (ω_n), and the damping ratio (ς), setting:

$$2.\varsigma.\omega_n = v_m\left(K_p - K_i\frac{T}{3}\right)$$
$$\omega_n^2 = v_m K_i \quad (13)$$

where (T) is the nominal period of the grid signal and is assumed to be (T=0.02s), (v_m=1 p.u) because of the normalization using division ($V_q = \hat{V}_q/\hat{V}_d$), or inverse tangent function. A typical value of the damping factor is (ς = 0.707), and the natural frequency (ω_n = 40π rad/s), yields; (K_p = 282.96, and K_i = 15791.36). to validate

the accuracy of the small-signal model, a phase-jump of ($\Delta\theta = 20^0$) is applied to the actual PLL and the small-signal model and the results are shown in Figure 3.

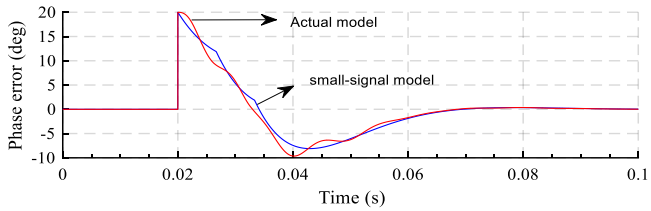

Figure 3. Small-signal model validation

2.2. Harmonic elimination in the proposed PLL

The harmonic rejection capability of the proposed PLL can be spotted from Figure 1; assuming that the grid voltage signal is harmonically distorted (1) can be rewritten as:

$$\begin{aligned} v_a &= v_g = V_{m1}\cos(\omega_g t + \phi_1) + \textstyle\sum_h V_{mh}\cos(h\omega_g t + \phi_h) + V_{dc} \\ v_b &= v_g(t-\tau_B) = V_{m1}\cos(\omega_g(t-\tau_B) + \phi_1) + \textstyle\sum_h V_{mh}\cos(h\omega_g(t-\tau_B) + \phi_h) + V_{dc} \\ v_c &= v_g(t-\tau_C) = V_{m1}\cos(\omega_g(t-\tau_C) + \phi_1) + \textstyle\sum_h V_{mh}\cos(h\omega_g(t-\tau_C) + \phi_h) + V_{dc} \end{aligned} \quad (14)$$

where V_{m1}, ϕ_1 are the fundamental voltage magnitude and phase angle, h, V_{mh}, and ϕ_h are the harmonic order, the h[th] harmonic magnitude, and phase angle, respectively. $\theta_1 = \omega_g t + \phi_1$, and $\theta_h = h\omega_g t + \phi_h$. The estimated DC offset in (2) becomes:

$$\begin{aligned} \hat{V}_{dc} = \tfrac{V_{m1}}{3}\left(\cos(\theta_1) + \cos\left(\theta_1 - \tfrac{2\pi}{3}\tfrac{\hat{T}}{T_n}\right) + \cos\left(\theta - \tfrac{4\pi}{3}\tfrac{\hat{T}}{T_n}\right)\right) \\ + \tfrac{1}{3}\textstyle\sum_h V_{mh}[\cos(\theta_h) + \cos\left(\theta_h - h\tfrac{2\pi}{3}\tfrac{\hat{T}}{T_n}\right) + \cos\left(\theta_h - h\tfrac{4\pi}{3}\tfrac{\hat{T}}{T_n}\right)] + V_{dc} \end{aligned} \quad (15)$$

Using (3), (14) and (15), the estimated DC-free voltage can be observed through only one phase as follows:

$$\begin{aligned} \hat{v}_a = V_{m_1}\cos(\theta_1) - \underbrace{\tfrac{V_{m_1}}{3}\left(\cos(\theta_1) + \cos\left(\theta_1 - \tfrac{2\pi}{3}\tfrac{\hat{T}}{T_n}\right) + \cos\left(\theta - \tfrac{4\pi}{3}\tfrac{\hat{T}}{T_n}\right)\right)}_{\cong 0\ ;\text{near synchronization}} + \\ \underbrace{\tfrac{1}{3}\textstyle\sum_h V_{mh}\left(2\cos(\theta_h) - \cos\left(\theta_h - h\tfrac{2\pi}{3}\tfrac{\hat{T}}{T_n}\right) - \cos\left(\theta_h - h\tfrac{4\pi}{3}\tfrac{\hat{T}}{T_n}\right)\right)}_{\text{Harmonics}} \end{aligned} \quad (16)$$

Reaching the steady-state (i.e. $\hat{T} \cong T_n$), the second, and the last terms in (16) reach zero, leaving the DC-free phase representation ($V_{m_1}\cos(\theta_1)$), and the harmonic term. The harmonic term can be decomposed to:

$$\begin{aligned} \text{Harmonics} = \cos(\theta_h)\left(2 - \cos\left(h\frac{2\pi}{3}\frac{\hat{T}}{T_n}\right) - \cos\left(h\frac{4\pi}{3}\frac{\hat{T}}{T_n}\right)\right) \\ - \sin(\theta_h)\left(\sin\left(h\tfrac{2\pi}{3}\tfrac{\hat{T}}{T_n}\right) + \sin\left(h\tfrac{4\pi}{3}\tfrac{\hat{T}}{T_n}\right)\right) \end{aligned} \quad (17)$$

The harmonic order in which the terms cancel each other can be extracted from: $\cos\left(h\frac{2\pi}{3}\right) = \cos\left(\frac{4\pi h}{3}\right) = 1$, and $\sin\left(\frac{2\pi h}{3}\right) = \sin\left(\frac{4\pi h}{3}\right) = 0$, which are satisfied if and only if $h = 3k, k = 1,2,3\ldots$. Therefore, the triplen harmonics in the grid voltage are canceled out of the box without extra cost or burden. Hence, the proposed PLL structure is inherently immune to the DC offset and the triplen-harmonics. The same analysis can be applied to the other phases resulting in a set of harmonic-free balanced three phase voltages.

3. RESULTS AND DISCUSSION

3.1. Simulation results

In this section, the dynamic performance of the proposed PLL has been tested numerically under two different operational scenarios. The 2% settling time criterion is used to assess the dynamic response, and the results are shown in Figures 4 to 6 and summarized in Table 1. The first scenario: a contaminated grid signal with (0.15 p.u) DC offset, and triplen harmonic components of (0.05 p.u for 3[rd],6[th],9[th],12[th]), resulting in 10% THD. At 0.1 sec a voltage amplitude reduction of 0.2 p.u is applied, then returned to 1p.u at 0.2 sec. a phase-

jump of 20° is applied at 0.3 sec, and finally, the DC offset is removed at 0.4 sec. The grid voltage is shown in Figure 4, and the results are shown in Figure 5. The second scenario: a DC offset of 0.15 p.u is initially imposed on the signal, a frequency-jump of +3Hz at 0.1 sec is applied. The frequency returned to its nominal at 0.2 sec, and the DC offset was removed at 0.3 sec; no harmonic components were imposed during this test. The results are shown in Figure 6.

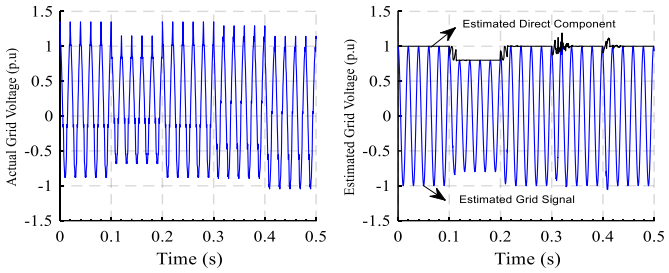

Figure 4. Grid voltage under the first scenario

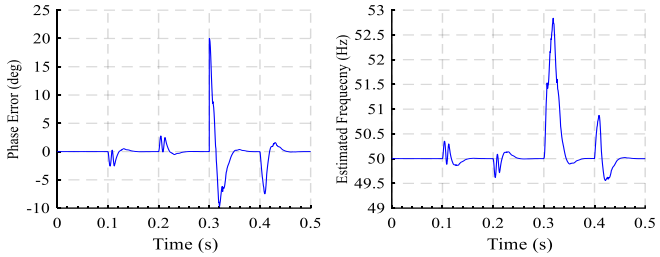

Figure 5. Estimated frequency and phase-error under the first scenario

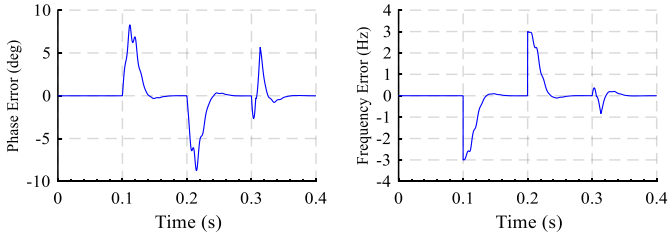

Figure 6. Estimated phase and frequency errors under the second test

Table 1. Simulation results

Disturbance		Amplitude Jump of (±0.2p.u)	Phase-jump Of (+20°)	Frequency-jump Of (±3Hz)	DC offset of 0.15 p.u Imposing (or removal)	THD of (10% Of the grid voltage
Test (1)	Phase settling time	34 ms with a maximum overshoot of ±2°	45 ms with phase swing (20°) -(-10°)	–	38 ms with a maximum overshoot of ±7°.	THD of the estimated voltage 0.01%
	Amplitude settling time	13 ms with a maximum overshoot of 0.79 p.u	38 ms with a maximum overshoot of 1.12 p.u	–	40 ms with a maximum overshoot of 1.2 p.u	
Test (2)	Phase settling time	–	–	38 ms with a maximum overshoot of ±8°	39 ms with a maximum overshoot of +6°	–
	Frequency settling time	–	–	34 ms	32 ms with maximum overshoot less than 1Hz	–

3.2. Performance comparison with other single-phase PLLS

In this section, the dynamic performance of the proposed PLL is compared with three PLL structures proposed in [30], [34], and [35]; the first one is the conventional non frequency dependent time-delay PLL (NTD-PLL), the second structure employs an in-loop MAF filter in the NTD-PLL to eliminate the DC offset and harmonic components from the grid signal the third structure uses a comb-filter of MAF and PLC to enhance the speed of response of the previous one. Three tests have been conducted with different operation scenarios.

Test 1: a phase-jump of 20º, with normal operating conditions. The results are shown in Figure 7.
Test 2: a frequency-jump of +3Hz, with normal operating conditions. The results are shown in Figure 8.
Test 3: a phase-jump of 20°, with the presence of 0.04 p.u DC offset and the same harmonics components in the first scenario. The results are shown in Figure 9.

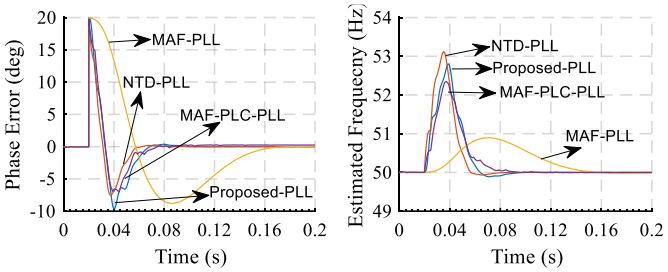

Figure 7. Comparison under Test 1

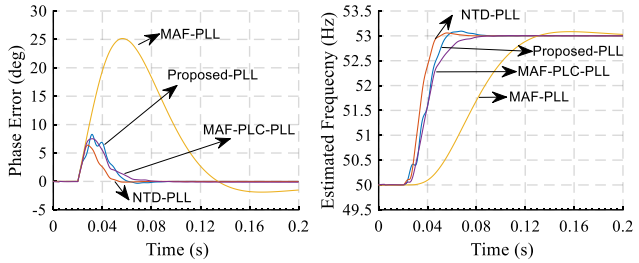

Figure 8. Comparison under Test 2

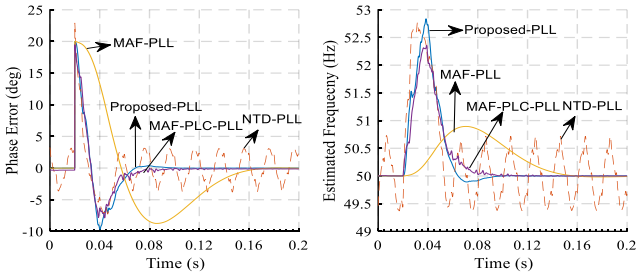

Figure 9. Comparison under Test 3

3.3. Discussion

Under the first test, the proposed PLL has (45 ms) phase settling time and a peak frequency of (52.7 Hz); the remaining structures have (36 ms, 53.1 Hz) for the NTD-PLL, (132 ms, 50.8 Hz) for the MAF-PLL, and (4 ms, 52.3 Hz) for the MAF-PLC-PLL. Under the second test, the readings are (34ms frequency settling time, 7º peak phase angle), (29 ms, 5.5º), (103 ms, 25.1º), (46 ms, 6.3º) respectively, the third test has the same readings as the first one, noticing that the conventional NTD-PLL does not have a rejection technique for the DC offset nor the harmonics. Therefore, the harmonic analysis was only conducted for the other structures resulting in a total harmonic distortion (THD) of 0.01% for the proposed PLL and less than 0.01% for the MAF-PLL and MAF-PLC-PLL. The results of the previous tests show that the proposed PLL has a competitive performance with other advanced structures, with the advantage of simple implementation, unlike the filter-based technique. Although the harmonic rejection is limited only to the triplen harmonics in the

proposed method, unlike the structures in [30] and [34], it can be easily improved by employing an additional pre-filtering stage for the remaining significant harmonic orders.

4. CONCLUSION

This paper uses a simple single-phase PLL with inherent DC offset and triplen harmonic rejection capability, utilizing two time-delay operators only. The proposed orthogonal signal generation provides a modulus PLL with the well-studied three-phase PLL filtering techniques making the elimination of the other significant harmonic orders an easy task. Full mathematical derivation has been provided through this paper, along with comparisons simulation study with advanced PLL algorithms proving the excellent response of the proposed PLL.

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