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An advanced LVRT controlled DSCC-STATCOM for reactive power compensation

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ABSTRACT

This article focuses on the control of STATCOM for the improvement of reactive power compensation during grid faults and unbalanced load. The problem encountered with convectional voltage source converter based STATCOM for reactive power management and capacitor voltage balancing during grid faults are analyzed and its operational limitations are studied. To remove the above problems, an adaptive low voltage ride through control technique based modular double star cascaded converter (DSCC) STATCOM is proposed. In this dynamic control, the positive reactive currents and negative reactive currents are separately controlled for reactive power management and a zero (Vo) sequence voltage is inserted for the management of active power. This advanced control method effectively balances the submodule capacitor voltage within its prescribed limits by managing the equal distribution of active power between converter legs and provides dynamic reactive power management during grid faults. The effectiveness of the DSCC-STATCOM, with proposed control method is verified using MATLAB/Simulink software-based simulations under single line to ground fault and unbalanced load.

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1. INTRODUCTION

With the increasing demand of better power supply and voltage stability, modern power systems are turning very complex. The sudden surge in demand of single-phase loads, smart energy efficient devices, induction motor drives, make the power system more vulnerable to faults. Also, with the integration of present renewable energy sources like wind and solar, the power system stability problems are increasing and this may lead to the cause of frequent faults at the load end. The faults cause voltage instability and this needs dynamic reactive power compensation. Voltage source converter (VSC) based convectional STATCOMs are used to support power system for providing reactive support, but present STATCOM are not sufficient in fulfilling requirement of reactive support under grid faults. To overcome from these problem recent modular multilevel converters are gaining attention [1]–[3]. These modular STATCOM configuration have high Mvar ratings and have several advantages over classical VSC based STATCOMs like high voltage configurations with low rated semiconductor devices, easily scalable to high voltages, lower switching losses and have lower weight and volume as compared to conventional converters [4], [5].

The modular multilevel converter (MMC) converter is comprised of several dc side submodules and during compensation these submodule switches takes real power from the grid to recover its internal losses [6].

The compensation of reactive power during grid faults causes unequal distribution of real power among the converters legs and this leads to the unbalancing of capacitors in submodules which considerably effects the dynamic reactive power management of the system. Several researches have focused in the improvement of control mechanism for MMC STATCOM for dynamic reactive power compensation during asymmetrical grid faults and unbalancing of capacitor voltages. Several techniques are addressed for dynamic reactive power management by balancing the capacitor voltages. Huber and Korn [7] the sub-module selection-based scheme is implemented in which most suitable module depending on the polarity is selected. A control mechanism is adapted to generate switching pulses reduces the unequal distribution of power among switches, which results in individual balancing of capacitor voltage. However, this method leads to the increased frequency and internal losses inside converter. Another method [8], [9] implementing a staircase modulation technique to generate pulses is proposed, in which all submodules are switched in a manner to charge their individual capacitors in every fundamental period by equalizing the switching frequency equal to the fundamental frequency. This method manages to maintain the capacitor voltages but in turn leads to the output voltage distortion when dealing with smaller submodules. Some hardware-based methods are also proposed which are effective in handling the reactive power compensation during faults and manages capacitor balancing but it increases the complexity of the circuit and requires extra oversized components, which indirectly increases the cost [10]–[12]. On the basis mentioned control techniques for reactive power management and capacitor voltage balancing it is analyzed that the control of MMC STATCOM during grid faults requires an adaptive control mechanism to manage stability of voltage supply during fault without the use of overrated switches and complex control method [13]–[18]. To remove the limitations of above-mentioned issues a new low voltage ride through (LVRT) based control method is implemented with the injection of positive iq^+ and negative sequence iq^- reactive current reference as an input to the system to adjust negative sequence id^- and the iq^+ and iq^- component can balances the capacitor voltages by adjusting the (Vo) zero-sequence voltage [19], [20]. With the advent of this technology the grid voltage magnitude is controlled by providing sufficient reactive power during faults. Based on this method individual control of iq^+ and iq^- components are possible which manages the system configuration within its prescribed limits and this also manages to maintain the capacitor voltages in each submodule within 5%.

2. MODULAR MULTILEVEL CONVERTER CONFIGURATION

The basic block diagram configuration of modular multilevel converter (MMC) based on double star cascaded cell (DSCC) STATCOM connected in shunt manner with the grid is shown in Figure 1. The double star modular multilevel configuration for reactive power control is proposed in this article. The converter is comprised of several submodules and the number of submodules depend upon the output voltage. The DSCC modular converter is based on multiple sets of stars connected converter cells modules, in which the less voltage levels of numerous bidirectional cascaded cells are composed at each arm of the converter. The difference in voltage between module is commonly half of the rated voltage carried by using each converter cell inside the DSCC. In this proposed converter synchronous reference frame method for calculating the positive and negative reference current. It is known that during faults and unbalanced conditions zero and negative sequence are added to the converter legs of the ac voltage [21], [22]. The system under fault causes the generation of negative and zero sequence voltages on the converter end. The MMC converter phase voltages can be given as (1) and (2).

$$\begin{aligned} &V_u(t) = V^+\cos(\omega t + \theta^+) + V^-\cos(-\omega t + \delta + \theta^-) + V^0\cos(\omega t + \theta^0) \\ &V_v(t) = V^+\cos\left(\omega t - \tfrac{2\Pi}{3} + \theta^+\right) + V^-\cos\left(-\omega t - \tfrac{2\Pi}{3} + \delta + \theta^-\right) + V^0\cos(\omega t + \theta^0)\, V_w(t) = \\ &V^+\cos\left(\omega t + \tfrac{2\Pi}{3} + \theta^+\right) + V^-\cos\left(-\omega t + \tfrac{2\Pi}{3} + \delta + \theta^-\right) + V^0\cos(\omega t + \theta^0)\, i_u(t) = \\ &I^+\cos(\omega t + \theta^+) + I^-\cos(-\omega t + \delta + \theta^-) \end{aligned} \quad (1)$$

$$i_v(t) = I^+\cos\left(\omega t - \tfrac{2\Pi}{3} + \theta^+\right) + I^-\cos\left(-\omega t - \tfrac{2\Pi}{3} + \delta + \theta^-\right)$$

$$i_w(t) = I^+\cos\left(\omega t + \tfrac{2\Pi}{3} + \theta^+\right) + I^-\cos\left(-\omega t + \tfrac{2\Pi}{3} + \delta + \theta^-\right) \quad (2)$$

Where, δ is the positive and negative component phase difference. The current and voltage form (1) and (2) are separated into positive sequence dq^+ and negative sequence dq^- reference frame aligned with positive and negative grid voltages. The instantaneous actual power (real) across legs of the converter is given as (3).

$$P_j(t) = v_j(t) i_j(t) \big(j = u, v, w\big) \quad (3)$$

The average power across converter legs is given as (4).

$$\overline{P_{uvw}} = \frac{\overline{P_T}}{3} + \overline{P_j^+} + \overline{P_j^-} + \overline{P_j^0}\ (j = u,v,w) \quad (4)$$

Where $\overline{P_{uvw}}$ is the actual power absorbed by the converter end, $\overline{P_{juvw}^+}$ and , $\overline{P_{uvw}^-}$ is produced from sequence current values of real power and $\overline{P_j^+} + \overline{P_j^-} + \overline{P_j^{0=}}\Delta$Pj (j=u, v, w) is a term as the average change of actual power among the converter ends. So, (4) can be rewritten as (5).

$$\begin{aligned} &\bar{P}_a + \overline{P_b} + \overline{P_c} = \bar{P}_T \\ &(\Delta Pa + \Delta Pb + \Delta Pc = 0) \end{aligned} \quad (5)$$

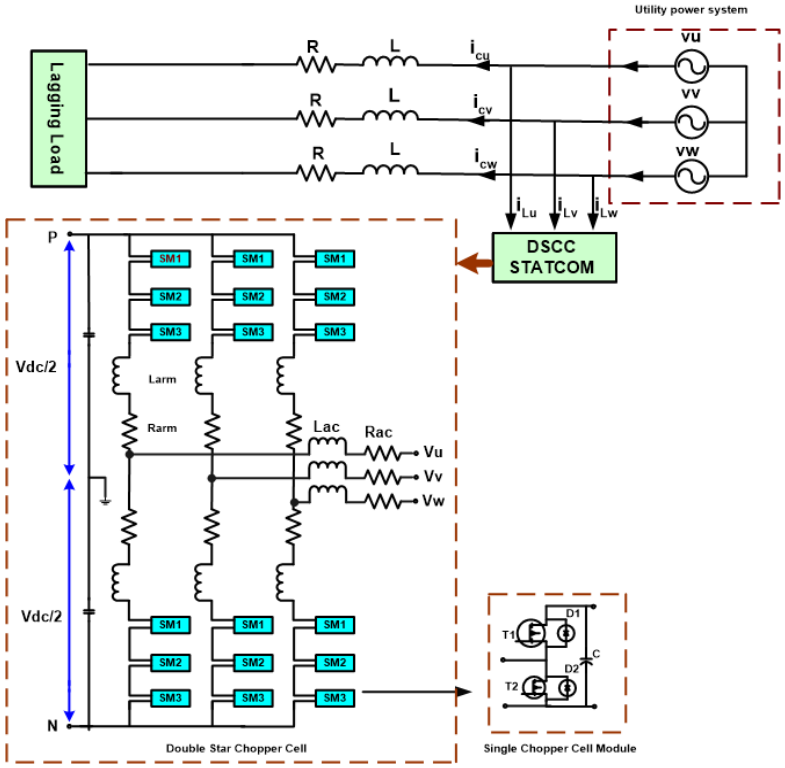

Figure 1. The DSCC-STATCOM configuration with grid

The comprehensive control of power to meet the requirement of system under fault and unbalanced load is fulfilled by controlling the components like id^+, iq^+, id^-, iq^- and vd^0 and vq^0. The reactive power injection during fault is utilized to recover the voltage sag and individual voltage control of capacitor, including cluster control within cell [23]. To control the various capacitor voltages in MMC STATCOM it is important to absorb real power form the grid and distribute it equally among various submodules. So measured real power can be given as (6)-(8).

$$\overline{P_T} = \frac{3}{2}\left(v_{sd}^{+}\, i_d^{+} + v_{sd}^{-}\, i_d^{-} + v_{sq}^{+}\, i_q^{+}\right) \quad (6)$$

$$\bar{P}_u = \bar{P}_v \cong \overline{\Delta P}u - \overline{\Delta P}v = 0 \quad (7)$$

$$\bar{P}_v = \overline{P_w} \cong \overline{\Delta P}v - \overline{\Delta P}w = 0 \quad (8)$$

From (6) the value of zero sequence Vo component can be obtained with the value of positive and negative sequence components as given in (9).

$$\begin{bmatrix} v_d^0 = v_d^0\, cos\ \theta_0 \\ v_d^0 = v_d^0\, cos\ \theta_0 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}^{-1} \begin{bmatrix} (P_v^+ - P_u^+) + (P_v^- - P_u^-) \\ (P_w^+ - P_v^+) + (P_w^- - P_v^-) \end{bmatrix} \quad (9)$$

Where,

$$A = \frac{3}{4}\left\{\begin{matrix} i_d^+ - \frac{1}{\sqrt{3}} i_q^+ + i_d^- cos\delta - i_q^- sin\delta \\ -\frac{1}{\sqrt{3}} i_d^- + i_d^- sin\delta + i_q^- cos\delta \end{matrix}\right\} \quad B = \frac{3}{4}\left\{\begin{matrix} \frac{1}{\sqrt{3}} i_d^+ + i_q^+ - i_d^- sin\delta + i_q^- cos\delta \\ -\frac{1}{\sqrt{3}} i_d^- cos\delta + \frac{1}{\sqrt{3}} i_q^- sin\delta \end{matrix}\right\}$$

$$C = \frac{\sqrt{3}}{2}\left(i_q^+ + i_q^- cos\delta + i_d^- sin\delta\right) \quad D = \frac{\sqrt{3}}{2}\left(-i_d^+ + i_d^- cos\delta + i_q^- sin\delta\right) \tag{10}$$

Other equations can be written as (11).

$$V^0 = \sqrt{(v_d^0)^2 + \left(v_q^0\right)^2} = f\left(i_d^+, i_q^+ i_d^-, i_q^-\right), \theta_0 = \tan^{-1}\left(\mathrm{v_q^0/v_d^0}\right) = \mathrm{g}\left(\mathrm{i_d^+, i_q^+ i_d^-, i_q^-}\right) \tag{11}$$

3. THE PROPOSED DSCC-STATCOM CONTROL

The block diagram representing the actual STATCOM working is shown in Figure 2. Considering the faulty and unbalanced load in grid, the control system of the DSCC STATCOM controls the reactive currents (id^+, iq^+, id^-, iq^-) and active, zero-sequence voltage components i.e vd^0 & vq^0. The reactive component iq^+ and iq^-references value is given by the grid, based on the unbalanced system. And all reactive and active components are obtained using in (10)-(12). In the proposed DSCC STATCOM, the components zero sequence component $-vd^0$, vq^0 and active power components (id^+, id^-) are dedicated to managing the real power circulations within the various submodules of the converter legs, this will manage the balancing of cluster voltage among cells within its operating range. The control of zero sequence voltage Vo and negative sequence current balances the dc voltage among converter. As shown in Figure 3, the proposed DSCC STATCOM control technique is comprised of three control modules i.e average control of overall power, cluster balancing module and current injection module. Also, it is considered that the reactive currents control is dedicated to manage the reactive control of the grid; while vd^0 and vq^0 is used to manage the power between the converter legs and id^- is used to limit the MMC power in its actual rated value. the DSCC MMC is four times than the other configurations because of the system chopper configuration in each cell.

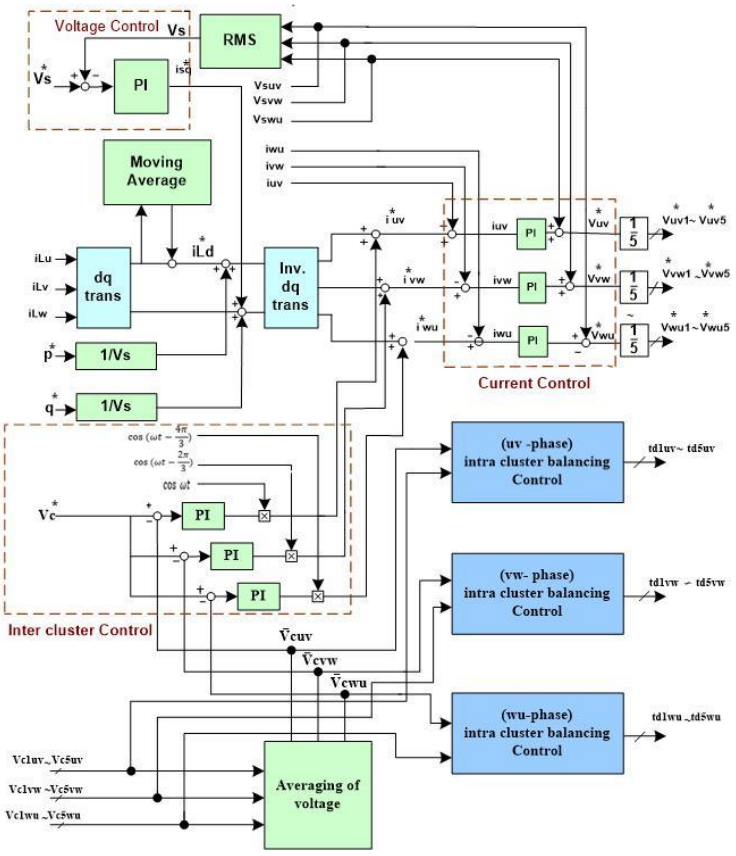

Figure 2. Overall control block diagram of the DSCC-STATCOM

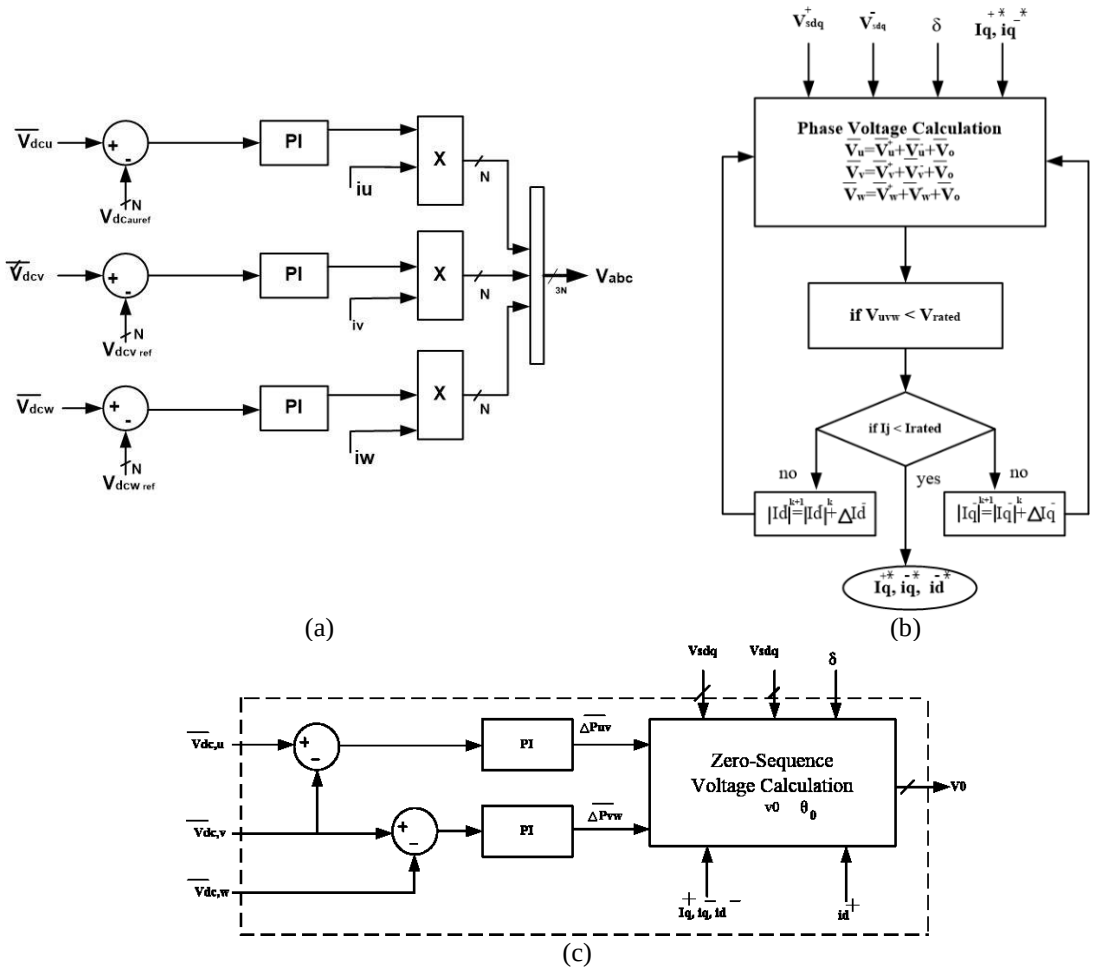

Figure 3. The control mechanism block diagram representation of DSCC based M-STATCOM: (a) individual capacitor voltage balancing block, (b) current control block, and (c) cluster voltage balancing block

The current control block determines the control of reactive and active current reference. As discussed, positive sequence iq^+ and negative sequence iq^- inputs are provided by the grid during faults and unbalanced conditions. These are the inputs given across the current control block. The zero-sequence voltage is determined from in (12). The positive and negative sequence values are obtained by adding zero sequence vector in the converter phases. The respective converter leg voltages are calculated as per the rated value (V_{uvw}< V_{rated}). If any of the phase value exceeds the rating of the converter nominal voltage, id- is raised to limit Vo to keep the MMC converter phase value in its rated voltage. Due to the advent of the faults in the power system MMC capacitor voltage balancing suffers. This capacitor voltage unbalancing is of two types namely inter-cluster and intra-cluster phase unbalancing of capacitor voltages [24]. The unequal distribution of real power among cells causes inter-cluster phase unbalancing of capacitor and the unbalancing due to unequal charging and discharging of current causes intra-cluster unbalancing in MMC. Thus, to prevent unbalancing of the capacitor voltage this zero-sequence current is injected within the phases of the 3 phase MMC modules to cancel the imbalance power [25]. The common average voltage need be obtained with the advent of zero sequence current in the converter. This calculated common reference voltage is applied to the converter to maintain the cluster voltage under control.

4. RESULTS AND DISCUSSION

The effectiveness of the proposed DSCC STATCOM control under faults and unbalanced load are simulated in MATLAB/Simulink environment with 5 level DSCC STATCOM configuration. Single line to ground fault and unbalanced load is taken as the input to check the performance of the proposed control for DSCC MMC STATCOM. Figure 4 shows the simulation setup of DSCC based STATCOM.

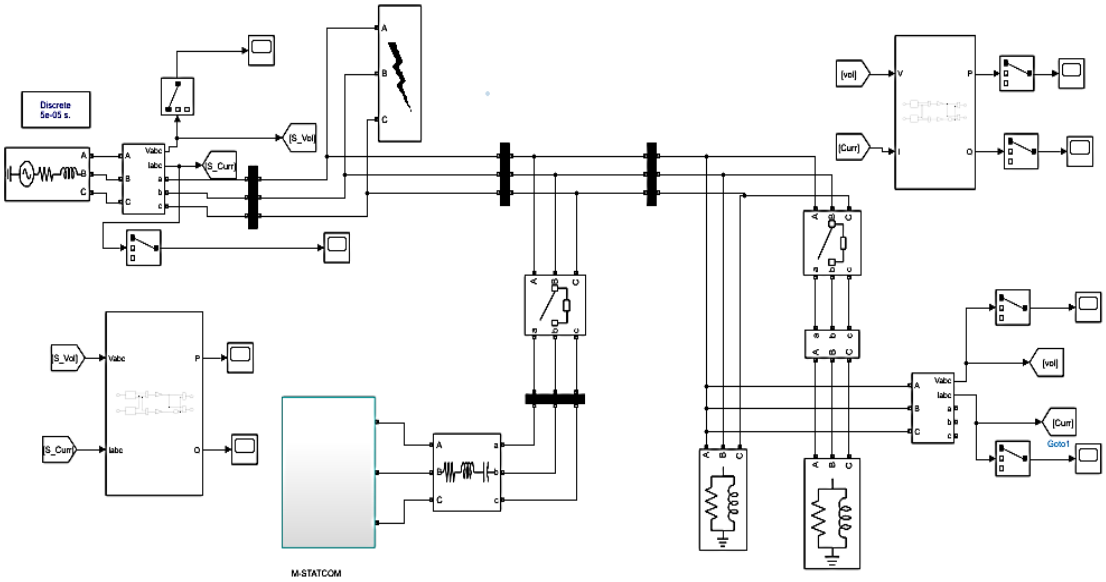

Figure 4. The simulation representation of DSCC based M-STATCOM in Simulink software

4.1. Case-1: Reactive power compensation under single line to ground fault (SLG)

To evaluate the execution of proposed LVRT control a SLG fault is enabled at time t=0.05 sec. The simulations were performed on three conditions i) without DSCC-STATCOM, ii) with convectional PI controlled DSCC-STATCOM and iii) with proposed LVRT controlled DSCC-STATCOM. In first simulation case without DSCC STATCOM it was observed that the voltage sag appeared on phase u was 0.723 pu (18.2 % of the reference voltage), as shown in Figure 5(a). It is observed that the during fault duration between t-0.05 sec. to t=0.1 sec. The second condition taken for simulation with DSCC-STATCOM, as shown in Figure 5(b). Here it is observed that during fault the voltage sag reduces to 0.8 pu, which is almost similar to the first condition with only 1% improvement in the system. The third simulation carried out with the proposed LVRT controlled DSCC-STATCOM as shown in Figure 5(c), here the results shown in figure revels that the voltage profile if improved from 0.72 pu to 0.1 pu, which is very vast improvement in the system as compared to conventional controlled method. The reactive power waveform across load is shown in Figure 6, where Figure 6(a) represents reactive power without STATCOM, Figure 6(b) shows reactive power with convectional waveform and Figure 6(c) is the reactive power with the proposed LVRT control circuit. The waveform shows the clear figure of improvement in the reactive power with the help of proposed LVRT STATCOM.

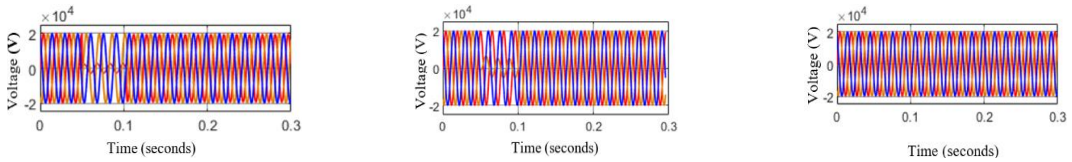

Figure 5. Single line to ground fault compensation waveforms: (a) voltage without STATCOM, (b) voltage with convectional DSCC-STATCOM, and (c) voltage with proposed DSCC-STATCOM

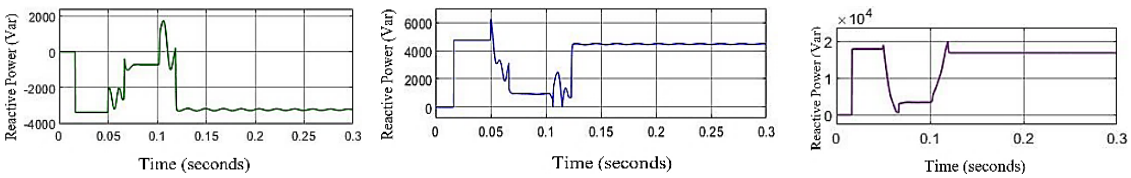

Figure 6. Single line to ground fault compensation waveforms: (a) Q without STATCOM, (b) Q with convectional DSCC-STATCOM, and (c) Q with proposed DSCC-STATCOM

4.2. Case-2: Reactive power compensation with unbalanced load

The simulations under unbalanced load are verified with three configurations i.e without DSCC-STATCOM, with convectional PI controlled DSCC-STATCOM and with proposed LVRT controlled DSCC-STATCOM. In case of without DSCC STATCOM, it was observed that the voltage unbalanced occurs between time t=0.05 sec. to t=0.1 sec. due to unbalanced inductive load as shown in Figure 7(a). The same system is observed under convectional DSCC-STATCOM, and here the unbalancing of voltage is marginally reduced, as shown in Figure 7(b), similarly the system is examined with the help of proposed DSCC modular STATCOM, and it is realized that the unbalancing of voltage among phases are considerably reduced as shown in Figure 7(c). The load side reactive power waveform without STATCOM, with convectional control STATCOM and with the proposed LVRT control waveforms are shown in Figures 8(a)-8(c) respectively.

The results shows that the proposed LVRT control method effectively manages the reactive power compensation for unbalanced load and thus provides the adequate reactive power for load compensation. The converter Figure 9(a) shows the reactive power compensation achieved under unbalanced load with and without proposed and similarly, Figure 9(b) shows the reactive power compensation achieved under single line to ground fault with and without proposed converter.

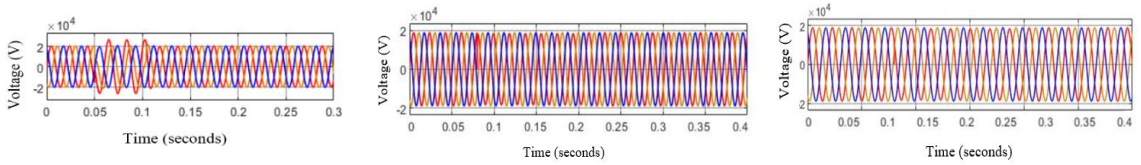

Figure 7. Unbalanced load compensation waveforms: (a) voltage without STATCOM, (b) voltage with convectional DSCC-STATCOM, and (c) voltage with proposed DSCC-STATCOM

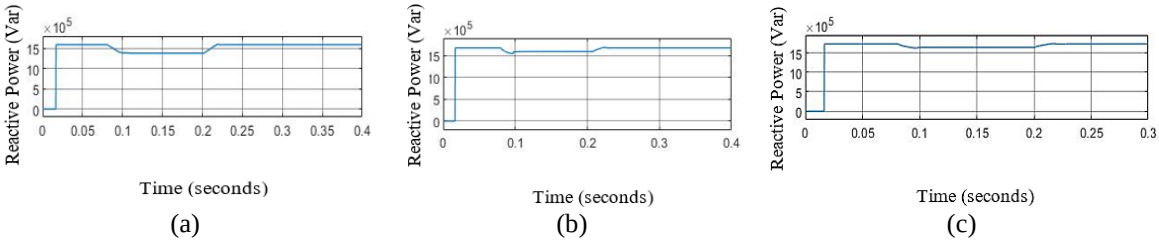

Figure 8. Unbalanced load compensation waveforms: (a) Q without STATCOM, (b) Q with convectional DSCC-STATCOM, and (c) Q with proposed DSCC-STATCOM

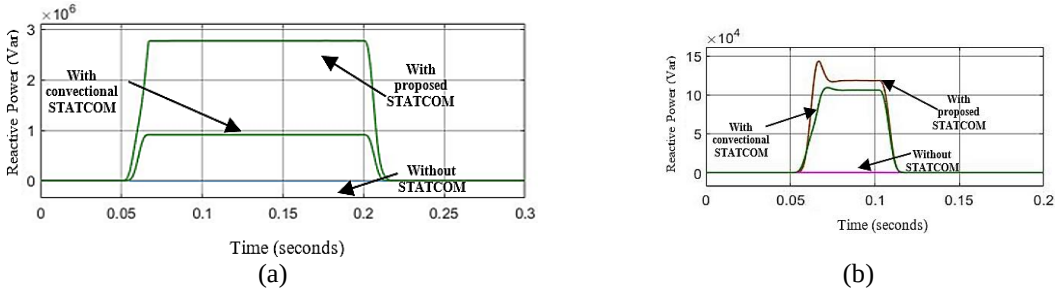

Figure 9. Reactive power compensation waveforms generated from converter end: (a) unbalanced load compensation and (b) single line to ground fault

4.3. Case-3: Capacitor voltage control

The capacitor voltages are unbalanced without the implementation of the capacitor voltage control technique in case of faults and unbalanced load in DSCC modular multilevel converter. With the advent of fault at t=0.05 sec to t=0.1 sec the voltage magnitude difference reaches 100 V in capacitor under fault duration time. This is because of the unequal distribution of active energy among converter to recover their switching

losses. Here the capacitor voltage deviation causes converter output voltage magnitude to sag and causes distortion also the distortion of output voltage waveforms introduces harmonics and will deviate source current. The proposed control effectively maintains the capacitor voltage among converter legs within its prescribed range i.e. 280 V. The capacitor voltage under single line to ground fault with convectional STATCOM and with proposed STATCOM is shown in Figures 10(a) and 10(b) respectively, and the capacitor voltage under unbalanced load with convectional STATCOM and with proposed STATCOM is shown in Figures 10(a) and 10(b) respectively. Another problem of inter-cluster capacitor unbalancing will be noticed among various submodules due to the different charging and discharging of the capacitor among legs. With the help of proposed control mechanism and all inter-cluster capacitor voltages are balanced as shown in Figures 12 and 13. The inter-cluster voltages under single line to ground fault with convectional STATCOM and with proposed STATCOM is shown in Figures 12(a) and 12(b) respectively and with proposed control under unbalanced load with convectional STATCOM and with proposed STATCOM is shown in Figures 13(a) and 13(b) respectively.

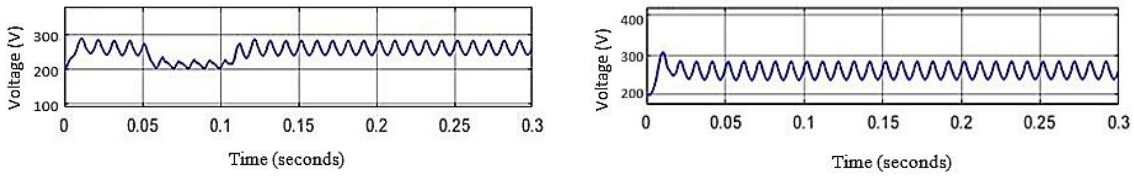

Figure 10. Capacitor voltage waveforms under SLG fault (a) without STATCOM and (b) with proposed controlled DSCC-STATCOM

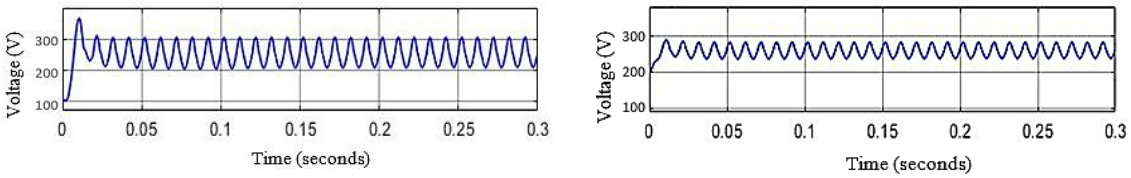

Figure 11. Capacitor voltage waveforms for unbalanced load (a) with convectional STATCOM and (b) with proposed controlled DSCC-STATCOM

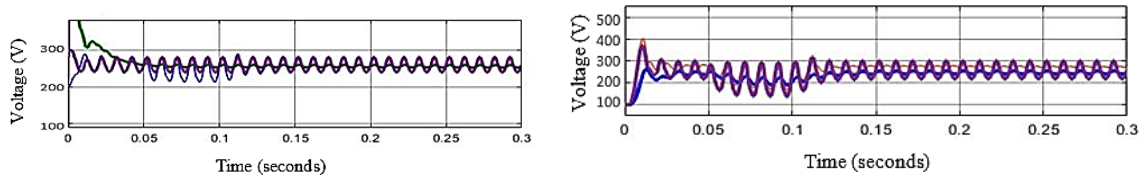

Figure 12. Inter cluster capacitor voltage waveforms of different submodules (a) under SLG fault without STATCOM and (b) under SLG fault with proposed controlled DSCC-STATCOM

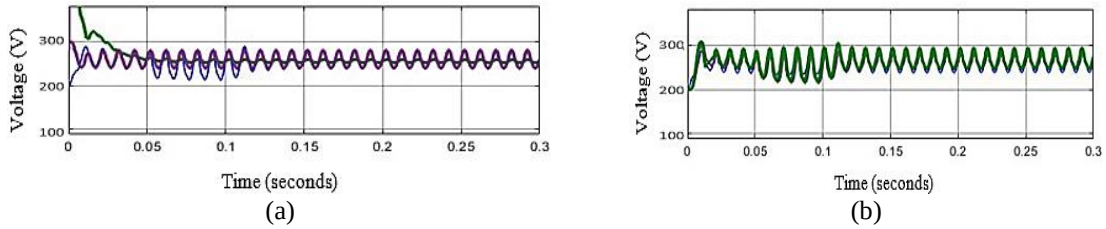

Figure 13. Inter cluster capacitor voltage waveforms of different submodules for unbalanced load (a) with convectional STATCOM and (b) with proposed controlled DSCC-STATCOM

The result obtained from simulations effectively represents the improvement in the compensation of the reactive power under unbalanced load and SLG fault in the power system. Analysis and novel contribution with proposed control method are as follows:

- The proposed LVRT method improves the voltage profile eliminates the voltage sag by providing sufficient reactive current.
- The proposed technique improves the STATCOM performance without tripping, as during the occurrence of grid faults, convectional STATCOM devices get disconnected from the system, and are not able to provide reactive support during fault duration.
- It manages to balance capacitor voltage within prescribed limit during the occurrence of grid faults and unbalanced load. And it does not require any extra circuitry for balancing inter cluster capacitor voltages, making the system less complex.
- The proposed technique improves the stability and provides dynamic reactive power compensation.

5. CONCLUSION

In this proposed LVRT controlled DSCC STATCOM, the positive and negative sequence reactive current parameter are controlled within the system during fault. The control algorithm for active and reactive power flow is derived to manage the real power among converter legs. This mechanism maintains the capacitor voltage under its prescribed range during fault and unbalanced load. Capacitor voltage management among converter is achieved by the injection of zero-sequence voltage in the system and with the advent negative-sequence current control. Moreover, the actual power flow within the converter legs is managed to keep the various sub module capacitor voltages in a balanced condition by the injection of zero sequence voltage in the system. The simulations results validate the performance of the proposed method for reactive power management and capacitor voltage balancing under fault and unbalanced load compensation.

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