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Hybrid control mechanism-based DVR for mitigation of voltage sag and swell in solar PV-based IEEE 33 bus system

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ABSTRACT

The power quality issues are raised due to sag/swell, which affects the overall performance of the grid-connected system. This study introduces the hybrid control mechanism based on a dynamic voltage restorer (DVR) to mitigate the sag and swell issues in the solar PV-based IEEE 33 bus system. The hybrid controller improves the dynamic performance and boosts the overall efficiency of the DVR system. The proposed work is also used to address the distribution system's voltage quality issues with minimal energy drawn out from the utility grid and effectively use solar energy. The sag and swell are introduced at the grid side and compensated at the load side by injecting DVR voltage. The proportional-integral (PI) controller followed by the fuzzy logic controller (FLC) is used to create the hybrid control mechanism for DVR. In this work, the solar PV system with DVR system is connected to the 29th location in the IEEE 33 bus system for performance realization. The hybrid control mechanism-based DVR provides 1.06% and 1.05% total harmonic distortion (THD) at sag and swell conditions for load voltage. The proposed work meets the IEEE 519 standards in terms of THD calculation. The proposed design compares with existing work and shows better THD reduction for load voltages.

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1. INTRODUCTION

The IEEE 33 bus distribution system is a well-known system invented by Baran and Wu in 1989 to investigate the effects of distribution system reconfiguration on load balancing and power loss reduction [1]. The IEEE 33 bus system is widely used to analyze most conventional distribution system problems. Solar photovoltaic (PV) is one of the efficient renewable energy resources available in most utility industries. The solar PV system attracts many users because of its features like being free from pollution, inherent characteristics, and availability in all sizes. The development of micro-grid PV systems is feasible with these features, and it supplies the electrical power from PV systems as a local renewable energy resource. The PV system's penetration is high in gigawatts, and the operation process becomes too complex. The PV array panel is incorporated with electrical devices and connected with the grid system for voltage profile conversion. However, it creates significant issues in power quality on the grid side, affecting the performance and quality of the electric power, which are unacceptable. It is necessary to investigate desirable power quality problems or disturbances caused by the solar PV system to enhance the solar PV-based grid system's reliability. The Power quality issues are raised due to voltage sag, swell, harmonics interruption, and

impulsive transients. These issues damage the machinery equipment while performing the process operation. Different methods like power system monitoring (PSM), unified power quality conditioner (UPQC), dynamic voltage regulator (DVR), an energy storage system (ESS), inverter method, and static synchronous compensator (STATCOM) are used to mitigate the power quality issues [2], [3].

The enhanced IEEE 33 bus system is commonly used in most intelligent power systems, integrating renewable energy resources, distributed systems, and advanced operation techniques to address the new challenges with optimal solutions The radial distribution system with distribution generation (DG) analyses the power flow calculation using the back/forward sweep technique. The IEEE 33 bus system is integrated with DG's to realize the impact on voltage profile. Combining the PV system with IEEE-33 bus radial feeders using genetic algorithms provides the optimal placement of PV and reduces the system's power loss. The multiple location distribution generations (MLDG) are used to enhance the performance and further reduce the power loss by placing DG in various locations in the IEEE 33 bus system [4]–[7].

The DVR is a cost-effective power electronic-based solution to mitigate and compensate the voltage sag and swells. The DVR injects the desired amount of voltage and mitigates the energy imbalanced and balanced voltages caused by the sag, swell, and disturbances. The DVR gets its active power from a direct current (DC) power source and injects its reactive power into the system. Furthermore, DVR runs on standby in typical situations until abnormal network circumstances arise. The DVR is responsible for supplying the voltage differential between lines (during voltage sag/swell) and maintaining the nominal voltage value (magnitude) at the load-connected DG system. It may safeguard essential loads by preventing unexpected voltage changes [8], [9]. The DVR typically uses an energy storage unit and DC-Link, injection transformer, voltage source inverter (VSI), harmonic filter unit, and bypass switch. The power-converter topologies used in DVR are either single-phase or three-phase. The central part of the DVR system is the control unit for mitigation and compensation of sag and swells. The DVR is operated in protection, standby, and injection mode based on principles [10], [11]. The DVR actively uses a reference generation unit, voltage and current control mechanism, pulse generator, and converter during injection mode in the control unit. The voltage compensation methods are chosen based on Load types, fault types, conditions, and DVR power rating. Techniques like Pre-sag compensation, in-phase compensation, Energy-minimized for balance sag/ imbalanced sag, and energy-minimized compensation are used for voltage compensation in the DVR system [12]-[15].

The existing works of DVR-based grid systems with performance metrics are discussed as below. The DVR-based 200 kW solar PV system is designed to reduce the THD with reactive power compensation by Gupta *et al.* [16], [17]. The fuzzy logic controller (FLC) output generates the three-phase voltage, and angle is used to control the pulse width modulation (PWM) generator, followed by voltage source control (VSC) based IGBT. The DC voltage compensation reduces the DC current injection, which is better with FLC than proportional-Integral (PI) controller. Benali *et al.* [18] presented the DVR-based grid-connected Solar PV systems to mitigate the voltage sag and improve the power quality. The system achieves the THD of 7.17% using load voltage during sag occurrence. Karthikeyan *et al.* [19] designed the performance comparison of the PI and pseudo derivative feedback (PDF) controllers using DVR under distorted grid conditions to analyze the dynamic response of the controllers. Tien *et al.* [20] introduced the DVR-based advanced control mechanism to mitigate power-based system voltage sags. The energy storage-based DVR mechanism is used for balance/unbalanced voltage sag mitigations. Kiswantono *et al.* [21] presented the DVR with battery energy storage (BES) and PV system to mitigate the distribution network system's voltage sag/swell and harmonics. This system achieves a THD of 4.39% during 60% sag and 3.07% during 60% swell. Zhang *et al.* [22] describe the DVR-based control mechanism, which uses double PQ theory to compensate for transient voltage disturbance in grid-connected systems. The work used more electric components; the cost is high, and a more complicated control mechanism for voltage compensation.

The single-phase DVR using FLC with a boost inverter is designed by Bajaj and Singh [23] for a solar energy PV system to mitigate sag/swell. The energy stored in the battery is used by DVR to mitigate sag/swell to reduce the cost and payback period. Thaha and Prakash [24] presented the FLC-based DVR control mechanism, which is used in a hybrid micro-grid system to reduce power quality issues. The system achieves a THD of 9.50% using a PI controller, THD of 7.5% using a genetic algorithm (GA) based PID controller, and THD of 4.15% using FLC based PI controller. Babu *et al.* [25] presented the solar PV inverter (SPVI) based DVR system to compensate for the voltage sag/swell. The system achieves a THD of 14% without DVR and a THD of 2.0% using the DVR approach. The unity power factor rectifier (UPFR) based DVR is designed by Ullah *et al.* [26] for micro-grid applications to maintain the power quality. The system achieves the THD of 2.40% using a diode bridge rectifier and 39.2% using UPFR. The DVR control mechanism with an online regulated DC-link capacitor for a micro-grid system is designed by Kandil and Ahmed [27] to compensate for the voltage sag level under different operating conditions. Molla and Cuo [28] presented the battery and super magnetic energy storage (SMES) based DVR system, and it is used to

compensate for the voltage sag in a grid-connected hybrid power system (wind+PV). The symmetrical and asymmetrical voltage sags conditions are analyzed and compensated using CAD software [29].

Gabalawy *et al.* [30] presented the double feed induction generator (DFIG) based wind turbines using the cuckoo search algorithm (CSA) to improve the output power. The PI controller and fractional order proportional-integral-derivative (FOPID) based control mechanism is introduced in CSA as an optimization approach to enhance the controller output response. The different control loops are discussed concerning the controller's response. The FOPID controller provides a better system response than the PI–based approach in DFIG-based wind turbines. The [31], [32] presented the direct converter-based DVR control mechanism to mitigate the voltage sag at the maximum point by modulating the carrier and error signals. The PWM-based control mechanism is used in DVR to mitigate the Voltage sag. The work achieves 52% of the sag mitigation using the DVR approach. The FLC-based STATCOM is designed by Suliman *et al.* [33] to improve the voltage profile in DGs. The static synchronous compensator is used as a control mechanism followed by the FLC system to analyze the balanced and unbalanced load voltages. After restoring the load voltage, the system achieves 97 % of the nominal value.

Abdulelah *et al*. [34] present the sliding mode control (SMC) and fly-back converter approach to realize the grid-connected PV inverter model. The work uses the Artificial neural network fuzzy interface system (ANFIS) based controller in maximum power point tracking (MPPT) to track the maximum power point in solar panels. Vuddanti *et al*. [35] describe solar PV with a weak grid system to improve the voltage profile. The work analyzes the voltage and current profiles at the grid and load sides. Kanagaraj and Rezk [36] presented the Hybrid combination of PV-thermoelectric generator (TEG) based DVR to compensate for the voltage disturbances in a three-phase system. The adaptive FLC with MPPT tracks the maximum power point at the grid side. The system achieves 3.52% of THD in sag conditions and 4.46% of THD in Swell conditions. The micro-grid source inverter control mechanism is introduced by Zadehbagheri *et al.* [37] using a novel backstepping controller. This controller controls the DG unit and also resists sudden load changes. Salman *et al*. [38] presented the DVR-based particle swarm optimization (PSO) approach with optimum control features. The feed-forward control using the PSO approach is adopted in DVR to mitigate the voltage disturbances. The DVR and DSTATCOM are integrated with gray wolf optimizer (GWO) and butterfly optimizer (BO) to improve the power quality issues, and it is analyzed by Chiranjivi and Swarnasri [39]. Saeed and Sheikhyounis [40] presented the PSO-artificial neural network (ANN) based unified power flow quality conditioner (UPQC) is designed to improve the power quality in DGs, which is caused by voltage disturbances.

Most of the exiting DVR-based grid system is designed using FLC/PI controller mechanism to mitigate the sag/swell conditions. But very little work contributed toward combining the IEEE Bus system with the DVR-based grid system and its performance realization. The contribution of the proposed work is highlighted as follows:

- The work introduces the integration of the solar PV grid system with IEEE 33 bus to realize the performance like THD at the load side. The proposed design is flexible to configure any type of bus system without altering the primary system.
- An efficient hybrid control mechanism based on DVR is used to mitigate and compensate for the voltage sag and swell in the Solar PV-based IEEE 33 bus system.
- The work compares the DVR-based hybrid controller with the DVR-based PI controller showing a better improvement in THD reduction and voltage magnitude during sag/ swell occurrence.

The manuscript is organized as follows: section 2 describes the modeling of the solar PV-based Grid-connected IEEE 33 bus system and working operations of the VSC control mechanism, DVR system, and FLC. The results and discussion of the proposed work are analyzed in section 3. The conclusion and future work are highlighted in section 4.

2. SOLAR PV BASED GRID CONNECTED IEEE 33 BUS SYSTEM

The solar PV-based grid-connected IEEE 33 bus system with a DVR mechanism is represented in Figure 1. The solar PV-based distributed generation (DG) system is connected to the 29th bus system to compensate for the sag and swell issues using DVR. The solar PV system for grid integrated DG applications mainly contains a solar PV array, and its power conditioning system, connected to IEEE 33 bus system, is represented in Figure 2.

The design includes two solar array panels, two DC-DC boost converters, a voltage source control (VSC) mechanism, a VSC inverter, a three-phase load, a three-phase transformer, and IEEE 33 bus system. The power conditioning system mainly contains an interface mechanism using MPPT features with a boost converter mechanism for connecting it to the IEEE 33 bus system. The 200 W solar PV system is connected to the proposed design of the IEEE 33 bus system. The two solar PV array panels are connected to two DC-

DC boost converters, which are used to track the MPP of the two solar PV array panels. The DC link capacitors are connected to the boost converters in both directions. The VSC control mechanism provides the reference gate pulses to the IGBT-based VSC inverter, allowing better synchronization between the PV and IEEE 33 bus systems. The three-phase transformer is connected to the grid bus via a three-phase programmable voltage source for grid voltage and current measurement (V_{grid} and I_{grid}). The three-phase programmable voltage source provides sag and swell conditions to the IEEE 33 bus system. The DVR is introduced to compensate for the sag/swell issues by injecting proper (V_{inj}) voltages across the load-connected IEEE 33 bus system. The three-phase breaker is connected between DVR input and output signals to compensate for the load-connected system.

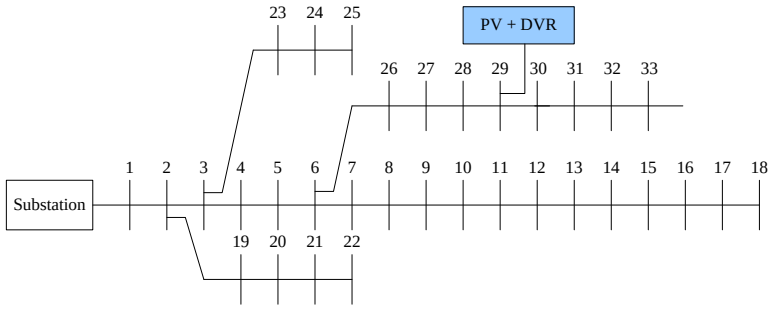


Figure 1. Solar PV-based grid-connected IEEE 33 bus system with DVR mechanism

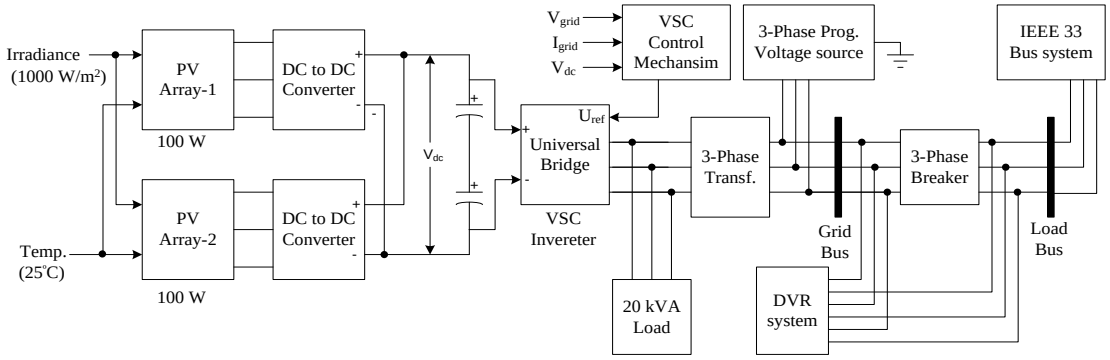


Figure 2. Proposed solar PV system with DVR mechanism for sag/swell mitigation

2.1. VSC control mechanism

The average model-based VSC inverter receives DC voltage and VSC control pulses for synchronization before connecting to the IEEE 33 bus system via a three-phase winding transformer. An RLC load of 20 kVAR is connected between the VSC inverter and the Three-phase transformer. Once the modulation index value changes, the VSC inverter output voltage will change automatically [6]. When the VSC inverter voltage exceeds the grid voltage (V_{grid}), the PV array system supplies reactive power to the grid; otherwise, active power is provided to the grid system. The VSC control mechanism is illustrated in Figure 3. It mainly contains Phase locked-Loop (PLL), park (abc to dq0) transformation module, V_{dc} Regulator, Current regulator, and the Modulation index finding module. The discrete PLL module synchronizes the three-phase sinusoidal signals of grid voltage (V_{grid}). The park transformation changes the three-phase (abc) reference frame to the dq0. The V_{dm} and V_{qm} have transformed the grid voltage's direct axis and quadrature axis components, respectively. Similarly, The I_{dm} and I_{qm} have converted the grid current's direct axis and quadrature axis components. The measured DC voltage (V_{dc}) is obtained after DC-DC boost conversion. The reference DC voltage (V_{dc_r}) is fixed to 500 V.

The V_{dc} and V_{dc_r} are applied to the PI-based Vdc regulator with regulated quadrature axis current ($I_{q\_r} = 0$) to generate the regulated direct axis current (I_{d_r}). The feed-forward current regulator with the inner current loop provides direct axis voltage (V_d) and quadrature axis voltage (V_q) using PI and FLC. When the direct axis current (I_d) and quadrature axis current (I_q) are positive in the inner current loop, the feed-forward

current regulator converter generates the active power (P+) and reactive power (Q-). The V_d and V_q, which are needed to determine the modulation index (m) and angle (δ), are represented as follows in (1). The inverter reference voltage (U_{ref}) is generated using modulation index and angle and connected to IGBT based VSC inverter. In general, The Park transformation converts the three-phase grid Voltage (V_{ga}, V_{gb}, and V_{gc}) to a three-level rotating reference frame (dq0) as shown in (2)-(4):

$$m = \sqrt{{V_d}^2 + {V_q}^2} \text{ and } \delta = tan^{-1}(V_d/V_q) \quad (1)$$

$$V_d = \frac{2}{3}[V_{ga}\, sin\theta + V_{gb}\, sin\left(\theta - \frac{2\pi}{3}\right) + V_{gc}\, sin\left(\theta + \frac{2\pi}{3}\right)] \quad (2)$$

$$V_q = \frac{2}{3}[V_{ga}\, cos\theta + V_{gb}\, cos\left(\theta - \frac{2\pi}{3}\right) + V_{gc}\, cos\left(\theta + \frac{2\pi}{3}\right)] \quad (3)$$

$$V_0 = \frac{1}{3}[V_{ga} + V_{gb} + V_{gc}] \quad (4)$$

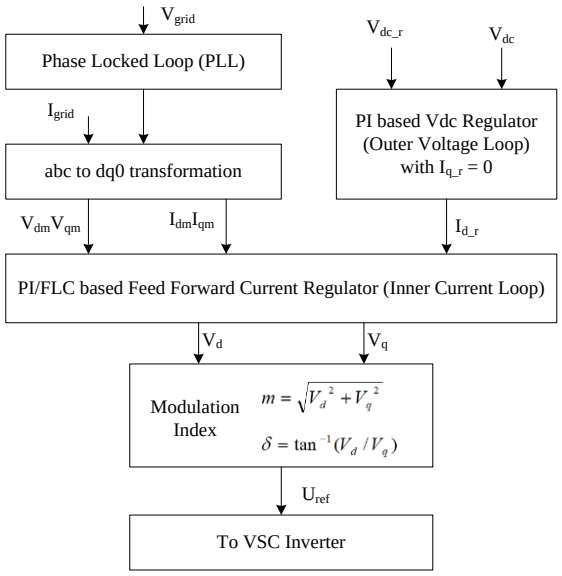


Figure 3. VSC Control mechanism using PI/FLC

2.2. DVR system

The DVR system is mainly used to inject minimum or maximum voltage components of amplitude, phase, and frequency between the power conditioning system and grid in series with the IEEE 33 bus system (load side) [2]. The complete DVR system is illustrated in Figure 4. The DVR system mainly consists of a hybrid control mechanism, PWM generator, and Two-level converter connected with a DC voltage, LC filter, and three-phase linear transformer with 12 terminals. The Hybrid control mechanism employed in the DVR system is represented in Figure 5.

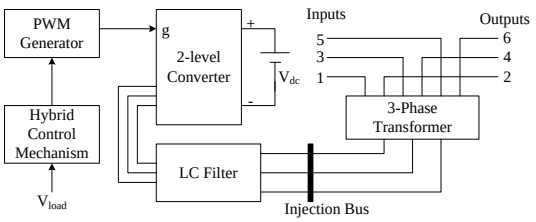


Figure 4. Modeling of the DVR system

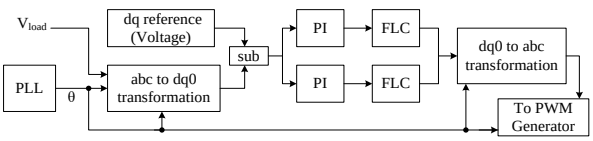


Figure 5. Hybrid controller for DVR system

The DVR detects sag/swell by monitoring load voltages and converting the 3-phase load voltage to direct current signals via the park transformation. The discrete PLL provides the angle (θ) to both park and inverse park (dq0 to abc) transformations. The error signal is generated by applying the load voltage (V_{load}) to the park transforms and subtracting it from the reference dq voltage. The error signal is fed to the Hybrid controller (PI controller followed by FLC) individually to generate controller output for dq voltage. Inverse park transformation is applied to create the actual state of three-phase voltage and the PWM generator. The inverse park transformation converts the three-level rotating reference frame (dq0) to the three-phase Voltage (V_a, V_b, and V_c) are represented using (5)-(7) is as follows:

$$V_a = V_d \, sin\theta + V_q \, cos\theta \; + V_0 \tag{5}$$

$$V_b = V_d \, sin(\theta - 2\pi/3) + V_q \, cos(\theta - 2\pi/3) + V_0 \tag{6}$$

$$V_c = V_d \, sin(\theta + 2\pi/3) + V_q \, cos(\theta + 2\pi/3) + V_0 \tag{7}$$

The PWM generator receives an angle from the PLL and provides a better controlling mechanism for an inverter (two-level converter) to generate the AC power from DC power. The PWM generator maintains the 3-phase sinusoidal voltage, which is a reference signal to the inverter. The PLL ensures that the frequencies and phases of the output signals match the reference values. The grid voltage with voltage sag/ swell is fed to a three-phase linear transformer. The Voltage series is injected via the 3-phase linear transformer using a hybrid controller and two-level converter coupled to the DC power source. The injected voltage is stored in an LC filter and connected to the IEEE 33 bus-based load system through 3-phase linear transformer output terminals for voltage compensation.

2.3. Fuzzy logic controller (FLC)

The fuzzy logic controller's motivation is to use human experience and expertise in the controller design application process. Instead of using the sophisticated dynamic model, the FLC gathers fuzzy variables to utilize directly in the dq0 process. The PI controller followed by FLC is used to provide a high-performance DVR control mechanism. By restricting the error (sag/swell) for compensation, the FLC improves the dynamic voltage (dq) responsiveness and other performance measures. The fuzzy logic controller's general block diagram is illustrated in Figure 6. Fuzzification, rule or knowledge base, inference engine, and defuzzification are significant blocks used in FLC construction. The fuzzification process turns crisp (actual) variables into fuzzier (linguistic) ones. The rule or knowledge base accumulates fuzzy variables and control rules information from the human decision process to achieve the decision-making logic or aim. The inference engine, also known as fuzzy inference or mechanism, is a process that performs different fuzzy logic operations to arrive at a control action mechanism for supplied fuzzy inputs. The defuzzification method converts the inferred fuzzy control action into the necessary crisp (actual) variables. Further within the DVR correction procedure, these crisp variables are utilized. For the DVR mechanism, two FLC are employed in this study. One FLC for the d process and another for the q process. The error value from the load dq voltage (V_{d_load} or V_{q_load}) and reference dq voltage (V_{dref} or V_{qref}) is sent to the PI controller. FLC receives the PI controller output for additional reference dq voltage limiting.

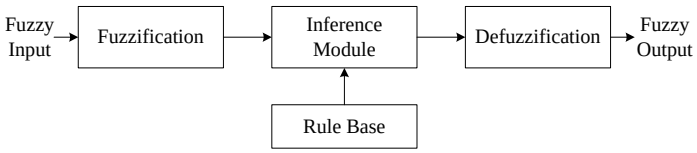


Figure 6. FLC operation

Input and output variables: The FLC use d or q error (e) and change in d or q error (Δe) as fuzzy input variables and produces the V_{d_flc} or V_{q_flc} as fuzzy output variable. The d or q error (e) and change in d or q error (Δe) are defined in (8) and (9) as follows:

$$e(i) = V_{dref} - V_{d_{load}} \; or \; V_{qref} - V_{q_{load}} \tag{8}$$

$$\Delta e(i) = e(i) - e(i-1) \tag{9}$$

The FLC Membership Functions are represented in Figure 7. The membership function graphs for fuzzy inputs such as d or q error (e) and change in d or q error (e) are shown in Figures 7(a) and 7(b) respectively. Figure 7(c) show the membership function plot for the FLC output. Using a set of membership functions for the provided universe of discourse, both inputs (e (i) and Δe (i)) are normalized to the display range -100 to 100. In contrast, in the specified universe of discourse, Fuzzy output is similarly configured with -100 to 100. Input fuzzy variables control the degree of membership with distinct classes. Each Fuzzy input variable has seven fuzzy values in this FLC architecture and is classified as a triangle membership function. Each Fuzzy output variable has seven fuzzy values and is classified as a trapezoidal membership function. Negative- large (NL), medium (NM), small (NS), zero (ZE), positive- large (PL), medium (PM), and small (PS) are the seven fuzzy values contained in the two fuzzy inputs and one FLC output.

Fuzzy rules: the two crisp inputs are turned into fuzzy variables and then translated into linguistic labels in the fuzzification process. The FIS supplies the rule basis as IF-THEN rules, which are represented in Table 1. Each linguistic label has two fuzzy inputs and one output, and the Membership functions are connected with them. In FIS, the two inputs are joined in an AND method. The Mamdani fuzzy interface system (FIS) is employed in the present FLC design process. This rule base comprises 49 rules that combine the two fuzzy input variables into a single output. Finally, the fuzzy results in the rule base are defuzzification with the centroid technique to provide crisp and executable output.

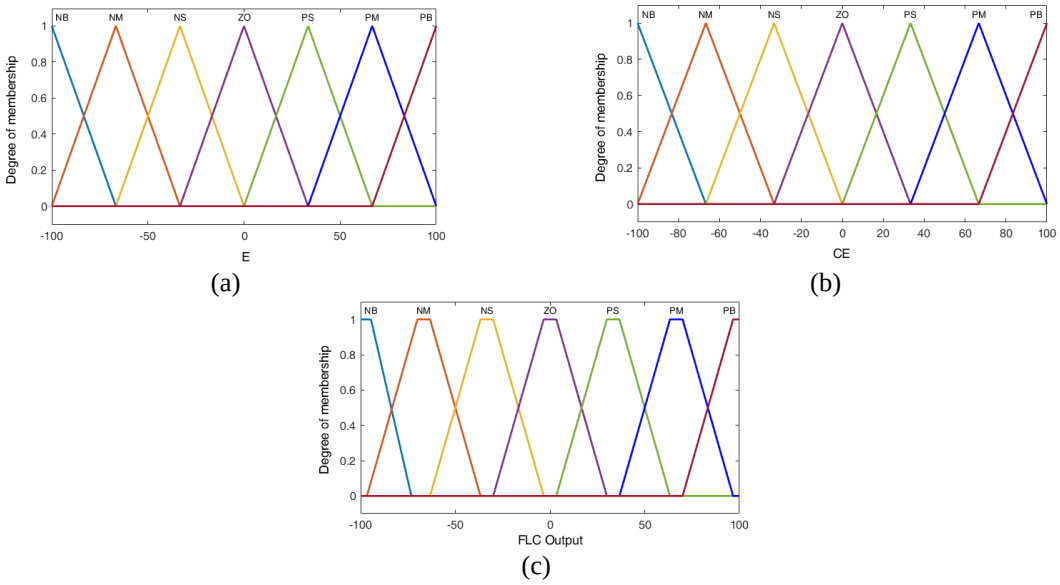


Figure 7. FLC membership functions (a) error input (b) change in error input, and (c) FLC output

Table 1. The fuzzy rule set for the DVR control mechanism

Output		Error (E)						
		NB	NM	NS	ZO	PS	PM	PB
CE	NB	NB	NB	NB	NB	NM	NS	ZO
	NM	NB	NB	NB	NM	NS	ZO	PS
	NS	NB	NB	NM	NS	ZO	PS	PM
	ZO	NB	NM	NS	ZO	PS	PM	PB
	PS	NM	NS	ZO	PS	PM	PB	PB
	PM	NS	ZO	PS	PM	PB	PB	PB
	PB	ZO	PS	PM	PB	PB	PB	PB

3. RESULTS AND DISCUSSION

The solar PV-based IEEE 33 bus system is designed using DVR with PI controller and Hybrid controller (PI with FLC) individually for sag or swell condition realization. The proposed design is modeled in MATLAB/Simulink. The mitigation of the sag/swell by injecting the DVR voltage in the IEEE 33 bus system is analyzed in detail. The performance analysis of the DVR-based PI controller and the hybrid controller is described through simulation and tabulation. The DVR dc voltage and simulation time are set to 500 V and 0.2 sec. The PWM pulses are generated at a carrier frequency of 22.5 kHz and a sampling time of 50 µs. The sag and swell appear between 0.08 and 0.12 seconds. The sag/swell amplitude variations are

introduced in a three-phase Programmable voltage source with a phase Voltage of 12.66 kV and 50 Hz frequency. The specifications and rated values for the solar PV-based IEEE 33 bus system using DVR are tabulated in Table 2. The bus data and branch data for IEEE 33 bus are from Baran and Wu [1].

The simulation results of the solar PV-based IEEE 33 bus system using the DVR mechanism at sag and swell conditions are illustrated in Figure 8. Figure 8(a) shows the grid voltage, load voltage, and DVR injected voltage under sag conditions. Similarly, Figure 8(b) shows the grid voltage, load voltage, and DVR injected voltage under swell conditions. All the Voltages are calculated phase to phase and measured in voltage per unit (Vpu). The single-phase grid, load and injected Voltage results using the DVR control mechanism (PI with FLC) are represented in Figure 9. The voltages at sag condition in Figure 9(a), voltages at swell condition in Figure 9(b), using the DVR control mechanism (PI with FLC) is illustrated.

The voltage (Vpu) calculation during sag/swell using DVR-based PI and hybrid controller is tabulated in Table 3. The grid voltage before sag/swell is set to 1 Vpu, the voltage at sag is set to 0.5 Vpu (50%), and the swell is set to 1.5 Vpu (50%). During sag condition, the injected voltage is 0.0452 Vpu, and during a swell, it is 0.055 Vpu. The load voltages are obtained after compensation using the DVR controlling mechanism. Load voltage of 0.95 Vpu and 0.96 Vpu are received during the sag condition using a DVR-based PI controller and DVR-based PI +FLC. The load voltage of 0.96 Vpu and 0.97 Vpu are obtained using a DVR-based PI controller and DVR-based PI +FLC during the swell condition.

Table 2. Specifications and parameter values used in solar PV-based IEEE 33 bus system

	Components Name	Values
Solar PV system (Sun power SPR-315E-WHT-D)	Parallel strings	64
	Series connected modules/string	5
	No. of solor cells/module	96
	STC module specification [V_{oc}, I_{sc}, V_{mp}, I_{mp}]	[64.6 V, 6.14 A, 54.7 V, 5.76 A]
	Module parameters [I_{lg}, I_{ds}, R_s, R_{sh}, Q_d]	[6.1461 A, 6.5043e-12, 0.43042 Ω, 430.05 Ω, 0.9507]
VSC control parameters	VSC nominal power and frequency	200 kVA, 50 Hz
	Nominal primary and secondary voltage	12.66 kV, 260 V
	DC bus voltage	500V
	Current regulator gains (Kp, Ki)	[0.3, 20]
	DC voltage regulator gains (Kp, Ki)	[7, 800]
	LC filter and DC capacitor	5mH, 100µF (with R =0.005 Ω) and 100µF
Grid Connected system	3-phase transformer nominal power and frequency	200 kVA, 50 Hz
	Winding voltages (phase to phase)	12.66 kV, 260 V
	3-phase programmable voltage source	12.66 kV (Phase to Phase)
	load (V_{p-p}, P, -Qc)	260 V, 20 kW, - 20 kVAR
	Sag amplitude and swell amplitude values	[1 0.5 1] and [1 1.5 1]
	Time values	[0 0.08 0.12]
	Three phase voltage source (substation)	12.66 kV (phase to phase) and 50 Hz frequency
	LC filter (DVR)	10 mH and 20 µF

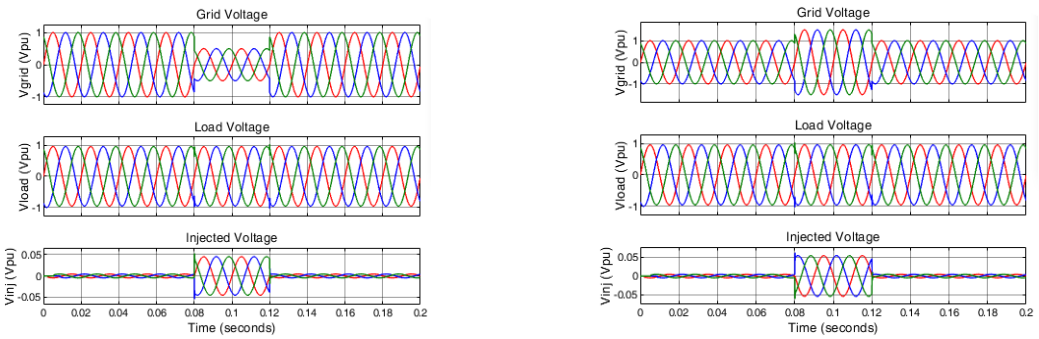


Figure 8. Simulation results of solar PV-based IEEE 33 bus system using DVR mechanism at (a) sag condition and (b) swell condition

The DVR controller outputs at the sag condition are illustrated in Figure 10. The error signal, PI Controller output, and PI+FLC output are represented in Figures 10(a)-10(c). Similarly, the DVR controller outputs at the swell condition are illustrated in Figure 11. The error signal, PI Controller output, and PI+FLC output at swell conditions are represented in Figures 11(a), 11(b), and 11(c), respectively.

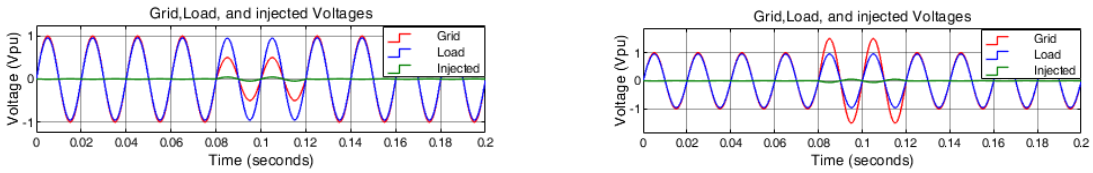


Figure 9. Grid, load and injected voltage (single-phase) using a DVR control mechanism at (a) sag condition and (b) swell condition

Table 3. Voltage (pu) calculation during sag/ swell using DVR-based PI and Hybrid controller

Voltages	50% sag		50% swell	
	DVR based PI	DVR based PI+FLC	DVR based PI	DVR based PI+ FLC
Grid Voltage before sag/swell (Vpu)	1	1	1	1
Voltage at sag/swell (Vpu)	0.5	0.5	1.5	1.5
Injected Voltage at sag/swell (Vpu)	0.0452	0.0452	0.055	0.055
Load Voltage at sag/swell (Vpu)	0.95	0.96	0.96	0.97

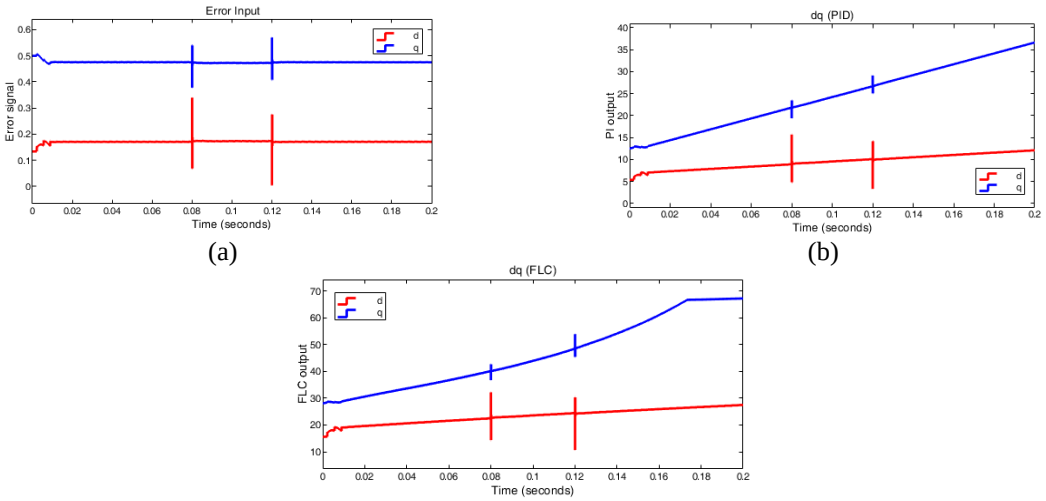


Figure 10. DVR controller outputs at sag condition for (a) error signal, (b) PI controller output and (c) FLC output

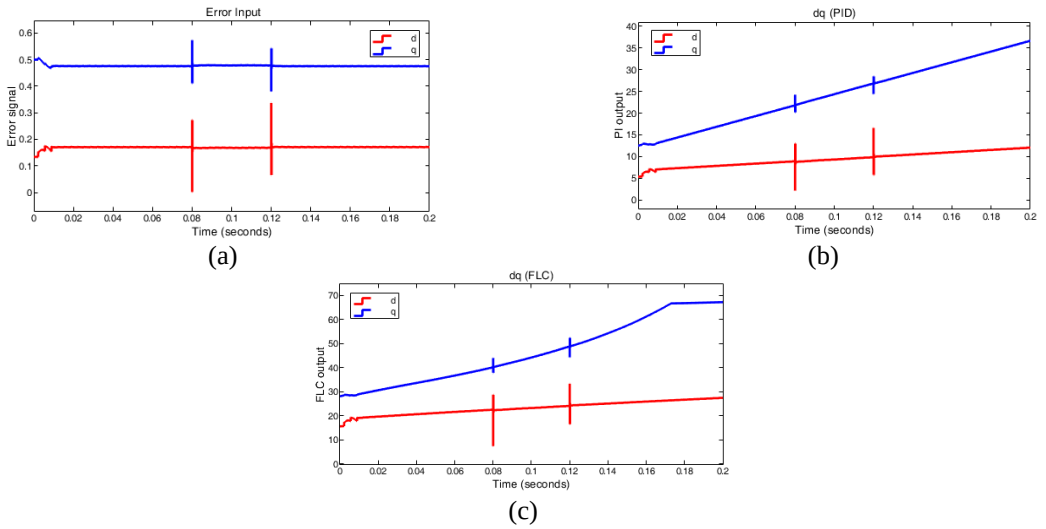
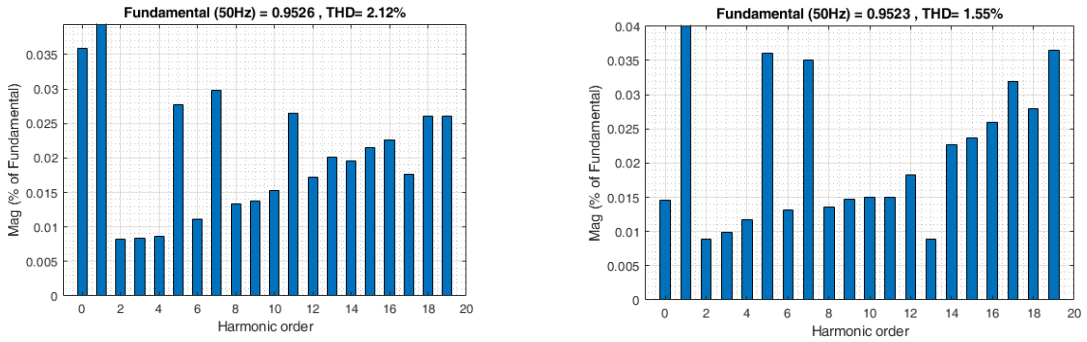


Figure 11. DVR Controller outputs at swell condition for (a) error signal, (b) PI controller output and (c) FLC output

The error signal is obtained by subtracting the load voltage from the reference dq voltage, with the d signal shown in red and the q signal in blue. The DVR with PI+FLC produces the desired dq voltages during sag and swell with the PWM generator. The DVR with PI+FLC also detects the required voltages for sag/swell mitigation. The % total harmonic distortion (THD) calculation during sag/swell using DVR-based PI and PI+FLC for the solar PV-based IEEE 33 bus system is tabulated in Table 4. Using FFT analysis, the THD is calculated for Load voltage during sag/swell at 0.08 sec. The load voltage of phase–A, phase–B, and phase–C is considered for THD calculation. Compared to the DVR-based PI controller, the DVR-based PI+FLC improves phase–A by 25 %, Phase–B by 26.88 %, and Phase C by 26.63 % THD during sag conditions. Similarly, the DVR-based PI+FLC improves phase –A by 25 %, phase–B by 27.01 %, and phase C by 27.23 % of THD compared to the DVR-based PI controller under the swell condition.

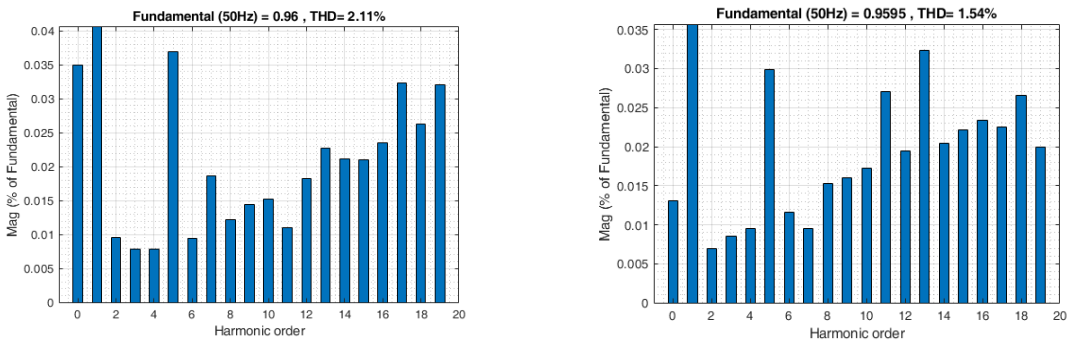
The % THD of load voltage (phase- B) obtained at sag condition is shown in Figure 12. The DVR-based PI controller in Figure 12(a) and the DVR-based PI +FLC controller in Figure 12(b) are represented. THD of 2.12 % is obtained for the DVR-based PI controller, whereas 1.55 % is accepted for the DVR-based PI+FLC controller. The percentage THD of load voltage (phase- B) obtained at swell condition is shown in Figure 13. The DVR-based PI controller in Figure 13(a) and the DVR-based PI +FLC controller in Figure 13(b) are represented. The THD of 2.11 % was obtained for the DVR-based PI controller, and 1.54 % of THD was obtained for the DVR-based PI+FLC controller.

The comparative analysis of different DG systems with a DVR control mechanism, disturbance type, and THD of the load voltage is tabulated in Table 5. The proposed design achieves an 85.35% reduction in THD at sag conditions compared to solar PV-based DVR with a PI controller [18]. The work reduces THD by 75.85% and 66.22% at sag and swells conditions, respectively, then the solar PV-based DVR with battery energy storage [21]. The work achieves a 74.69% reduction in THD at swell conditions compared to IEEE 14 bus-based DVR with PI and FLC [24]. The work reduces THD by 47.76% in the swell state compared to solar PV-based DVR with PI [25]. The work achieves a 56.25% reduction in THD at the Swell condition than the DVR with an energy storage unit [29]. Lastly, the proposed work provides a 69.88% reduction in THD at sag conditions than the solar PV with TEG-based DVR with PI [36]. Overall, the proposed solar PV-based IEEE 33 bus system using a DVR system achieves a better THD reduction than the other existing approaches.



(a) (b)

Figure 12. THD (%) of load voltage at sag condition for (a) DVR based PI and (b) DVR based PI+ FLC



(a) (b)

Figure 13. THD (%) of load voltage at swell condition for (a) DVR based PI and (b) DVR based PI+ FLC

Table 4. THD (%) calculation during sag/swell using DVR-based PI and PI+FLC

% THD Calculation for V_{load}	50% sag		50% swell	
	DVR with PI	DVR with PI+ FLC	DVR based PI	DVR based PI+ FLC
Phase -A	0.08	0.06	0.08	0.06
Phase -B	2.12	1.55	2.11	1.54
Phase -C	2.14	1.57	2.13	1.55

Table 5. Comparative results of different DG systems with DVR control mechanism and its THD

Designs	DG type	Injection transformer	Grid system	DVR control type	Disturbance type	THD of V_{load}
[18]	200 kW solar PV	200 kVA, 11 kV/260 V	NA	PI controller	sag	7.17%
[21]	600 W solar PV	10 kVA, 11 kV/380 V	NA	BES	sag	4.39
					swell	3.07
[24]	NA	NA	IEEE 14 bus	PI+FLC	swell	4.15
[25]	Solar PV	230 V	NA	PI controller	swell	2.01
[29]	NA	415 kV	NA	Energy storage unit	swell	2.4
[36]	Solar PV + TEG	4 kVA, 230 V/460 V	NA	PI controller + BES	sag	3.52
This work	200 W solar PV	200 kVA, 12.66 kV/260 V	IEEE 33 Bus	Hybrid (PI+FLC)	sag	1.06
					swell	1.05

4. CONCLUSION AND FUTURE WORK

In this manuscript, an efficient solar PV-based IEEE 33 bus system is designed using DVR with a hybrid control mechanism to compensate for the voltage sag and swell conditions. The solar PV system is connected to the 29th bus of the IEEE 33 bus system for load voltage analysis. The solar PV system is designed using an MPPT algorithm with a VSC control mechanism. The hybrid controller reduces the error and injects the three-phase voltage for load voltage compensation. The simulation results of the grid, load, and injected voltages are analyzed at sag and swell conditions. The load voltage profile of 0.96 Vpu and 0.97 Vpu is achieved during sag and swell duration. The output of the DVR with PI and hybrid controller (PI+FLC) is analyzed in detail. At sag and swell conditions, the DVR-based hybrid controller reduces the THD by 26% and 27%, respectively, compared to the DVR-based PI controller. The proposed work meets the IEEE 519 standards for THD analysis at sag and swell conditions. When compared with existing approaches, the proposed design improves THD reduction. In the future, a neural network-based DVR control mechanism can be used to increase the grid-connected system's efficiency and performance.

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