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A 1.8 V, 10 mA low dropout voltage regulator for IoT application in 90 nm CMOS technology

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ABSTRACT

A complementary metal-oxide-semiconductor CMOS low dropout voltage regulator (LDO) design flow using 90 nm CMOS technology is described and simulated in this paper. The circuit consists of an analogue LDO with using PMOS pass device, an error amplifier, a bandgap voltage, a biasing circuit, a feedback resistive network sized to have the desired closed loop gain. This LDO was designed to maintain stable voltage at 1.8 V and 10 mA of current output in low resistive load. The LDO regulator achieves 105 uA quiescent current, -47 PSRR@13 KHz noise frequency. The final design occupies approximately 0.05 mm^2. The results were satisfying and make the designed circuit suitable for IoT application.

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1. INTRODUCTION

The internet of things (IoT) is referring to the collection of all those devices that have the ability to connect to the internet and collect and share data [1]. RFID technology has matured to the point where it can now be used as part of the physical layer of the IoT for a variety of applicati [2] ons using low-cost, energy-efficient sensors [3]. A power-efficient rectifier that derives its energy from the RF field can provide the supply voltage for the transponder's circuits [2]. However, there are two major flaws with this strategy. To begin with, there are just a few microwatts of power available, which must be sufficient for the entire transponder chip. Second, the rectified signal may be affected by severeuctuations. A voltage regulator is a superior alternative for providing a more steady supply voltage while also reducing ripple [4]. The back-end circuits in the node are not influenced as much by supply voltage and load current changes with this approach. In this article, a low dropout voltage regulator for IoT application in 90nm CMOS technology using 2.5 V devices is proposed. We presented this article at the following: section 2 detailed circuits' description; section 3 presents the simulation results of our LDO circuit; and we conclude in section 4.

2. DETAILED CIRCUITS'DESCRIPTION

The architecture of the proposed LDO is presented in Figure 1 [5]. As shown in the figure, the components includes an error amplifier (EA), a pass device (Mpass), a feedback circuit (R1 and R2) and load (Cout and Iload). In this article it will be discussed separately later. The working principle of low drop out

regulator (LDO) [6]–[11] is that the error amplifier compares the scaled down regulated voltage, Vdiv with Vref and regulates the internal resistance of the pass transistor such that the error, V_{ref} - V_{div} is least or zero ideally.

The [12] and [13] are two examples of CMOS implementation of LDO [12] has proposed bulk modulation technique for improving load regulation and stability of capacitor-less LDO. Similarly [14] has proposed techniques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

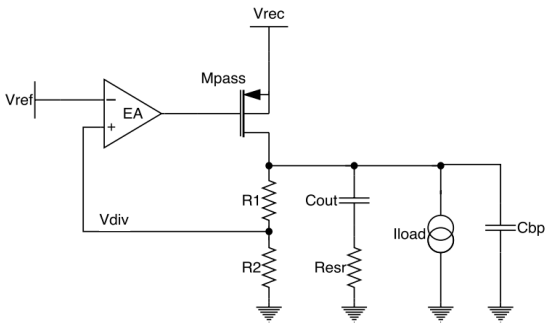

Figure 1. Generic LDO with pMOS pass device

2.1. LDO voltage regulator design

Figure 2 shows the CMOS implementation of LDO [15] in this article. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback network of resistors. As briefly mentioned above, the error amplifier amplifies the error i.e. difference in scaled regulated voltage, Vdiv and reference voltage, Vref. It is known that an amplifier with higher open loop DC gain reduces the closed loop gain error and hence amplifier with higher gain is desired here which is turn increase the accuracy of regulated voltage, Vreg [12]. Typically error amplifier has gain > 40dB which is not achieved with a single stage amplifier with this technology. Higher gain can be achieved by cascading multiple single stage but with increased difficulty in making the multistage amplifier stable. So for achieving higher DC gain and at the same time for stability convenience, folded cascode amplifier [15] is chosen.

The amplifier has a nMOS differential input stage, perferably for its higher mobility for achieving more gain. Reference voltage, Vref will be bandgap voltage, 1.17 V, of silicon and thus ICMR for EA lies almost at half the supply voltage. This amplifier drives a pMOS buffer which is used to supply sufficient current to drive the large pass transistor. Moreover, pMOS as a buffer passes 1 better which means it can turn off the pass device completely and hence LDO regulates better at low load or no load condition. However for heavier load/larger load current, this pMOS buffer is not able to pull down the gate of pass device suffuiciently lower [16]. This is overcome by making the pass device large enough to feed the required maximum load current.

The pass device is a pMOS transistor in this design. It is chosen because it has several advantages over it's counterparts like nMOS and BJT devices in terms of dropout voltage [16], quiescent current, input voltage, thermal response and noise [17]. Prominently, there are two factors that give pMOS edge over other devices; dropout voltage and quiescent current, when it comes to application in low power and low voltage devices. nMOS as a pass device requires a positive drive voltage with respect to output to operate. On the other hand, pMOS is driven by a negative signal with respect to input which means pMOS is preferable for a low input LDO. Similarly compared to BJTs, pMOS requires less headroom and less quiescent current to be driven, [17], [18], which means low dropout and low power operation, typical requirement of today's micro devices' power supply.

However, pMOS as a pass device in LDO causes challenges in stability [19]. As mentioned above, LDO utilises a high gain feedback loop in order to provide a regulated output voltages independent of load current and in any system with feedback loop, the locations of poles and zeros determine stability of the system [20]. In case of the pMOS LDO, the pass device is configured in a common source configuration [21]. LDO with big output cap has a dominant pole pole at the output, which is a low frequency pole. The second pole is located at the gate of pass device because as mentioned earlier pMOS pass device is large and has a big parasitic capacitance [22]. This second pole may be located closer to the dominant pole, resulting in significant reduction in phase margin (PM). Consequently, this may lead to instability of the LDO with pMOS pass device. Various methods have been implemented for ensuring the stability of the pMOS LDO. In

this article, a large external capacitor, C_{load} in Figure 1, is used for stabilising the system at the cost of additional settling time. When an external capacitor is used for designing a stable LDO, the minimum value of capacitance, Cload and minumum value of its equivalent series resistance (ESR) [23], Resr should be specified [18]. Cload determines the dominant pole of the LDO and Resr in series with Cload introduces a left half plane zero below unity gain frequency, UGF of LDO in order to cancel out the non-dominant pole below UGF, producing a stable LDO system.

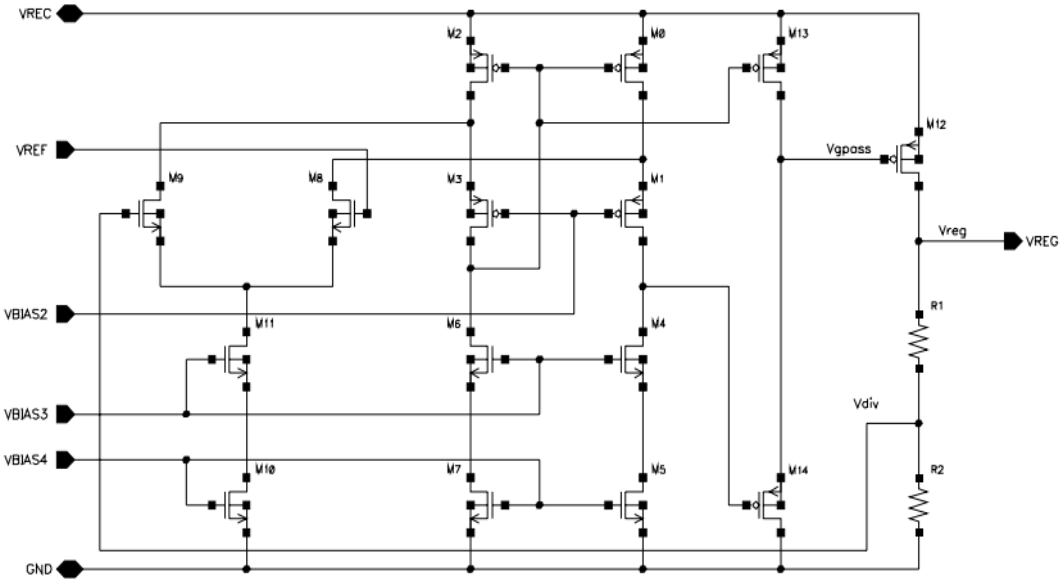

Figure 2. CMOS implementation of LDO

3. RESULTS AND DISCUSSION

The full layout is designed in 90nm process using 2.5 V devices. This process provides 1P-9M - 1 poly layer and 6 metal layers. However in this design, 1 poly and 8 metal layers is used. Basically every component layout used up-to 4 metal layers. Only the high current paths are made with parallel path of higher metal layers. The layout is shown in Figure 3 occupying a total area of 0.05 mm^2 including pads.

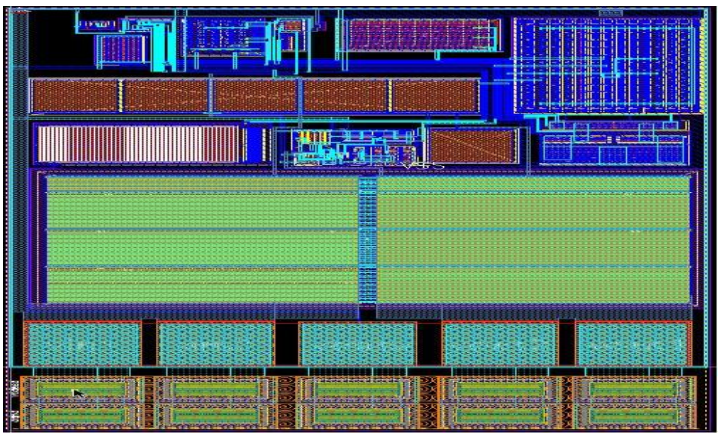

Figure 3. Layout of the LDO

Figures 4 and 5 show the transient response of LDO for line, Vrec and load, Iload variation. It gives information about how well and how fast regulated output settles for line and load variations. In Figure 4 load is given as pulse varying from 10 uA to 10 mA with both falling and rising time of 1 ns keeping input supply constant to 2.2 V. Sudden increase in load causes the output voltage to drop. The error amplifier then takes some time adjusts the gate voltage of pass device to low to fully turn on the device. Like wise when the

load suddenly drops to minimum, it causes the output voltage to increase. Again error amplifier adjust it back by increasing the gate voltage of pass device to turn it off. Similarly for line variation observation, input, Vrec is pulsed from 2 V to 2.5 V with 1 ns rising and falling time keeping load current constant to 10 mA. Sudden increase in input voltage causes output to increase and vice-versa. As in load variation case, similar recovery pattern is seen. In both case of load and line regulation, the output voltage is maintained quickly, less than 0.15 us. Both results from schematic and post layout have same transition behaviour except post layout result offset by 3.7 mV as explained in DC response.

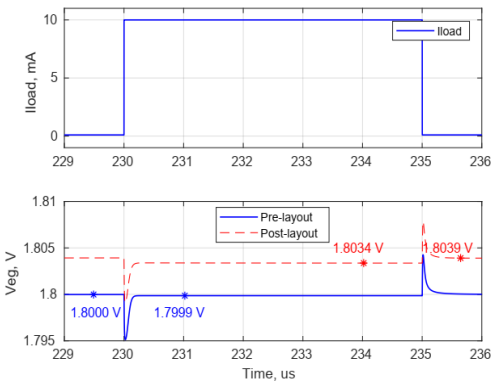

Figure 4. LDO step load regulation

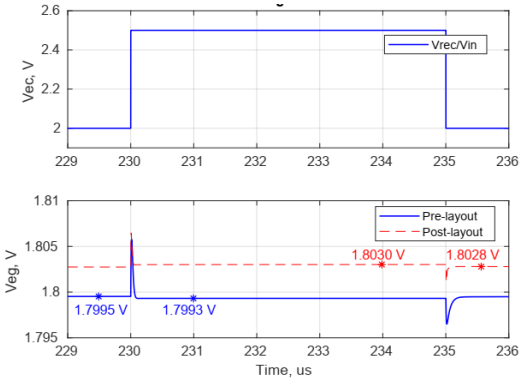

Figure 5. LDO step line regulation

Figure 6 show LDO response to input voltage. The regulator is turned off for input below 1.85 V. Since the input is also the supply for the entire design, higher voltage is required for creating proper biasing of internal folded cascode error amplifier. However after turning on, it requires only 100 mV drop for proper regulation for maximum load and is even lesser for lighter load. This shows that minimum value of supply required for LDO to function properly is 1.95 V. In Figure 6 it is seen that regulated output voltage for post layout simulation is 3.7 mV higher than for schematic. Since $V_{ref} = (1 + R_1/R_2) * V_{ref}$, the mismatch in the resistors has resulted in slightly higher ratio, consequently increasing the close loop gain.

Figure 7 is open loop gain and phase margin of LDO without and with compensation. In the upper uncompensated bode plot, two poles below UGF are seen: the first one at 300 KHz due to output resistance of pass device and its parasitic capacitance, and the second one at 60 MHz due to buffer output resistance and gate capacitance of pass device. UGF is at 100 MHz. Due to these two poles both occurring below UGF, the PM fallen to -45°. For making the LDO stable, as discussed in the beginning, a capacitor, Cload, 2.5 uF with specific series equivalent resistance, Resr, 0.8 Ω is used at the output. Cload and pass device output resistance creates the dominant pole at 1 KHz and Resr and Cload creates a left half plane zero below UGF which cancels the non dominant pole. This eventually gives 75 °PM and 30 dB GM.

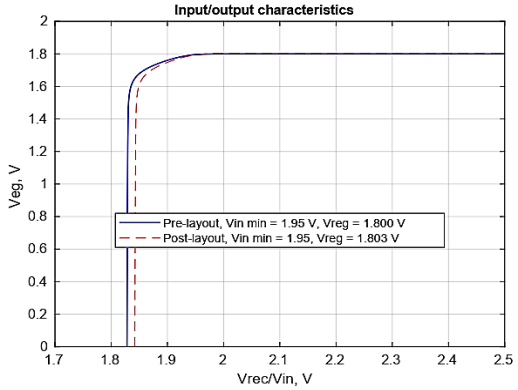

Figure 6. Regulated voltage with supply variation

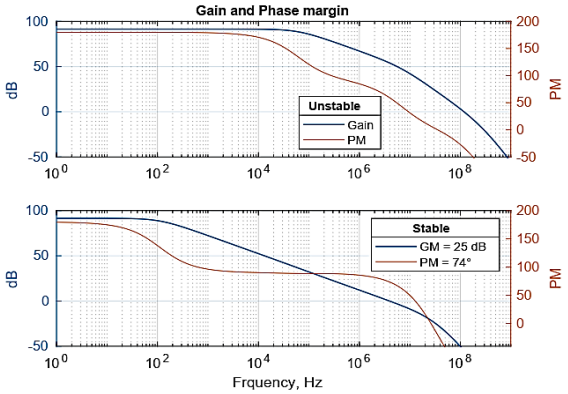

Figure 7. LDO stability before and after compensation

Likewise Figure 8 is the plot showing PSSR of this LDO. It can be seen that it has poor PSSR performance for frequency higher than 200 KHz. Low frequency noise like 50Hz supply ripple is effectively

rejected. In this design 13.56 MHz ripple and its first harmonics is expected in the input of LDO because rectified output from rectifier operating at 13.56 MHz as input signal is used as supply and/or input for this LDO. Unfortunately, PSSR performance is worst around this frequencies. However the ripple rejection is still -36 dB at 13.56 MHz which is decent. As seen in Figure 7 the open loop gain of LDO feedback circuit is 90 dB, which has contributed in achieving decent PSSR even at higher frequency [24]–[27]. The stability technique in this design also gives adverse effect on PSSR performance as UGF is significantly lowered by large output capacitor.

Table 1 summaries the performance of LDO regulator discussed above. Power efficiency is calculated as power delivered to load to power consumed from the source. Quiescent current includes biasing currents for error amplifier, feedback resistors and buffer which is obtained by taking the difference of current drawn from the source and current delivered to the load. Both power efficiency and quiescent current is calculated for maximum load operation.

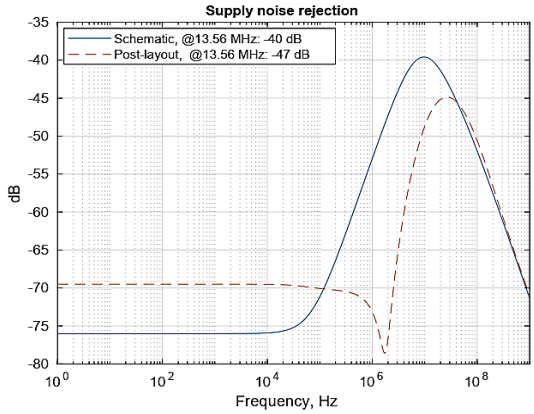

Figure 8. PSSR performance

Table 1. LDO performance summary

PSSR	-40 dB@13.56 MHz	PSSR	-40 dB@13.56 MHz
Phase margin	75°	Quiescent current	105 uA
Gain margin	30 dB	Load regulation	13 uV/mA
Power efficiency	80.9 %	Line regulation	395 uV/V

4. CONCLUSION

In conclusion, a CMOS low dropout voltage regulator voltage has been successfully designed in 90 nm CMOS technology. Circuit design, simulation, analysis and layout design are all included in this study. The performance of LDO is enhanced in this study. The proposed LDO is stable for the whole range of load current with quiescent current of only 105 µA when the load current is 10 mA. A load regulation is 13 uV/mA, a line regulation 395 uV/V, and a PSSR is -47 dB@13.56 MHz. An efficiency of 81% while delivering an output voltage of 1.8 V and the total area of the LDO is 0.005 mm^2. The chip possesses super characteristics suitable for various applications such as IoT.

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