International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 14, No. 2, June 2023, pp. 1011~1023
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v14.i2.pp1011-1023

A new flying capacitor multilevel converter topology with reduction of power electronic components

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Article Info

Article history:

Received Sep 14, 2022
Revised Jan 8, 2023
Accepted Jan 21, 2023

Keywords:

Flying capacitor
LSPWM
Multilevel inverter
Power electronic components
Total harmonic distortion

ABSTRACT

High power capacity and reliability are characteristics of multilevel inverters. The using a collection of DC sources can produce a terminal voltage that is very close to sinusoidal. The power quality can be improved by adding more levels, but this makes the control system more complicated and expensive. The number of power components in a multilevel inverter has been studied for decades. So, research needs to be done on multilevel inverter configurations to find ways to add levels with fewer power switches than with traditional topologies and those that have already been proposed. In this research, a new power-efficient arrangement of a flying-capacitor inverter is introduced. In order to illustrate the suggested topology, a seven-level multilevel inverter is constructed and demonstrated in a simplified form. Fewer power components, including power switches, capacitors, and gate driver circuits, are required in this topology than in other topologies described in the recent literature, which is one of its main advantages. The improvement mentioned above can be seen in the way this topology works, which is shown by the characteristics of the circuit. MATLAB/Simulink R2021a is used to simulate and verify the circuit to ensure the proposed topology is correct.

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1. INTRODUCTION

The industrial demand for high power equipment has been met by the power electronics scientific community by developing higher power semiconductor switches and offering high-power converter topologies [1]–[3]. Variable voltage and frequency are made possible by converting DC to AC electricity [4], [5]. A wide range of industrial applications have benefited from the development of multilevel inverters (MLIs) in recent years [6], [7] including active power filtering, motor drive applications, distributed generation systems, FACTS applications, UPS systems, induction heating applications, and many more [8], [9]. MLIs have several advantages over traditional two-level inverters, including lower total harmonic distortion (THD), reduced voltage stress in power switches, output filters are smaller, and immunity to electromagnetic interference [10], [11].

Multilevel inverters are designed to generate a staircase output voltage with high power goodness and a near-sinusoidal waveform [12]. There are many switches that work together to provide the right staircase voltage waveform, reducing total harmonic distortion (THD) and power switch voltage stress [13], [14]. Traditional multilevel converters may be divided into three types: diode-clamped (DC-MLI), cascaded H-Bridge (CHB-MLI), and flying capacitor multilevel inverter (FC-MLI) [14], [15]. Each of these three types has a distinct advantage over the others. However, high-level neutral-point clamped inverter topologies

need many clamping diodes and capacitors' balancing, which makes system maintenance more complicated, less reliable, and more costly. An additional feature of a FC-MLI inverter design is its capacity to store energy. The switching state of the topology ensures that the voltages of the flying capacitors are maintained at their proper levels [16], [17]. This complicates the voltage balancing system. This inverter is limited in its ability to operate at higher voltages because of the large number of flying capacitors and the sophisticated control system for balancing them. CHB MLIs are made up of many H-bridge cells and are therefore capable of providing multiple levels of output. CHB MLIs, on the other hand, need a variety of independent power sources, making them unsuitable for many applications. Additional power losses occur from MLIs' increased usage of gates and power switches [18]–[20].

In recent years, a significant amount of research attention has been focused among researchers on the topological evolution of MLI structures as well as on the quest to find a solution to the problem of capacitor voltage imbalance. A large number of MLI devices have also been presented [21]–[24]. In order to get an increased number of output voltage levels, several topologies with fewer switches and hybrid MLI topologies have been devised so far [25], [26].

This research proposes a new FC-MLI-based topology. With the suggested design, the number of switches and capacitors is significantly reduced compared to other designs in the same family. As a result, high-power converters may be smaller, more cost-effective, and more reliable, which is critical for industrial applications. It is discussed in this paper how the suggested converter works as well as the different switching states. Multicarrier sine pulse width modulation (MCPWM) is recommended for setting the output voltage precisely where it should be. Comparisons of the suggested structure's benefits are made to current structures in this family. The viability of the suggested structure in carrying out its function is demonstrated through the presentation of simulated outcomes.

2. FLYING CAPACITOR MULTILEVEL INVERTER

For their 1992 invention, Meynard and Foch devised the flying capacitor inverter [27]. Figure 1 depicts the essential components of the phase-leg FC-MLI. Flying capacitor multilevel inverters are constructed in a similar way as diode-clamped multilevel inverters, with the exception that capacitors are employed in place of diodes. The capacitors on the DC side of this design are arranged in a ladder topology. Each capacitor has a different voltage across it compared to the following one. The voltage rise between neighboring capacitor legs provides the size of a step in the voltage waveform at the output.

More voltage levels at the output can be achieved by connecting extra switches and a capacitor. FC-MLI also uses 2(m-1) switches, [(m-1) (m-2)/2] clamping capacitors per phase, and (m-1) capacitors on a shared DC-bus, where m is the number of inverter levels.

Across (a) and (n), the multilevel inverter shown in Figure 1(a) can produce one of three possible output voltages: V_{an}=0V, V_{an}=Vdc/2, or -Vdc/2V. In order to reach Vdc/2 voltage, turn on both S2 and S1 switches.; To generate a voltage of -Vdc/2, both S'2 and S'1 switches must be activated; and to achieve a voltage of (0), pairs S1 and S'1 or S2 and S'2 must be turned on. The output voltage of a FC-MLI with five levels is more adjustable than a three-level. Figure 1(b) depicts a five-level voltage over the neutral point (n). A sequence of power-switching combustions produces the V_{an}.

- S4, S3,S2 and S1 needs to be turned on for V_{an} to be equal to Vdc/2.
- When one of the top switches is turned off and its counterpart in location is switched on for V_{an} = Vdc/4. For example, consider the following formula: At the time of S4, S3, S2, and S'4 activation, V_{an} = 3Vdc/4 of the C3s-Vdc/2 (of the lower C4s). In this way, capacitors are connected in series to get the result that is wanted.
- Two higher switches have been switched off and their counterpart switches have been turned on, resulting in V_{an} = 0V. A comparable computation may be done, much like the one above.
- When V_{an} is equal to -Vdc/4, just one of the top switches is turned on.
- Turn on all the lower switches, S'4, S'3, S'2, and S'1 for V_{an} = -Vdc/2.

Figure 1(c) illustrates a seven-level flying capacitor MLI. A 7-level FC- MLI needs a DC supply, 12 power switching devices, 15 clamping capacitors, and 6 DC-link capacitors. This level has more output voltage switching states than a five-level inverter.

The capacitors' voltage varies as current runs through them. In order to regulate this voltage, one can either measure the capacitor voltages and the direction of the current and then select the appropriate switch state to right the capacitor voltage, or one can employ a natural balancing method, which is a method that keeps the steady-state stability of the capacitor voltages through employing equal duty cycles for every couple of complementary switching devices. This paper uses a natural balancing approach.

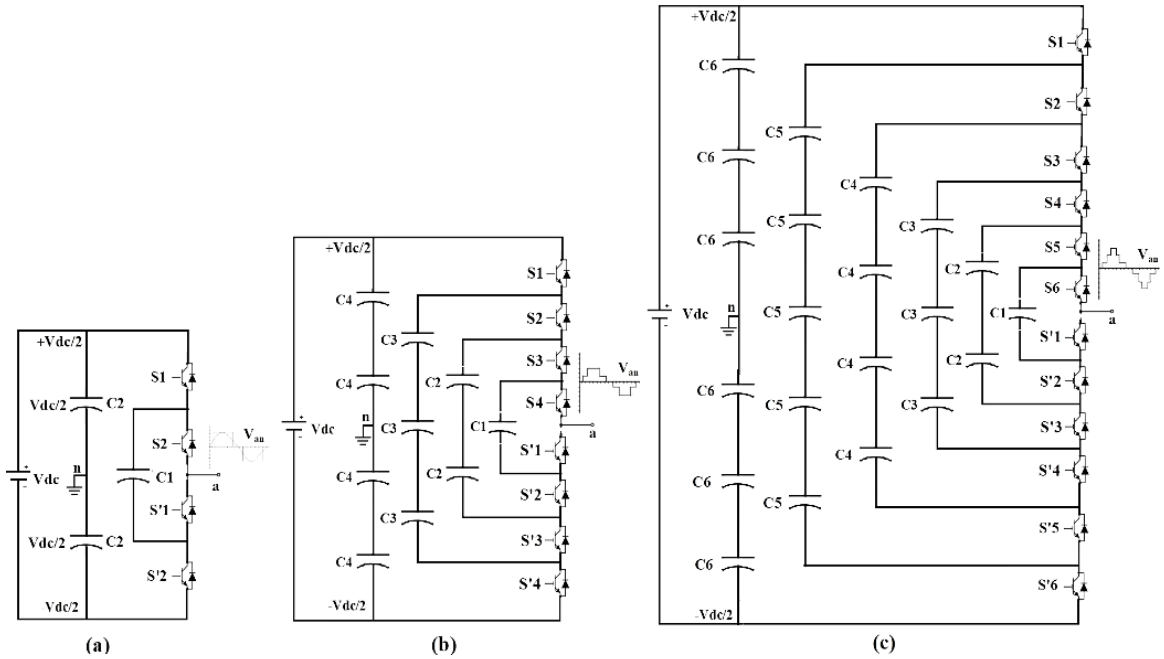

Figure 1. FC-MLI diagram (a) 3-level, (b) 5-level, and (c) 7-level

3. PROPOSED CONFIGURATION

The FC-MLI is the most common multilevel inverter design. It clamps a component to a dc bus using a capacitor to produce the output waveform step. In all conventional multilevel inverter systems, the level of output voltage decides the number of power components. Adding power switches to the inverter circuit makes it bigger, more expensive, harder to control, and needs more space to be installed. The suggested MLI uses a new power generating circuit design and an appropriate method for detecting a dc voltage level to provide a broad variety of output levels while using a minimum number of power components. Figure 2 depicts the basic building block of the proposed multilevel inverter.

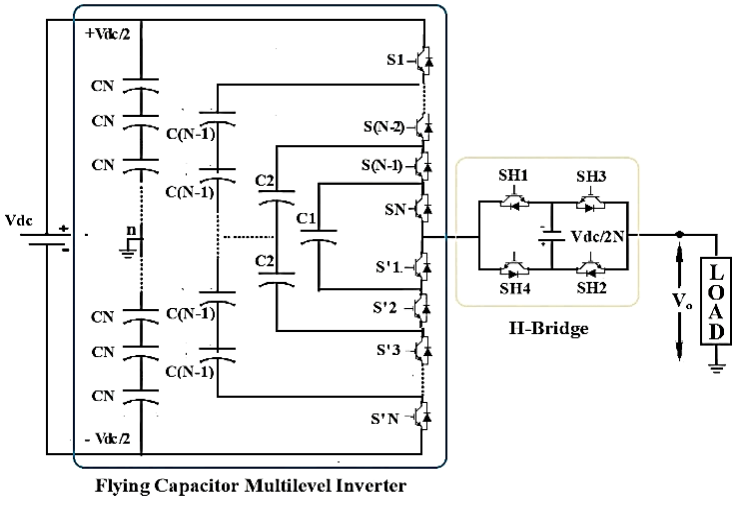

Figure 2. Propose structure for a single-phase circuit

Increasing the output level number is done by raising the number of levels in the flying capacitor circuit and keeping the power source at full bridge as it halves the voltage across the DC capacitor. The base level to get started is seven levels. The following equation can be used to calculate the range of levels of output voltage in the new MLI:

$$N_{Levels} = 2N + 3 \quad (1)$$

N is the number of capacitors on the dc bus as a whole. As for the suggested single phase, the number of clamping capacitors is equal to the number of clamping capacitors in the conventional FC-MLI part of the proposed topology. The equation below can be used to find out how many clamping capacitors are used in a traditional FC-MLI.

$$N_{\text{Clamping capacitor}} = \sum_{k=0}^{N\_1} k \quad (2)$$

Therefore, the clamping capacitor in the proposed topology equals:

$$N_{\text{Clamping capacitor}} = N(N-1)/2 \quad (3)$$

Here is an equation for determining the total number of power switches:

$$N_{\text{Switches}} = 2N + 4 \quad (4)$$

For a single-phase system, the peak output voltages (V_{omax}) and (V_{omin}) are defined as:

$$V_{omax} = +\frac{(N+1)V_{dc}}{2N} \quad (5)$$

$$V_{omax} = -\frac{(N+1)V_{dc}}{2N} \quad (6)$$

Since both the provided MLI and the traditional FC-MLI have the same number of levels, Table 1 shows how the power components of the two architectures compare.

The Figures 3 and 4 depict the number of power switches and clamping capacitors required for the traditional FC-MLI topology and the new proposed FC-MLI design, respectively. The proposed topology required a minimum of seven levels, so that's where we begin with these numbers. The PIV and period of switching working at a frequency carrier in each cycle depend on a position in the proposed circuit's structure. Also, the voltage and current ratings of the switches have the same load rating.

Table 1. Compares the suggested seven level FC-MLI with a conventional FC-MLI that has the same number of levels

Parameter	Type of topology	
	Conventional FC-MLI	Proposed configuration
Number of levels	7	7
power switches	12	8
Clamping capacitor	15	1
DC bus capacitors	6	2
Voltage drops in every state	6 V_D	4 V_D

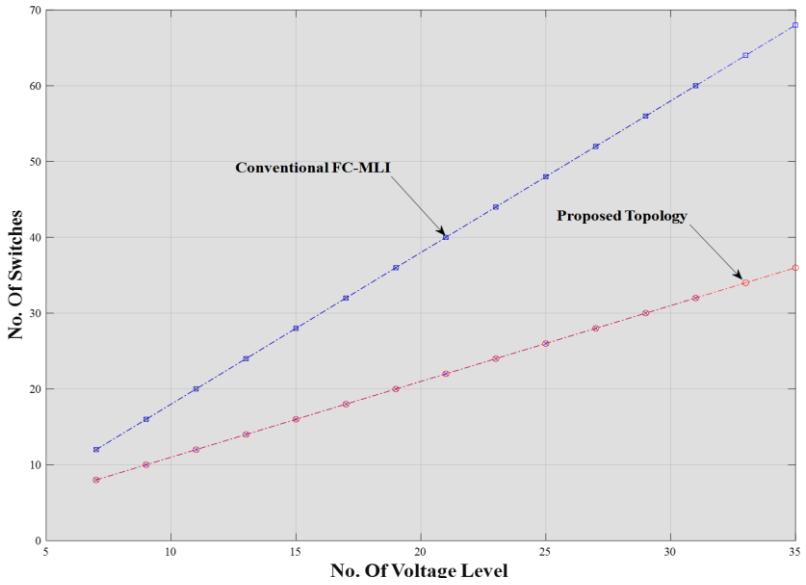

Figure 3. Compares proposed and conventional FC-MLI power switches counts

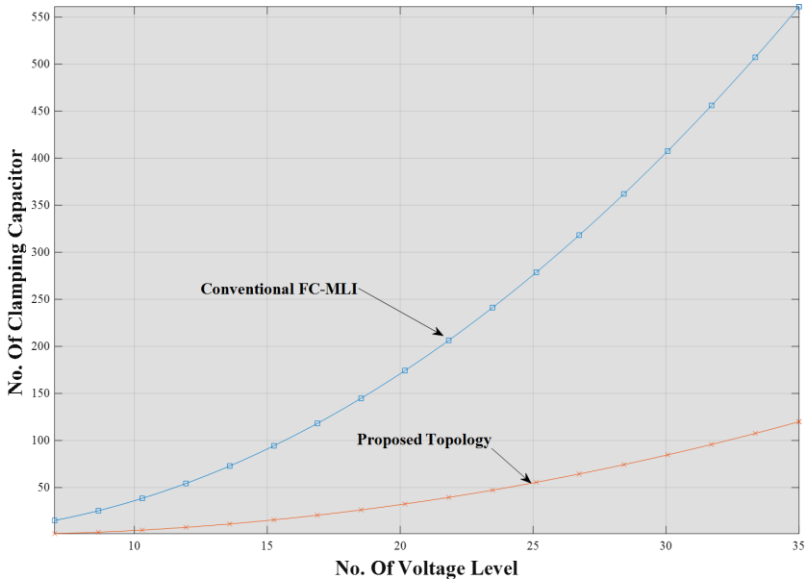

Figure 4. Compares suggested and conventional FC-MLI clamping capacitor counts

4. MODULATION TECHNIQUE

The multilevel inverters have been controlled using a variety of modulation approaches. Multicarrier Sine Pulse Width Modulation (MCPWM) approaches are among the most often employed for diverse multilevel inverter topologies. For three or so more levels, a MCPWM is used. They may be divided into two categories: level shift and phase shift [28], [29].

4.1. Phase shifted pulse width modulation (PSPWM)

The PSPWM technique is the easiest and most common way to switch. However, when designing an m-level inverter, m-1 carrier waves are necessary, and they should be displaced by 360/(m-1) with regard to one another. Figure 5 shows the explanation above [30], [31].

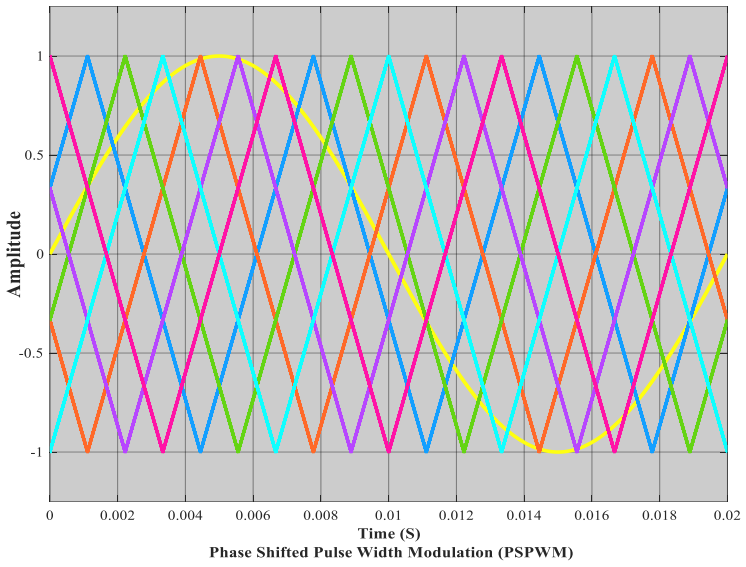

Figure 5. Carrier's waves in the PSPWM modulation

4.2. Level shifted PWM (LSPWM)

In LSPWM, an m-level inverter requires a total of (m-1) carrier signals. Equal amplitude and frequency should be used to ensure proper signal processing. All carrier signals are phase-shifted in relation to one another, with zero reference in mind [32], [33]. Three primary types of LSPWM exist:

4.2.1. Phase disposition (PDPWM)

Carrier and reference signal settings for PDPWM in a seven-level MLI are shown in Figure 6. All the carrier signals here are perfectly phase-locked and of the same frequency and amplitude. The method relies on the comparison between a vertically oriented carrier wave and a sinusoidal reference wave.

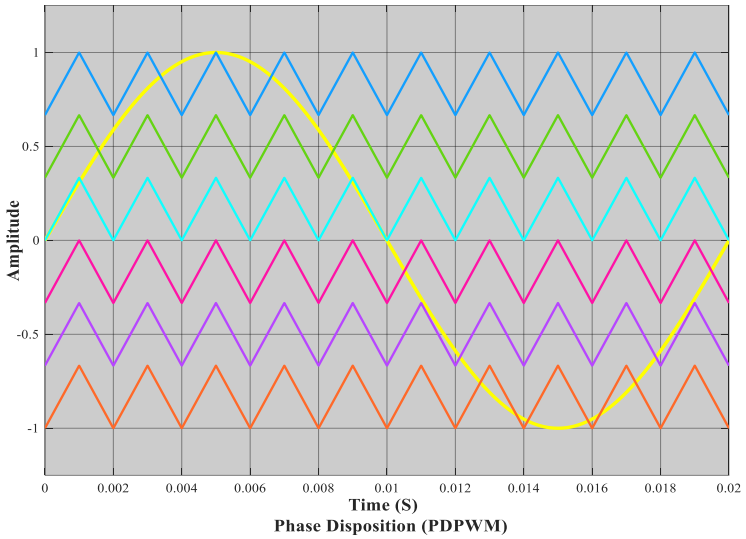

Figure 6. Carrier and reference signals throughout PDPWM technique

4.2.2. Phase opposition disposition (PODPWM)

This technique utilizes disposition and phase opposition. Frequency and amplitude are same for all carrier signals. Carrier signals above the zero reference have a phase shift of 180 degrees with respect to those below. Figure 7 illustrates the carrier signal and reference configurations used in PODPWM for the seven-level multilevel inverter. The zero level arises without a carrier, whereas the upper three carriers generate three positive levels and the bottom three negative levels.

4.2.3. Alternate phase opposition disposition (APODPWM)

In the case of alternative opposition disposition (APOD) modulation, the carrier signals are rotated via an angle of 180 degrees with respect to the carrier signal that came before them. Figure 8 clearly demonstrates this concept. The APODPWM uses a combination of six carriers to produce seven levels.

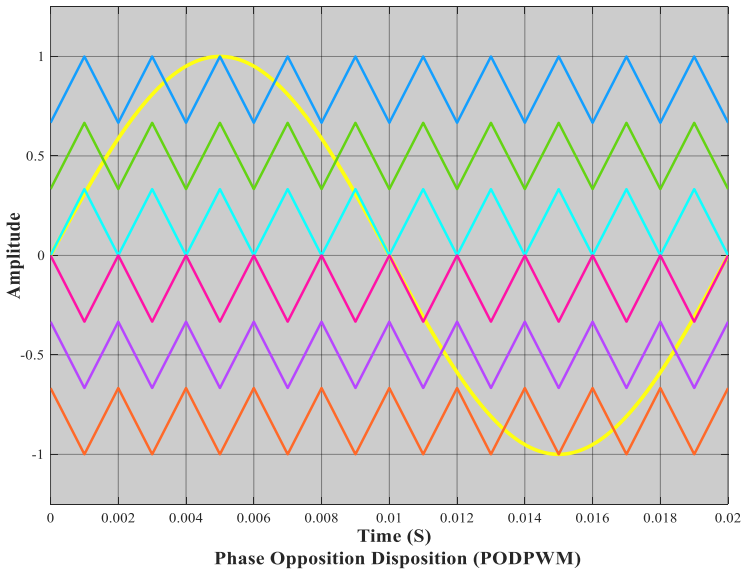

Figure 7. Seven-level carrier arrangement (using the PODPWM method)

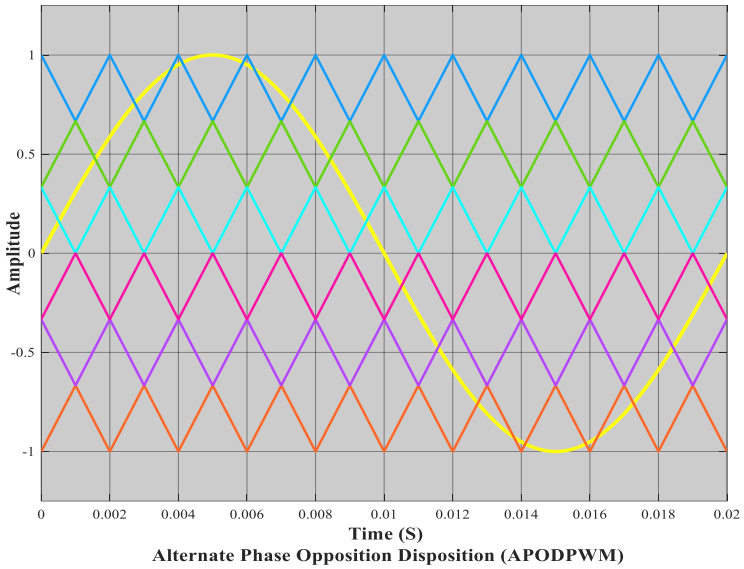

Figure 8. Carrier configuration on a seven-level scale (in accordance with APODPWM)

5. SIMULATION RESULTS

A model based on the proposed design, as shown in Figure 2, is simulated to confirm the capability of the proposed multilevel inverter to generate an appropriate waveform of output voltage. The simulation work was done in MATLAB using the Simulink toolbox. The seven-step staircase waveform at 50 Hz is produced by the proposed multilevel shown in Figure 9 with resistive load.

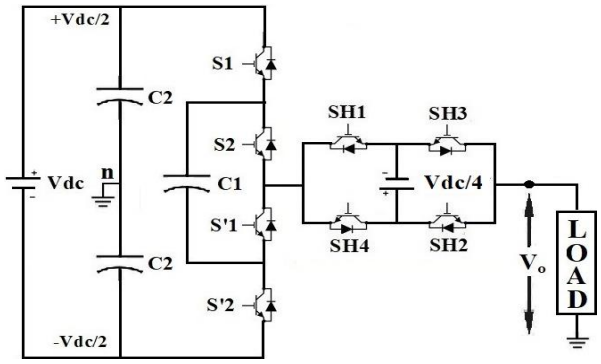

Figure 9. A new single-phase multilevel inverter with a seven-level configuration

Table 2 provides a depiction of the look - up table for ON-OFF power switches. The control scheme aims to supply load with a voltage that is as near to the reference voltage as is technically feasible. This research utilizes multicarrier modulation with modulation index = 1 and carrier frequency = 3000 Hz to reach this result.

Table 2. Demonstrates both the voltage output as well as the switching states of the proposed

Output voltage V_0	Switches between states							
	S1	S2	S'1	S'2	SH1	SH2	SH3	SH4
Vo=+3/4Vdc	1	1	0	0	1	1	0	0
Vo=+1/2Vdc	1	1	0	0	1	0	1	0
Vo=+1/4Vdc	1	0	1	0	1	1	0	0
Vo=0	1	0	1	0	1	0	1	0
Vo= - 1/4Vdc	0	1	0	1	0	0	1	1
Vo=-1/2Vdc	0	0	1	1	0	1	0	1
Vo= -3/4Vdc	0	0	1	1	0	0	1	1

Figures 10 and 11 display the suggested multilevel inverter's output voltage, which has seven levels: -150 V, -100 V, -50 V, 0, 50 V, 100 V, and 150 V, with clamping capacitor voltage (using PSPWM) and the waveform's harmonic spectrum of the output voltage. Figures 12 to 17 show the output voltage with clamping capacitor voltage and the output voltage with THD spectrum for the three basic LSPWM methods (PDPWM, PODPWM, and APODPWM). Table 3 shows the THD comparison between the various types of multicarrier modulation.

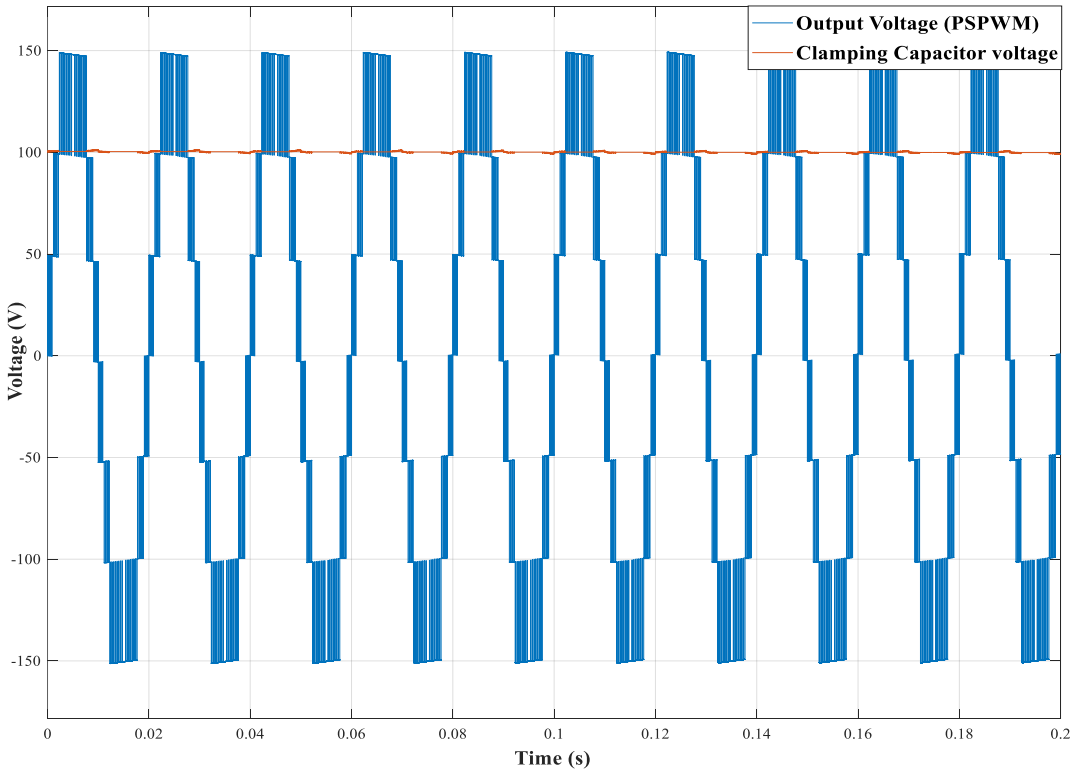

Figure 10. Output voltage and clamping capacitor voltage using PSPWM

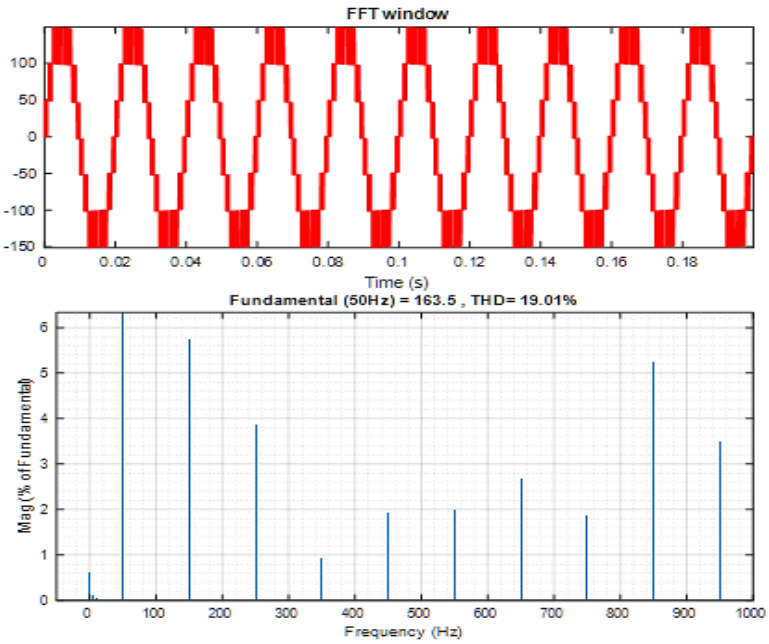

Figure 11. 7-level output voltage with THD utilizing PSPWM

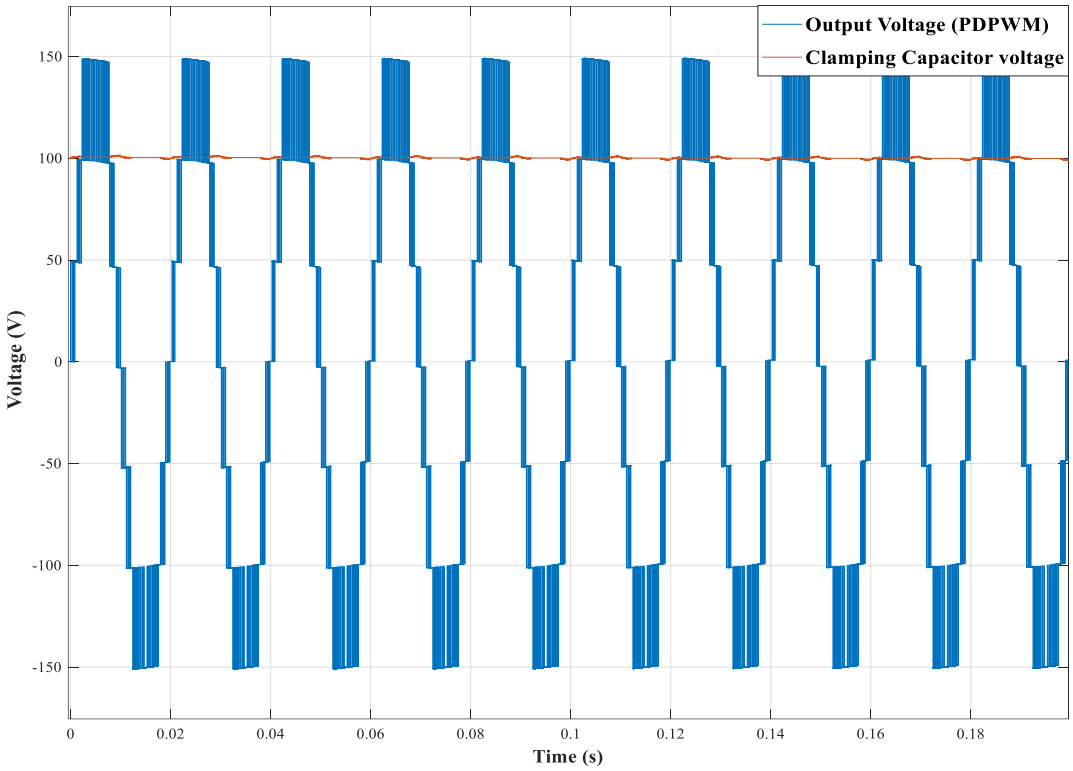

Figure 12. Output voltage and clamping capacitor voltage adopting PDPWM

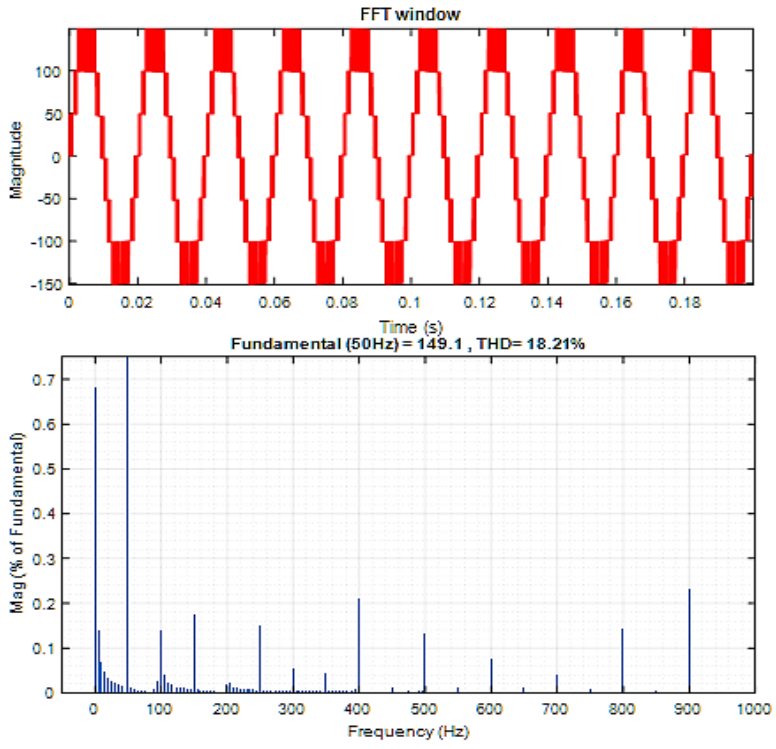

Figure 13. 7-level output voltage with THD applying PDPWM

Table 3. A comparision of THD in the output voltage with different modulation techniques

	Phase shift PWM	Level shifted PWM		
		PDWM	PODPWM	APODPWM
Seven level proposed topology	19.01%	18.21%	18.13%	18.38%

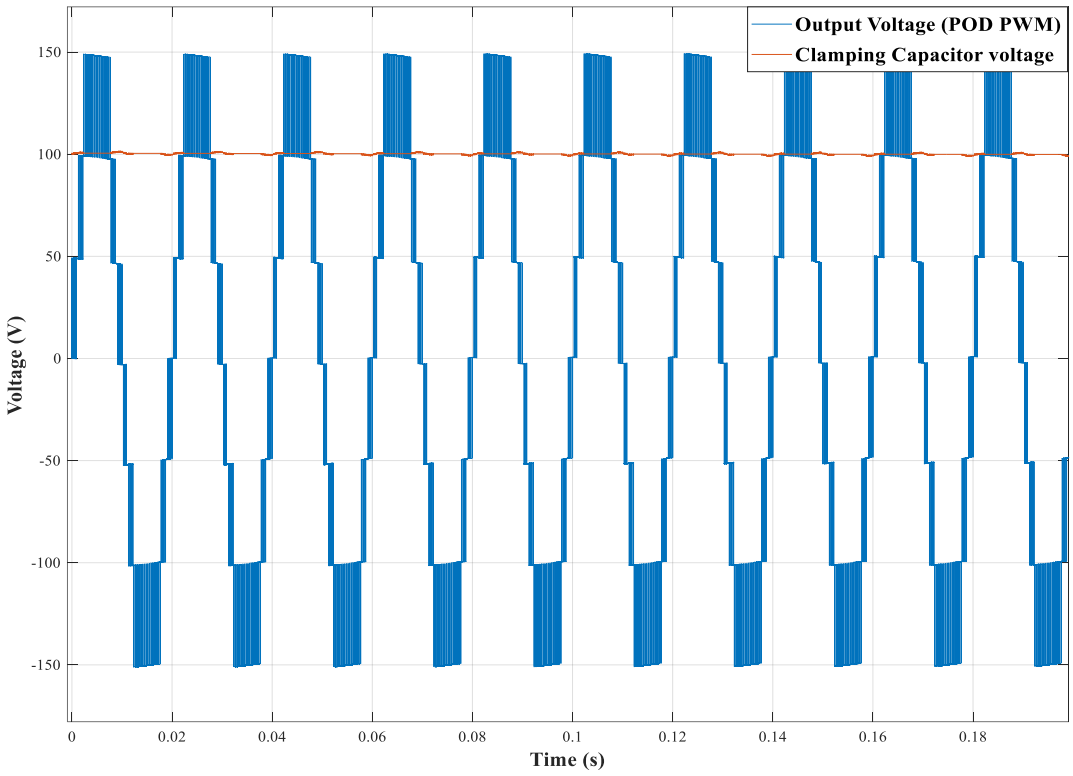

Figure 14. Output voltage and clamping capacitor voltage with PODPWM

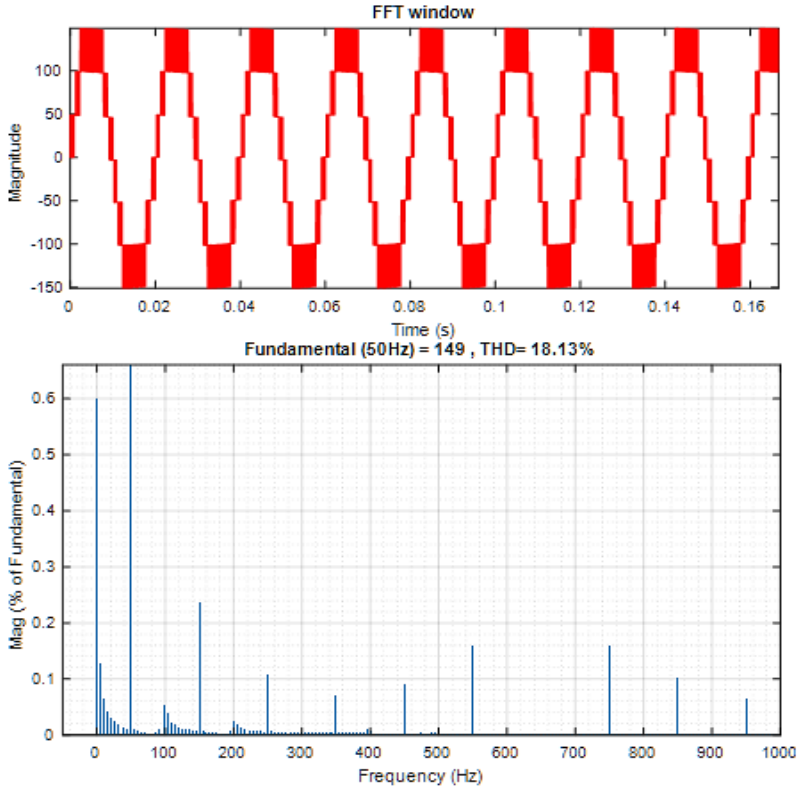

Figure 15. Waveform of seven output voltage levels utilizing PODPWM with THD

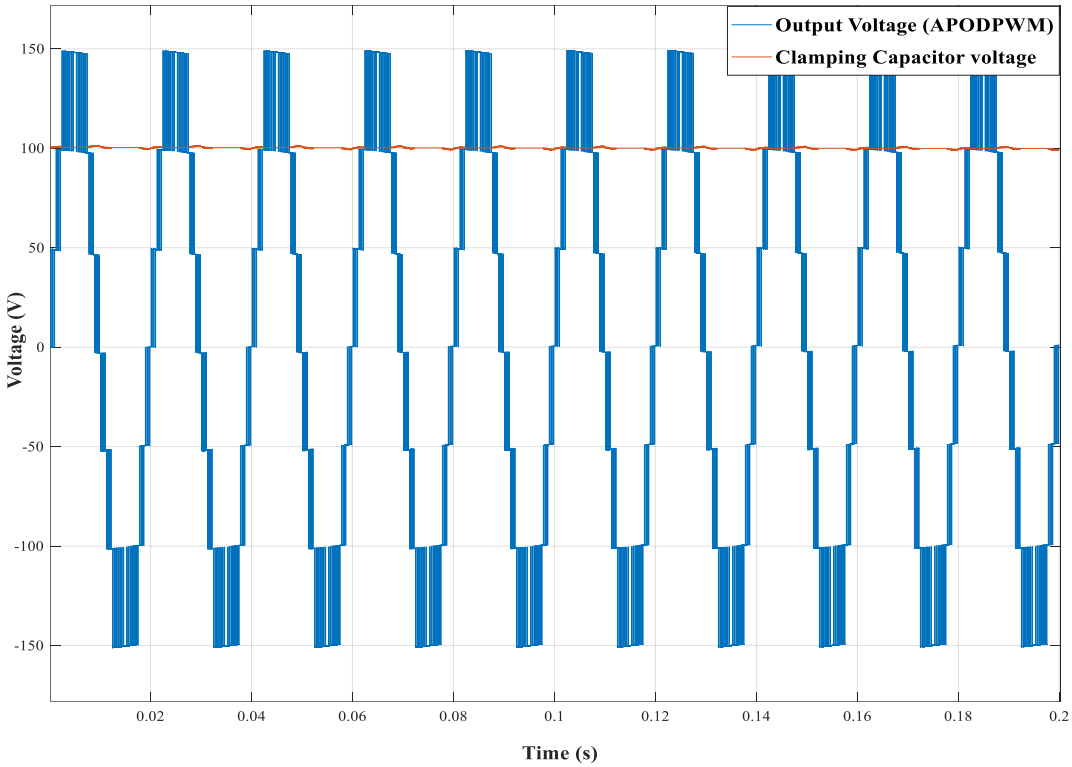

Figure 16. Output voltage and clamping capacitor voltage applying APODPWM

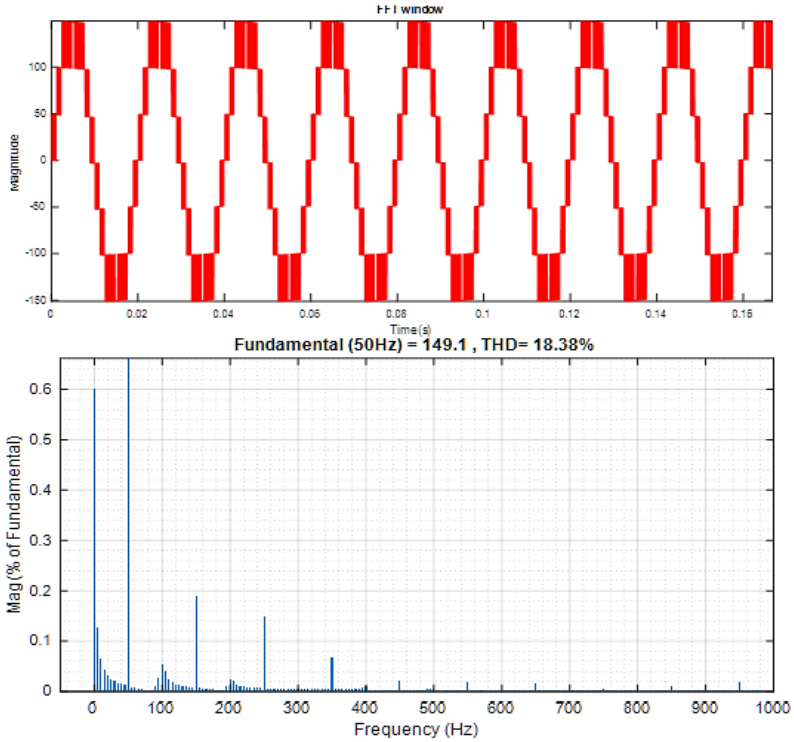

Figure 17. 7-level output voltage with THD using APODPWM

6. CONCLUSION

A new structure for multilevel inverters is presented in this research that makes use of fewer power components. The multilevel inverter's workings are explained in detail. The new topology and the most

common FC-MLI topologies were compared in detail. The topology has been explored in MATLAB/Simulink. It is also shown through simulation results that the proposed model works. FFT analysis gives a clear picture of the proposed model's effectiveness by measuring total harmonic distortion for various modulation techniques. As a result, the circuit's overall complexity is reduced while the system's performance is maintained. Because the proposed circuit has fewer components, it is both highly reliable and has low conduction losses.

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