

A novel step-up/step-down DC-DC converter based on flyback and SEPIC topologies with improved voltage gain

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ABSTRACT

A novel step-up/step-down DC-DC converter with improved voltage gain characteristics is suggested in this paper. The proposed converter combines flyback and single-ended primary inductance converter (SEPIC) converters. The voltage control loop design is simplified due to the use of only a single controlled switch. It has been discussed how switch duty cycle affects voltage gain. This relationship demonstrates that the proposed converter voltage gain is improved compared with flyback and SEPIC converters. However, compared to flyback and SEPIC converters, it has a higher voltage gain at any given duty cycle. The proposed converter operation is thoroughly discussed, the associated equations are derived, and its parameters are expertly designed. Moreover, it is designed to supply a DC load of 2.5 kW, 500 V, and 5 A. The proposed converter efficiency exceeds 84% under rated load conditions. Additionally, it is also presented as an adapter for electric vehicles. The waveforms associated with the simulation of the converter across the universal line voltage of 110-260 Vrms are shown. At both line voltages, the total harmonics distortions (THDs) of the line current are 17.12% and 27.26%, respectively. MATLAB/Simulink is utilized for validation in order to validate the topology for different applications.

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1. INTRODUCTION

With the rapid spread of renewable energy, smart grids, and electric vehicles, power electronics play the predominant role in their implementation within electric power systems [1]–[3]. Highly efficient converters especially isolated DC-DC converters are widely used for renewable energy integration, micro-grids, and electric vehicles [4]. There is a great concern in system operating efficiency by upgrading power converters; increasing their efficiency, reducing power losses including switching losses, which occur by reducing number of semi-conductor devices, and do the accurate control [5]. DC-DC converters are controlled to achieve a stable operation and maintain the output voltage at the desired value with the highest possible efficiency [6], [7].

Flyback is an isolated DC-DC converter, it is a buck-boost converter with coupled inductor at the input, flyback topology is shown in Figure 1(a), it consists of a controlled switch, magnetizing input inductance, a transformer, diode, and output capacitor. The flyback converter stores energy in the ON state of the switch and transfers that energy to the load in the OFF state. The terminal of its transformer is directly connected to the input voltage source when the switch is closed, storing the energy in the transformer. Transformer secondary is negative, and the diode is reversed-biased, the load is fed from the capacitor. When the switch is opened, the secondary voltage becomes positive, the diode is forward-biased, allowing the energy released from the transformer core recharges the capacitor and supplies the load [8]. Flyback primary is isolated from

its output, thus it has the capability to supply multiple outputs, all are isolated from its primary, and regulated with a single control. It can be operated over a wide range of input voltages, also it uses a low component count which results in a simplified required control [9], [10]. Flyback is an isolated converter mainly used in ultra-power applications and in PV systems to maintain a higher voltage gain [11]. This converter has a simple structure and low-cost components, so it is widely used in low-power domestic and industrial applications.

Single-ended primary inductance converter (SEPIC) is illustrated in Figure 1(b). SEPIC is classified as a non-isolated converter; its output is greater or less than its input with no polarity reversal. SEPIC is characterized by using two uncoupled inductors, one at the input, and the other at the output, the two inductors are coupled by a series capacitor to couple energy from the input to the output [8]. SEPIC tends to achieve higher output voltage. To overcome its drawbacks a high-frequency transformer can be used resulting in reduced switching stress, and also maintaining a continuous output current [12]–[15]. Due to SEPIC, all its energy is transferred via its series capacitor, thus it requires a high capacitance to handle its current. Also, its components count makes SEPIC control is difficult, and only compatible with low-varying applications.

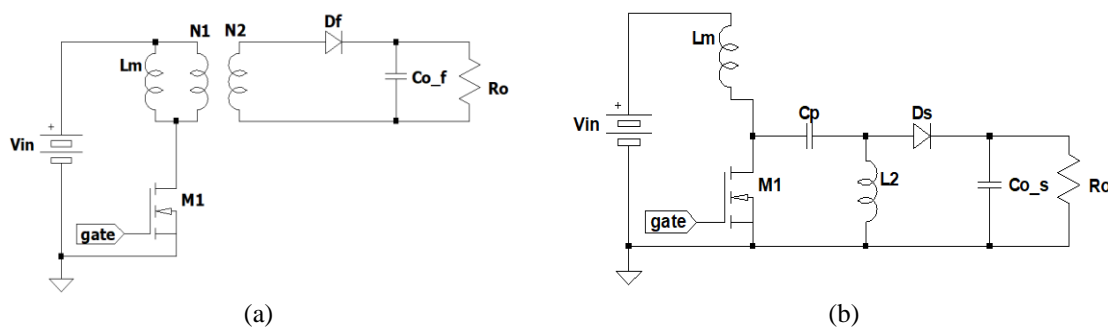


Figure 1. The component topologies of (a) flyback and (b) SEPIC converters

DC-DC converters play a dominant role in different applications such as the electric vehicles (EV), [16]–[20], to control the energy flow within EV systems, also increase the efficiency of energy transfer. Flyback is utilized in EV to provide insulation between low and high voltage sides. Kashif [16] has provided a flyback configuration for hybrid EV supplemented by PSPICE simulation, the flyback's transformer isolates source side and load side. Moreover, DC-DC converters are found in integrating renewable energy resources into the power system requires integration of power electronic converters together in addition to energy management strategies; resulting in higher efficiency, reduced weight, smaller size, higher power density, load transient response is faster, and lower cost and maintenance [21]. Basic converters' combinations are described in [22]; a comparison of features of three-port DC-DC converters possible topologies, it has proposed a discussion of different topologies, their features, advantages, and disadvantages of each topology.

Recently, the combination of two different DC-DC topologies becomes more attractive to the researchers. Zeng *et al.* [23] have presented new hybrid step-up converter topologies to overcome conventional boost converter with drawbacks concluded in large output voltage ripple and slow load transient response. The two proposed hybrid converters called “dual-path step-up converter (DPUC) [24]” and “KYC converter (KYC) [25],” are discussed and simulated under continuous conduction mode (CCM). Simulation results of that DPUC has the highest power efficiency under light loads conditions, fastest transient load response, and smallest voltage ripple while, KYC shows a neutral efficiency, output voltage ripple, and transient load response. However, the proposed converters use numerous controlled switches that need a complex control circuit to achieve the output voltage.

Chi-Wa *et al.* introduced two step-down DC-DC converter topologies have been proposed by [26]. They called switched-inductor-capacitor buck converter (SICBC) and 3-level buck converter (3LBC) were designed and analyzed. The two converters have been simulated and the results that SICBC has the highest efficiency under heavy loading conditions with the largest voltage level, while 3LBC had the smallest ripple voltage and highest efficiency under light loading conditions. Whereas the proposed circuits are only used in cases of high-frequency and low-power applications. Thus, the selected passive parameters need to be carefully designed to avoid their resonance.

Another step-down hybrid converter based on flyback-cuk converters (HFC) is proposed in [27] with reduced switching losses, higher duty cycles range over the same conventional converters' step-down capability, and improved power factor, HFC shows a better characteristic compared to single flyback or cuk converter which makes it applicable for many applications, for example, energy conversion. The proposed

converter can only be used to step down capabilities because it has two output terminals with inverted polarities which results in differentiated overall output voltage.

A forward-flyback topology is illustrated in [28]; two transformers are implemented to improve the efficiency and reduce conduction loss by reducing current stress on power components based on the concept of leakage energy recycling. Whenever the proposed converter is operated in the step-up, or step-down mode the voltage stress on the switch is clamped to the input voltage; and the leakage energy is recycled to the voltage source in step-up mode and to the capacitor or the voltage source in the step-down mode.

This paper proposes a novel step-up/step-down DC-DC converter based on combining both flyback and SEPIC converters. The proposed converter has improved voltage gain characteristic compared with the flyback and SEPIC converters. Moreover, the proposed topology uses only one controlled switch, two output diodes, one transformer, one coupling capacitor, and two inductors. There are two proposed versions of the converter as seen in Figures 2 and 3. Figure 2 shows that the proposed converter can feed two different loads simultaneously. Figure 3 can supply only one load with higher boosting capability that Figure 2. This is related to the fact that the load terminals is connected to the summation of flyback and SEPIC output terminals. The proposed converter uses low component counts which reduces the size of the PCB and the cost. The control loop will be very simple and has a simplified design, concerning with efficiency the proposed converter reaches about 85% at rated load conditions. A case study of an EV adaptor is presented within this work.

This rest of the paper is structured as follow: section 2 presents the proposed converter and its principle of operation. Section 3 presents the design parameters and voltage control loop; section 4 examines the simulation results together with efficiency. Section 5 illustrate a case study of using the proposed converter as an EV adaptor. Finally, section 6 concludes the paper.

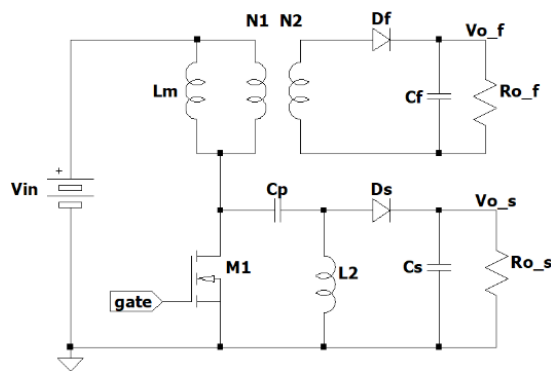


Figure 2. The proposed converter-two outputs

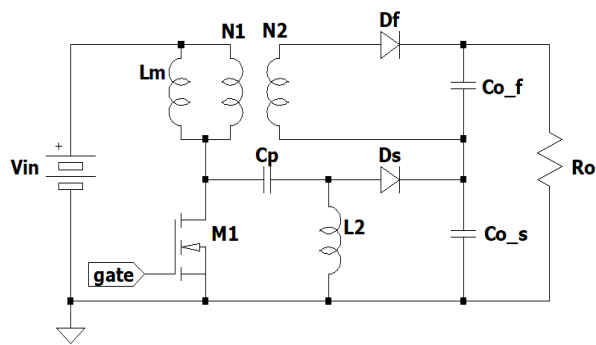


Figure 3. The proposed converter-single output

2. THE PROPOSED CONVERTER AND PRINCIPLE OF OPERATION

This paper discusses two cases of the proposed converter. The first case when the converter has two outputs, see Figure 2. Second, when the converter has only one output, as shown in Figure 3. The proposed converter comprises flyback and SEPIC converters. The input sides of both converters are merged together. Therefore, the input side comprises of a single controlled switch (M_1) which is connected to the DC power supply through a primary side of the flyback converter. The primary inductance of the flyback transformer represents the input inductance of the SEPIC converter. Moreover, the output side of the proposed converter has two different sides. The upper side which comes from the flyback converter, and the lower one which comes from the SEPIC converter.

To analyze the operation principle of the proposed converter in the two cases, there are some assumptions must be taken into consideration:

- The average voltage of C_p must be equal to the applied input voltage. But its average current must be equal to zero.
- The average voltage of L_1 and L_2 must be equal to zero. But its average current must not be equal to zero (operating in constant).

Case 1, two outputs converter: this converter is shown in Figure 2. In steady state, the proposed converter has two periods of operations based on the switch M_1 status. The output diodes (D_f , and D_s) are complementary to the main switch. The two periods are:

- When the switch M_1 is ON, the output diodes are both off as shown in Figure 4(a). During this period the inductance L_m is connected to V_{in} . Therefore, the inductor current starts raising up to its maximum value. Thus, the energy is stored in the inductor. The inductor current is given by (1).

$$\frac{dI_{Lm}}{dt} = \frac{V_{in}}{L_m} \tag{1}$$

moreover, the coupling capacitor is discharging its energy in L_2 through the main switch M_1 . Hence, the current of the inductance L_2 is given by (2).

$$\frac{dI_{L2}}{dt} = -\frac{V_{Cp}}{L_2} \tag{2}$$

- When the switch M_1 is OFF, see Figure 4(b), the output diodes are both on. During this period the inductance L_m is connected to the coupling capacitor C_p . Therefore, the inductor current starts falling to its minimum value. Thus, the energy stored in L_m will be transferred to C_p . The current in the inductor is given by (3).

$$\frac{dI_{Lm}}{dt} = -\frac{V_{o_s}}{L_m} \tag{3}$$

And the current in the inductor L_2 is given by (4).

$$\frac{dI_{L1}}{dt} = -\frac{V_{o_s}}{L_2} \tag{4}$$

For the two operating modes, it should be noted that the switch current is equal to:

$$I_{M1} = I_{L1} + I_{L2} \tag{5}$$

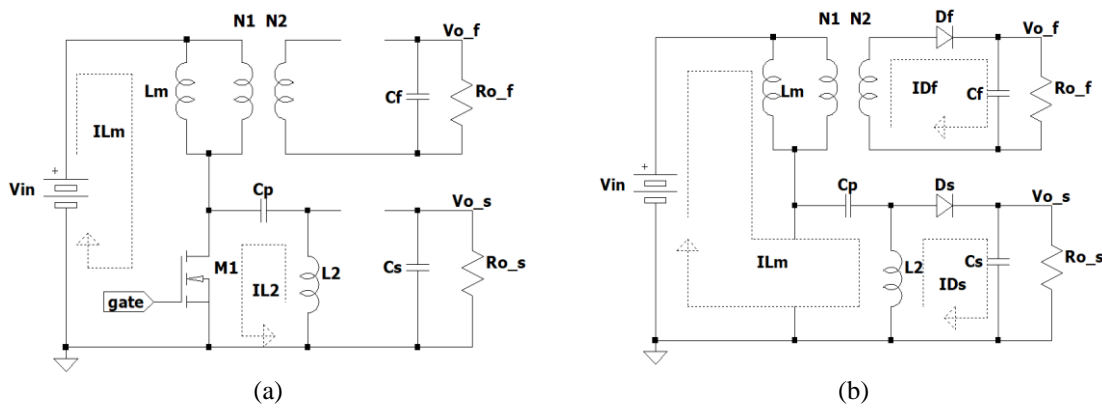


Figure 4. The switch of (a) M_1 is ON and (b) M_1 is OFF

Case 2, single output converter: This converter is shown in Figure 3. The operation principle of this converter is similar to the proposed one in case 1. The load voltage is given by the sum of the flyback capacitance voltage and the SEPIC capacitance-voltage. This is given by (6).

$$V_o = V_{o_f} + V_{o_s} \tag{6}$$

based on (6), the voltage gain of the proposed single-output converter can be obtained based on the relationships between the input and output voltages of both flyback and SEPIC converters. This is given by (7).

$$V_o = \frac{N_2}{N_1} V_{in} \frac{D_{M1}}{1-D_{M1}} + \frac{D_{M1}}{1-D_{M1}} V_{in} \tag{7}$$

thus,

$$\frac{V_o}{V_{in}} = \frac{N_2 + N_1}{N_1} \frac{DM_1}{1 - DM_1} \quad (8)$$

Figure 5 plots the voltage gain of flyback (dashed curve), SEPIC (curve with circles), and the proposed converter (solid curve) versus the applied duty cycle. One merit of the proposed converter (case 2) can boost up the load voltage at a low duty cycle. This is clearly illustrated in Figure 5. It also shows that the proposed converter has higher voltage gain compared with the other two converters: flyback and SEPIC converters.

Conventionally, both flyback and SEPIC converters are boosting up the output voltage if the duty cycle of the switch exceeds 50% (if the flyback transformer turns ratio is 1:1). Whereas the proposed converter has the ability to boost up the output voltage for the duty cycle lower than 50%. Moreover, it can be seen from the Figure 5 that, the proposed converter can buck the output voltage in case of low duty cycle.

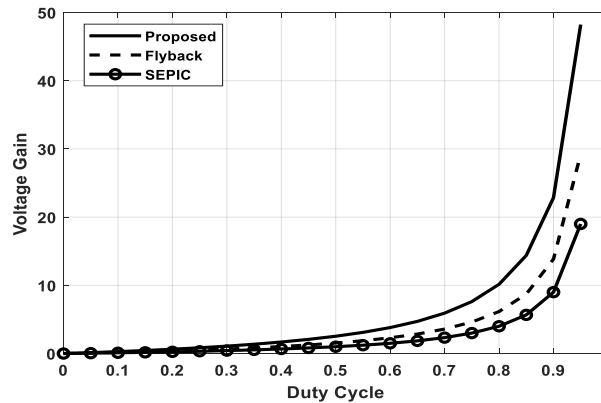


Figure 5. Voltage gain as a function of duty cycle of the proposed single output converter

3. DESIGN PARAMETERS AND VOLTAGE CONTROL LOOP

3.1. The selected parameters

The proposed converter is operated in continuous conduction mode and supplying a 2.5 kW load at 20 kHz switching frequency. The selected passive components of the proposed converter are computed as the following steps:

- The magnetization inductance (L_m) is designed to reduce the ripple in the primary current. Therefore, reducing the design complexity of the circuit's EMI filter [22]. The lower limit for this inductance is:

$$L_{m-min} = \frac{(1-DM_1)^2 R_o}{2f_s} \quad (9)$$

where f_s is the switching frequency, and R_o is the load resistance.

- The flyback output capacitance C_f plays an important role in reducing the output voltage ripple, setting the poles of the system transfer function, and implying the response of the supply to a sudden large change of the load current [23]. The minimum limit of flyback output capacitance is calculated by (10).

$$C_{o,f-min} = \frac{DM_1}{\frac{\Delta V_o}{V_o} R_o f_s} \quad (10)$$

Where, $\frac{\Delta V_o}{V_o}$ is the required output voltage ripple of the flyback.

- The transformer turns ratio (N_1/N_2) is set to determine the proposed converter duty cycle of the flyback converter [23]. This reduces the flyback diode voltage stress and the voltage stress on output capacitance. Then, the turns ratio can be calculated by (11).

$$\frac{N_1}{N_2} = \frac{V_{in} DM_{1-max}}{V_{o,f}(1-DM_{1-max})} \quad (11)$$

- The SEPIC inductance L_2 is designed to make the EMI filter is simpler [24]. The inductance is given by (12).

$$L_2 = \frac{V_o(1-D_{M1})}{\Delta I_2 f_s} \quad (12)$$

Where ΔI_2 is the desired current ripple L_2 .

- The SEPIC output capacitance C_{os} is designed to be:

$$C_{os-min} = \frac{\Delta I_2}{8\Delta V_{o_s} f_s} \quad (13)$$

- The SEPIC coupling capacitance C_p is designed to pass a high RMS current when it is compared to C_{os} , therefore, it should be selected to be (where L_{eq} is the equivalent of parallel inductance L_m and L_2):

$$C_{p-min} = \frac{L_{eq} I_2^2}{2\Delta V_{c-p}} \quad (14)$$

assume that the switch, Figure 4(b) is OFF, then the voltage across the loop is given by (15).

$$-V_{in} + V_{Lm} + V_{cp} - V_{L2} = 0 \quad (15)$$

This equation is valid for instantaneous and average voltage. But in steady-state conditions, the average voltages across L_m and L_2 are zero. Thus, $V_{cp} = V_{in}$ (note that this capacitance is large enough and this is the average voltage).

To prove the functionality of the proposed converter, it is designed for medium power applications with a rated power of 2.5 kW. Thus, the system specifications are set such as: input/output power, input/output voltages, and switching frequency, the other parameters are calculated based on the mathematical model presented so far.

3.2. The voltage control loop

The proposed converter with a single output, as shown in Figure 3, has a very simple voltage control loop to maintain the output voltage within the desired limit (V_{ref}). As seen in Figure 6, the measured feedback voltage is compared with a reference voltage. The PI controller is used to reduce the steady-state error of the comparison stage. The output of the PI controller stage is called the duty cycle of the main switch. Then, the gate to source voltage of the selected MOSFET is generated by using the PWM generator at a specific switching frequency (f_s). The PI parameters are: K_p is the proportional constant, K_i is the integral constant, and t is the time constant of the loop. They are selected by trial and error, and they are set to 0.051, 0.001, and 0.5, respectively.

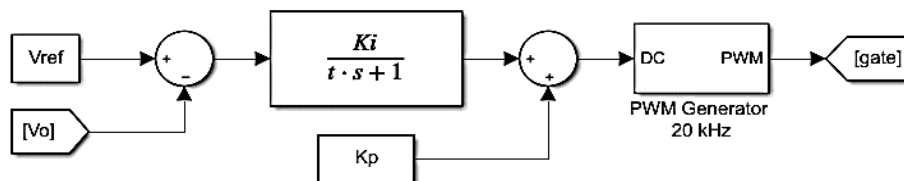


Figure 6. Voltage control loop

4. SIMULATION RESULTS

This section discusses the simulation results of the proposed converter as seen in Figure 4. Using MATLAB/Simulink R2020a, the results are validated. A maximum step size of 25 s and an ordinary differential equation (ode23tb) solver with a relative tolerance of 10^{-3} are used. The proposed converter will eventually operate at a steady state because the simulation time is set to 3 s. The simulation results are discussed for both converters. The parameters are selected based on the aforementioned discussion with some adjusted parameters as mentioned in Table 1 which summarizes the selected parameters for the 2.5 kW power application used in the simulation. These parameters are fit in different applications such as: electric vehicles adapters, micro-inverter applications, and hybrid renewable energy resources integrated with power systems. To verify the operation of the proposed converter, it is operated to step the output voltage in CCM mode with a constant switching frequency, constant duty cycle, and constant power.

The load voltage is measured in Figure 7. The reference voltage is set to 500 V in the voltage control loop, and it can be seen that from Figure 7 the load voltage is about 497 V. The error in this value is less than 0.6% which is accepted error percentage. Moreover, the voltage ripple in the output voltage ($\frac{\Delta V_o}{V_o}$) is less than 0.2%. The load current is shown in Figure 8. It can be seen that the load consumed a DC current with an average value of 5.35 A. The ripple in the load current is about 0.9%.

The voltage across the coupling capacitor in steady-state conditions is equal to the input voltage. From Figure 9, it is shown that the coupling capacitor voltage in average is equal to V_{in} with almost neglected voltage ripple. Meanwhile, the coupling capacitor current is plotted in Figure 10. It can be seen that the charging and discharging periods. When the current is lower than zero, this means the capacitor is in discharging mode, and its energy transfers to L_2 . And when it is higher than zero it is being charged through L_m . As discussed in the operation modes, the inductance L_m is being energized when the switch M_1 is on, thus, its voltage is higher than zero shown in Figure 11, and its current ramps up to its maximum value in Figure 12. On the other hand, when the switch is off, the inductor voltage polarity is reversed and its current starts falling down to its minimum value as shown in Figures 11 and 12. During the steady state operation, the average inductor L_m voltage must be zero.

Table 1. The selected parameters for the simulation

Simulation	Parameter	Description	Value	
Design Parameters	P_{in}/P_o	Input/output power	2.5 kW	
	V_{in}	Input DC voltage	200 V	
	V_o	Output voltage	500 V	
	I_o	Output current	5 A	
	R_o	Load resistance	100 Ω	
	f_s	Switching frequency	20 kHz	
	L_m	Magnetization inductance	100 μ H	
	N_1/N_2	Transformer turns ratio	1000/350	
	C_f	Output capacitance of flyback	720 μ F	
	C_p	SEPIC coupling capacitance	670 μ F	
	L_2	Cuk second inductance	800 μ H	
	C_S	SEPIC output capacitance	520 μ F	
	PI controller parameters	K_p	Proportional constant	0.051
		K_i	Integral constant	0.001
T		Time constant	0.5	
Two outputs converter	V_{of}	Flyback output voltage	500 V	
	V_{os}	SEPIC output voltage	20 V	
Single output converter	V_o	Overall output voltage	500 V	
For EV adapter application	V_{ac}	Universal line voltage	110-260 Vrms	

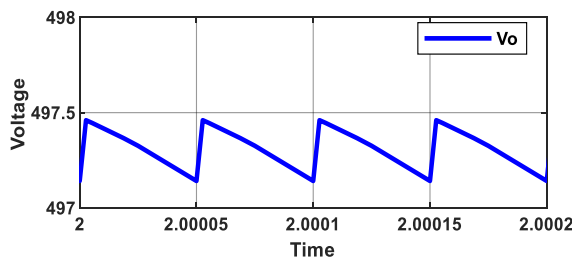


Figure 7. The output voltage

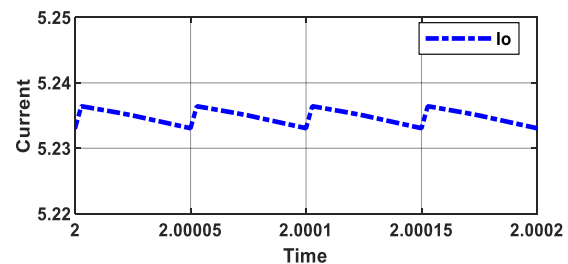


Figure 8. The load current

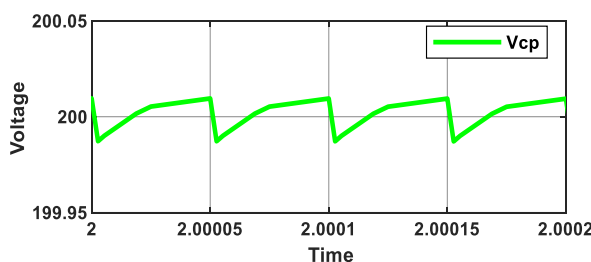


Figure 9. Coupling capacitor voltage

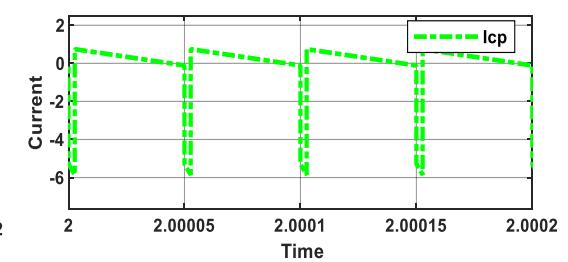


Figure 10. Coupling capacitor current

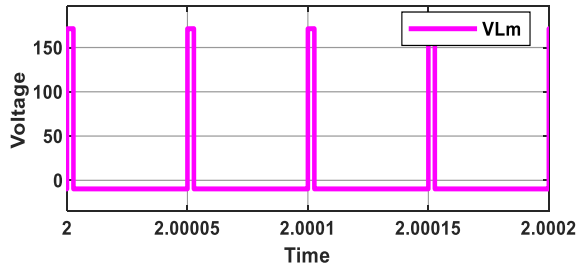


Figure 11. Inductor L_m voltage

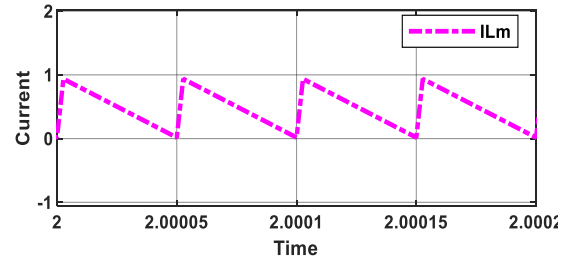


Figure 12. Inductor L_m current

Figure 13 plots the inductor voltage L_2 . As illustrated in the figure, the energy in the inductor is transferred to the coupling capacitor during the turn-on period of the main switch M_1 . But it stores energy during the turn-off time of the main switch. This can be seen in the current pattern illustrated in Figure 14. The currents in Figures 12 and 14 guarantee the CCM operation of the proposed converter.

The switch selection in the power converters is a vital issue. The switch must be able to block the voltage when its off and must be able to pass the current through its channel when it is on. Figure 15 shows the drain-source voltage of the main switch M_1 , in which it illustrates the switch blocking voltage capability. Meanwhile, the switch current is shown in Figure 16. Lastly, Figure 17 shows the variation of the proposed converter when the load is changed. As seen in this figure, when the load is increased the efficiency increases. The efficiency of the proposed converter reaches about 85% at rated load conditions (500 V, 5 A, and 2.5 kW).

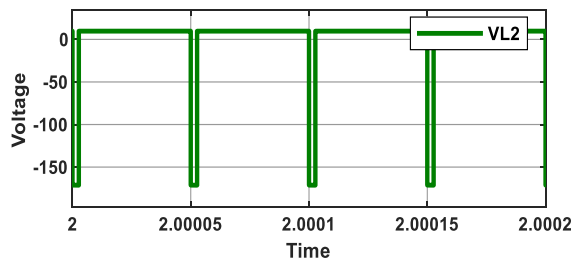


Figure 13. Inductor L_2 voltage

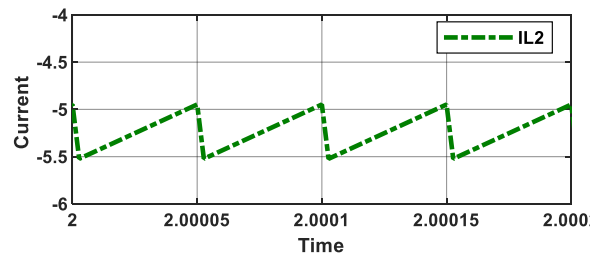


Figure 14. Inductor L_2 current

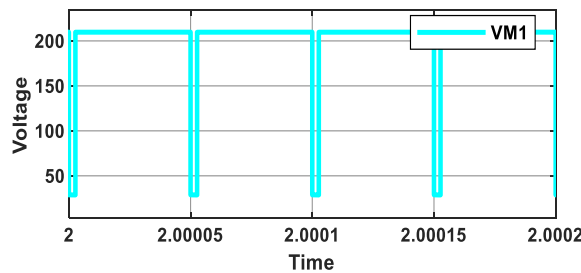


Figure 15. Switch M_1 voltage

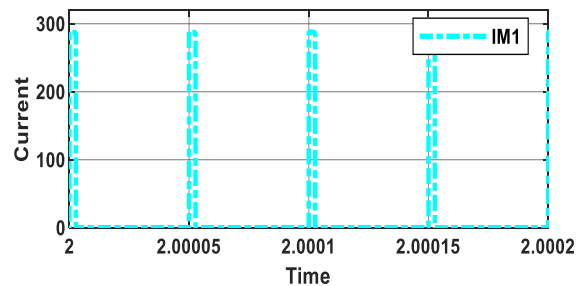


Figure 16. Switch M_1 current

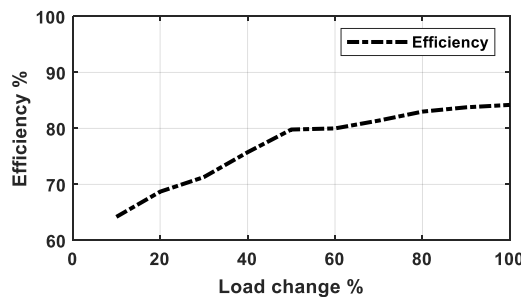


Figure 17. Efficiency of the proposed converter when the load change

5. THE PROPOSED CONVERTER AS AN EV ADAPTER APPLICATION

The proposed converter is used to build a 2.5 kW EV adapter over a universal line voltage of 110-260 V_{rms} as shown in Figure 18. The adapter comprised a diode bridge rectifier (DBR) as an interfacing stage between the AC power line and the proposed converter. The overall system in Figure 18 is simulated by MATLAB using the same parameters mentioned in Table 1. Due to the switching nature of the controlled switch at a specific switching frequency, this behavior affects the quality of the input AC line current. Figures 19 and 20 show the AC phase voltage and AC input current of the EV adapter at 260 V_{rms}, and 110 V_{rms}, respectively. The AC currents (brown) have approximately sinusoidal shapes.

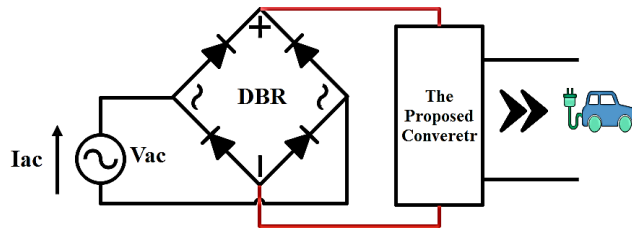


Figure 18. The use of the proposed converter in EV adapter

However, the total harmonics distortion (THD) of both currents are illustrated in Figures 21 and 22, respectively. By using the fast fourier transform (FFT) tool in MATLAB, the THD of the line current of Figure 18 is about 17.12% for high line voltage. Whereas the THD of the line current when the line voltage is low is 27.26%. Taking an in-depth look into both currents' harmonic components, see Figures 21 and 22, the THD can be further reduced by designing a proper input filter to reduce the third harmonics component. Whereas in the low line voltage, the third and fifth harmonics components have relatively high values. Hence, by attenuating the proper EMI filter these values will be reduced. In both cases of line voltages, the power factor of the line current is a poor value, and it needs to be corrected. This issue is left for future work.

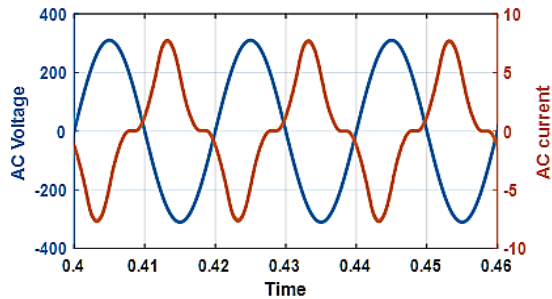


Figure 19. The line voltage (260 Vrms) and current

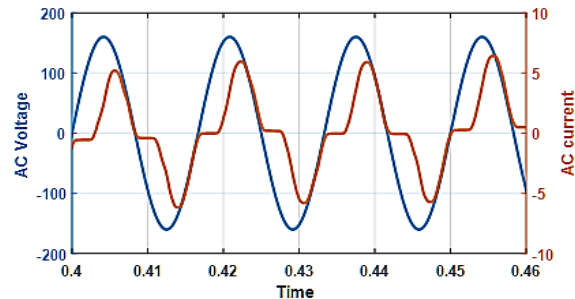


Figure 20. The line voltage (110 Vrms) and current

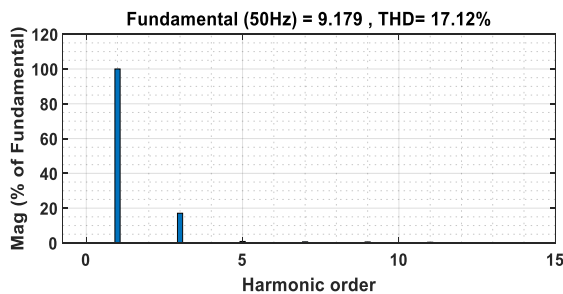


Figure 21. THD of the line current-high line voltage

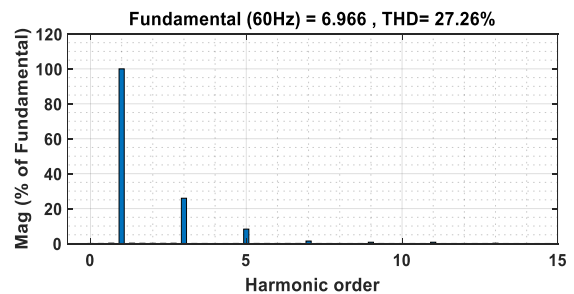


Figure 22. THD of the line current-low line voltage

6. CONCLUSION

This paper proposes a novel buck-boost DC-DC converter with improved voltage gain characteristics. The proposed converter is a combination of flyback and SEPIC converters. The proposed converter comprises only a single controlled switch which simplifies the voltage control loop design. The voltage gain as a function of the switch duty cycle has been discussed thoroughly. This relationship shows that the voltage gain of the proposed converter is superior to flyback and SEPIC converters. However, it has a higher voltage gain at any specific duty cycle compared to flyback and SEPIC converters. The operation of the proposed converter is discussed in detail and the related equations are derived, and its parameters are very well designed. The proposed converter is designed to feed A 2.5 kW, 500 V, and 5 A DC load. At rated load conditions, the efficiency of the proposed converter records a value of around 84.5%. Moreover, another effective application of the proposed converter in Electric Vehicles adapters. The converter is simulated over the universal line voltage 110-260 Vrms, and the related waveforms are presented. The THDs of the line current are 17.12%, and 27.26% at both line voltages, respectively. To verify the topology, MATLAB/Simulink is used for validation.




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