

Self-aligned hybrid carrier-based PWM for modular multilevel converters

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ABSTRACT

The self-aligned hybrid carrier-based pulse-width modulation (PWM) for modular multilevel converters (MMC) based on decentralized control is proposed in this paper. It is based on parallel cells in a submodule (SM) using self-aligned hybrid carrier-based PWM, which combines the concept of level-shifted carrier-based PWM (LSC-PWM) and phase-shifted carrier-based PWM (PSC-PWM) methods. By implementing a decentralized control system digitally, hybrid carriers align themselves. Each SM interacts with the other SMs and each parallel cell in an SM communicates with the other cells to generate hybrid carriers. The proposed control strategy makes advantage of the redundancy idea by adding or removing a cell in the case of cell malfunction and system reconfiguration. A current balancing method is incorporated into the decentralized control system to ensure current balance among parallel cells in an SM. The simulation results illustrate the effectiveness of the presented control method in piecewise linear electrical circuit simulation (PLECS) software.

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1. INTRODUCTION

Nowadays, a popular and high converter topology is the modular multilevel converter (MMC), which was initially introduced in [1]. The modular multilevel converter has become a significant and desirable option despite the availability of a variety of topologies, not only for high voltage direct current (HVDC) applications [2]–[5] but also for static compensator (STATCOM) [6]–[8] or motor drives applications [9]–[12]. The reason for this is because MMC provides greater flexibility, reliability, performance, and output quality as compared to conventional multilevel converters.

Submodules (SMs) are the key basic components that make up a modular multilevel converter, exhibiting modularity in the topology. Numerous SM circuit topologies have been presented in the literature to achieve various goals and applications [13], [14]. Among them, the half-bridge SM structure is widely used in MMC because of its simplicity and controllability. Figure 1(a) shows the typical diagram of a three phase MMC with half-bridge SMs. However, with the simple structure, in the case of a failure, the SMs with half-bridge configuration are fully removed from the circuit and replaced by another SM. This replacement might take a long time for reconfiguration and interrupt MMC operations. To address this issue, the parallel cells in SM (or interleaved half-bridge SM) configuration, which was introduced in [15], is an alternative because of its redundancy concept. In this topology, each SM is constructed by several parallel half-bridge legs (or called

by cells) as shown in Figure 1(b). This structure not only allows the total current to be shared across cells to increase quality output [16], but it also ensures the redundancy concept. For that reason, an appropriate modulation method is required to exploit the advantages of this converter.

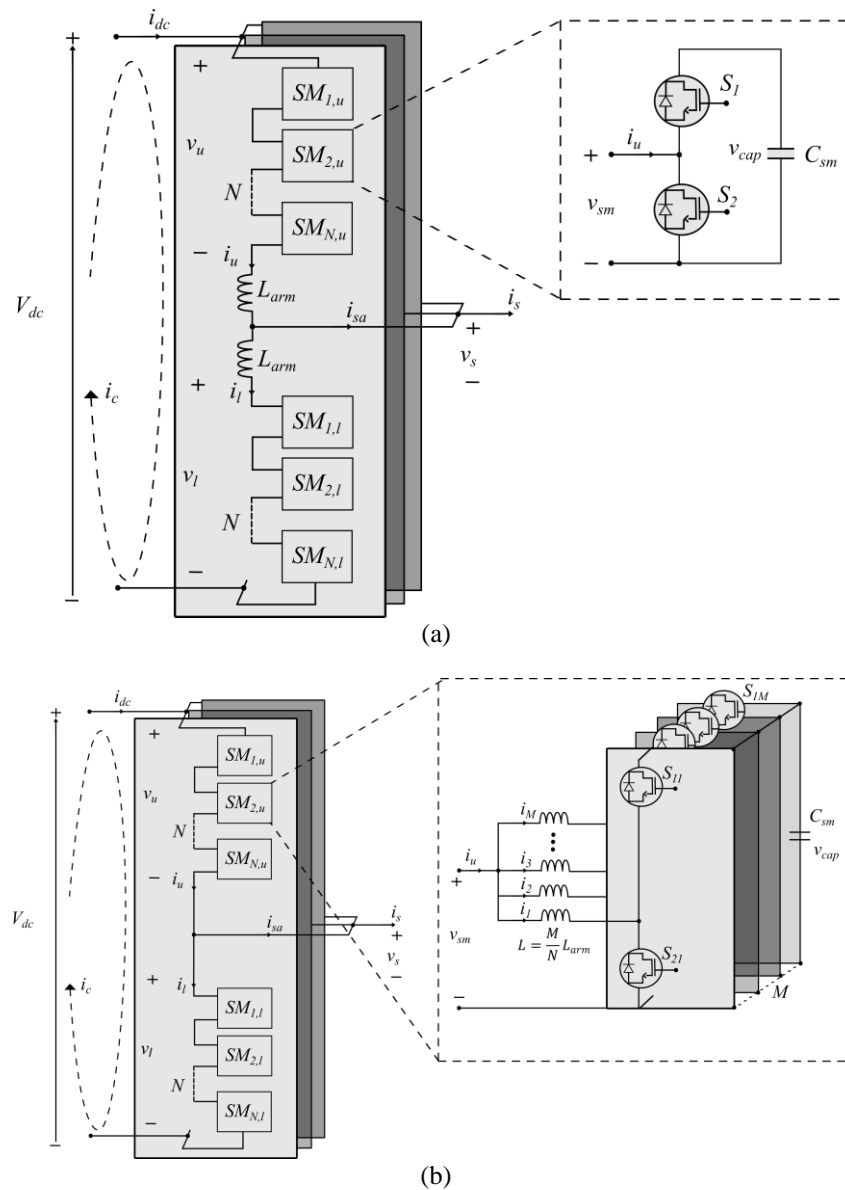


Figure 1. Schematic of (a) the MMC with half-bridge SMs and (b) the MMC with parallel cells in SM

Output levels of the MMC are achieved by adjusting the number of SMs inserted/bypassed into the upper and lower arms, whereas current quality is depending on the number of parallel half-bridge legs. Both of the above criteria are related to the MMC modulation scheme. The nearest level modulation (NLM), Space vector modulation (SVM), and multi-carrier based modulation are widely used modulation methods for MMCs [17]. The NLM approach is one of the most widely applied methods [18]. It allows a simple implementation and computation of gating signals while ensuring an arm voltage by selecting the nearest voltage level to the desired output voltage reference even regardless of the number of levels. However, the rounding voltage level process creates significant total harmonic distortion (THD) into the MMC's output voltage. SVM is a flexible modulation method for optimizing switching waveforms, however the algorithm's complexity grows exponentially with the number of levels [17]. The multi-carrier based pulse-width modulation (PWM) techniques is also an alternative for MMCs due to simple realization, less computational burden and improved

THD [14]. This technique is typically divided into two types: level shifted carrier-based PWM (LSC-PWM) and phase shifted carrier-based PWM (PSC-PWM). While the PSC-PWM approach employs carrier signals of the same amplitude and frequency that are phase-shifted horizontally, the LSC-PWM method creates carriers that are shifted vertically in their waveforms. All carrier signals in LSC-PWM could be phase disposition (PD-PWM), phase opposition disposition (POD-PWM), or alternative phase opposition disposition (APOD-PWM). PSC-PWM is generally used for MMCs because it achieves uniform power distribution across the SMs and is simple to implement, whereas LSC-PWM has lower THD but uneven power distribution [14].

To enhance the most advantageous characteristics of these modulation methods, several hybrids multi-carrier PWM techniques have been suggested. In [19], a hybrid PWM approach is developed that combines the best features of PSC-PWM and PD-PWM to address the issue of uneven power distribution while keeping reduced capacitor voltage ripple. The work in [20] provides a method base on the combination of PD-PWM, POD-PWM, and APOD-PWM methods to achieve lower THD than that of the PSC-PWM method. The other hybrid techniques are reported and analyzed in [14] to match with several aims and applications. It is noted that because of the horizontal/vertical shift and adjustment of the carrier waves, the implementation of these hybrid modulation schemes becomes more complex, requiring microcontrollers to perform significant computations. The decentralized control system might be an expected approach for hybrid approaches because of its modularity and flexibility.

The majority of MMCs are generally controlled by a central controller whose main responsibility is to balance the capacitor voltage, circulating current control, and modulation scheme. As the number of SMs and cells increases, the requirements for internal calculation may become more complex, which demands a large number of inputs and outputs as well as a high processing capacity of controller. Furthermore, if one of the SMs or parallel cells is damaged and has to be replaced during operation, the system is required to be reconfigured, and the central control unit must be recalculated the system. This process might disrupt the operation of power converter. Recent study has shown that as compared to centralized control, decentralized control of power converters constructed in the form of converter cells or modules, can reduce central controller computation and increase operational flexibility [21]–[24]. For the MMCs, the use of self-aligned carriers in [25] allows for the removal or replacement of malfunctioning SMs without disturbing main control while capacitor voltage balance is achieved. In [26], a distributed control architecture was presented in which the regulation of MMC internal dynamics and the synthesis of PWM signals are separated among local controllers to increase the flexibility of MMC system. The mentioned works regarding the decentralized or distributed architecture for MMC have focused on the half-bridge SM topology and conventional carrier-based modulation. Therefore, this research focuses on self-aligned hybrid carrier generation, which combines the LCS-PWM and PSC-PWM, based on decentralized control for the MMC with parallel SMs topology.

In this paper, the decentralized self-aligned principle for MMC with parallel cells in SM using the hybrid carrier generation combines the concept of PSC-PWM and LSC-PWM is proposed while cell currents balancing is achieved. The information of phase shifted angle and leg current between neighboring cells is exchanged at the cell level, whereas LSC-PWM carrier amplitude is shared at the submodule level. As a consequence, a self-aligned hybrid carrier with equally phase-shifted carriers for the cells in each SM and vertical-shifted carriers for each SM is synthesized. This scheme could reduce the computing burden on the central controller during normal operation or reconfiguration, maintains the MMC's redundancy concept, while ensuring the quality of output waveforms. Furthermore, currents across cells in an SM are shared and balanced by the current control stage, which aids in scaling the current output capacity. The results are verified through simulation on PLECS software to evaluate the effectiveness of proposed method.

This paper is organized as follows: the structure and operation principle of MMC with parallel SMs are presented in section 2. The explanation of the proposed method is explained in section 3. Section 4 shows the effectiveness of the proposed method by simulation results and the conclusion is given in section 5.

2. MATHEMATICAL MODEL AND OPERATION OF MMC

Figure 1(a) depicts the generalized schematic of a three-phase MMC with half-bridge SMs. Each phase leg of the MMC consists of two arms: upper and lower. N series SMs are connected in each arm. The SMs could be considered as controllable voltage sources that can be inserted or bypassed from the circuit. A half-bridge SM is made up of two controllable switches (generally IGBTs) S_1 and S_2 with antiparallel linked diodes and a capacitor C_{sm} . When an SM is inserted, the output voltage equal to capacitor voltage, otherwise it outputs zero. The upper and the lower arm voltage v_u and v_l can be varied between zero and the sum capacitor voltage of the arm by inserting the appropriate number of SMs. To avoid excessively high switching harmonics in the arm currents, each arm should be coupled with an inductor L_{arm} .

In this paper, the MMCs with parallel cells in SM are considered. Figure 1(b) depicts the schematic of a three-phase MMC with parallel cells in SM. It also consists of two arms; each one of them comprises a series connection of SMs. However, the SMs are created by wiring M half-bridge legs (or called cells) in

parallel to a common capacitor (C_{sm}). Each cell is connected to a common point via an inductor $L = \frac{M}{N} L_{arm}$, so the classical MMC topology's equivalent inductance are attained [16]. The output voltage of SM (v_{sm}) is the voltage between the common point of the leg currents and the below side of the capacitor. The relationship between the DC link voltage (V_{dc}) and the output voltages (v_s) can be expressed as (1) and (2).

$$\frac{V_{dc}}{2} - v_s = v_u \quad (1)$$

$$\frac{V_{dc}}{2} + v_s = v_l \quad (2)$$

Subtracting (1) from (2) results in (3).

$$v_s = \frac{v_l - v_u}{2} \quad (3)$$

The output voltages v_s drives the output current i_s as (4).

$$i_s = i_u - i_l \quad (4)$$

The voltage v_c that produces the circulating current inside the MMC i_c is:

$$v_c = \frac{v_l + v_u}{2} \quad (5)$$

$$i_c = \frac{i_l + i_u}{2} \quad (6)$$

the upper or lower arm voltage $v_{u,l}$ can be derived as a sum of SM voltages:

$$v_{u,l} = \sum_{i=1}^N v_{sm|u,l}^i \quad (7)$$

in a SM, submodule's voltage v_{sm} depends on the switching state of parallel cells:

$$v_{sm} = \frac{1}{M} \left(L \sum_{m=1}^M \frac{di_m}{dt} + R \sum_{m=1}^M i_m + \sum_{m=1}^M S_m v_{cap} \right) \quad (8)$$

where M is the number of parallel cells in a SM, i_m is the current of the m^{th} in an SM, S_m is gate signals of m^{th} cells and v_{cap} is capacitor voltage. The sum of cell currents inside an SM is actually the arm current can be expressed as (9).

$$i_{u,l} = \sum_{m=1}^M i_m \quad (9)$$

Figure 2 explains the operation principle of an upper arm MMC in case of $N=2$ and $M=3$ while Table 1 illustrates the switching states and output voltages of an SM with three parallel cells. As noticeable from (8), the voltage of SM will be synthesized depending on the switching state of the cells contained in that SM. In the case of M parallel-connected cells, the number of voltage levels for the SM voltage will be $M + 1$ between 0 to v_{cap} . For $N = 2$ and $M = 2$, each SM is a unipolar SM that could offer 4-level operation (0, $1/3v_{cap}$, $2/3v_{cap}$, and v_{cap}) depend on the switching states. The arm voltage is the total of the SM voltages as shown in (7), therefore it has a 7-voltage level. Similarly, the output voltage has a 13-voltage level of 13 based on (3). Compare to the classical MMC with $N = 6$ SM per arm modulated by $2N + 1$ modulation (which has the same number of switches per arm as the MMC with three parallel cells in SM), the output voltage levels are the same (13 levels).

It is also noted that because the current is shared by the cell's legs, the total rated current of the SM can be M times more than the conventional SM based on half-bridge topology giving this topology an advantage in terms of power scalability. Except for the submodule's voltage v_{sm} and arm current of the submodule, these equations for MMCs with parallel SMs are similar to those for a traditional MMC structure based on half-bridge SMs. As a result, the classical MMC control strategy presented in [27] is also applicable for an MMC with parallel cells in SM.

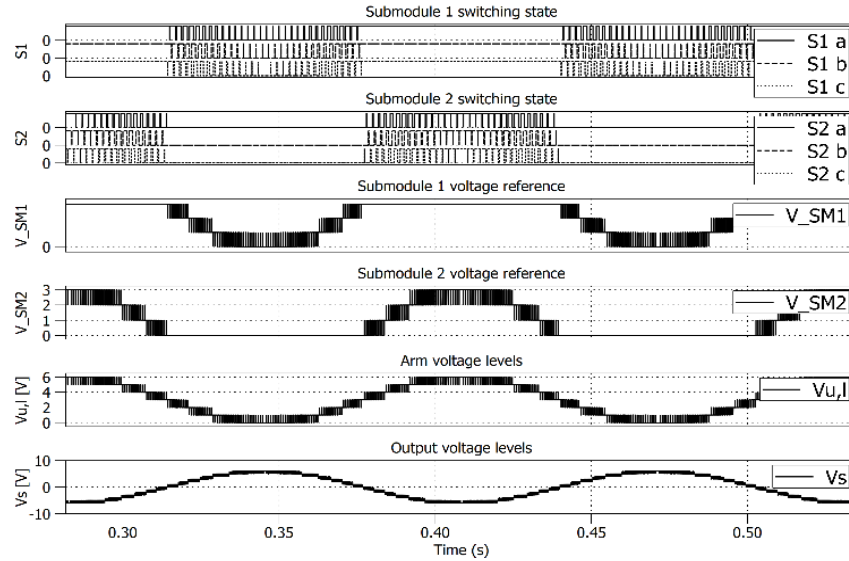
Figure 2. Operation principle of an upper arm MMC in case of $N=2$ and $M=3$

Table 1. Switching states and output voltages of an SM with three parallel cells

Operation stages	Switching states ($S_{11}S_{12}S_{13}$)	Submodule voltage (v_{sm})	Insert capacitor
1	000	0	Bypassed
2	001	$1/3v_{cap}$	C_m
3	010	$1/3v_{cap}$	C_m
4	100	$1/3v_{cap}$	C_m
5	011	$2/3v_{cap}$	C_m
6	101	$2/3v_{cap}$	C_m
7	110	$2/3v_{cap}$	C_m
8	111	v_{cap}	C_m

3. PROPOSED METHOD

The proposed control scheme for the MMC with parallel cells in SM is depicted in Figure 3. The typical MMC control has both high-level and inner-level control, with objectives such as circulating current control, sum capacitor voltages, submodule capacitor voltage balancing, output current control, and so on. An uneven current across parallel legs in each SM is another control objective to consider for the MMC with parallel cells in SM. For that reason, this method modifies the classical control scheme for conventional MMCs with standard half-bridge SMs to accommodate MMCs with parallel cells in SM, applies the definition of decentralized control to create the self-aligned hybrid carrier system and address the current balancing issue. A self-aligned hybrid carrier based PWM modulator and a current balancing control scheme based on the decentralized control method are included in the proposed method. The purpose of a decentralized self-aligned hybrid PWM modulator is to provide an appropriate triangular carrier system for the modulation scheme, while the current balancing control ensures a balanced current between each cell leg in an SM.

3.1. The self-aligned hybrid carrier's method

In the centralized control method, the central controller is employed to generate phase-shifted and level-shifted carriers for each cell leg and each SM. To create an appropriate carrier system, the number of SMs in each arm and the number of cells in each SM must be determined. In case of a cell or a SM fails, the system must be reconfigured. In terms of the decentralized control technique, the number of SMs in each arm and the number of cells in each SM are unknown and that could be changed during MMC operation in the case of failure. As a result, each SM interacts with two neighboring SMs and shares information about its amplitude level, and each cell in an SM exchanges phase angle and cell's current with the cells next to it. To achieve the balanced state, each carrier is locally adjusted on its angle and amplitude level based on the current values of the neighboring elements. The effectiveness of this communication scheme has been validated for the multiphase and multilevel converters [23].

Figure 4 shows the proposed communication scheme between SMs in each arm and cells in each SM for the MMC with parallel cells in SM topology. In k^{th} SM, the controller of m^{th} cell automatically calculates

updated value of its phase angle based on the information of nearby cells θ_{m-1} and θ_{m+1} . The updated rule is implemented using (10), at iteration i .

$$\begin{cases} \theta_m^{i+1} = \theta_m^i + K(\tilde{\theta}_m^{i+1} - \theta_m^i), K \in [0, 1] \\ \tilde{\theta}_m^{i+1} = \text{mod}(\theta_{m+1}^i + 0.5\text{mod}(\theta_{m-1}^i - \theta_{m+1}^i, 360), 360) \end{cases} \quad (10)$$

Similarly, each SM interacts with its neighbors and shares information as needed. The index number of $(k-1)^{\text{th}}$ SM (named count_in) is collected, updated, and assigned to count_out at iteration i of the k^{th} SM. It is repeated for every SM in order to get the total number N of active SMs in series. Based on the peak value of carrier amplitude of the previous SM, the local SM controller quickly computes the updated value of its peak value of carrier amplitude based on (11) and (12).

$$\Delta A_{base}^{i+1} = 2/N \quad (11)$$

$$A_k^{i+1} = A_{k-1}^i + \Delta A_{base}^i \quad (12)$$

Figure 5 illustrates the hybrid carrier system combining level-shifted and phase-shifted carriers which is generated by the proposed decentralized self-aligned hybrid carrier method. It is a combination of LSC-PWM, which is applied to series-connected SMs, while the PS-PWM is used to deal with interleaving carrier of parallel cells in each SM. Depending on the number of parallel cells in an SM, phase-shifted carriers are formed at an angle of $360/M$ degree spaced evenly from each other. Similarly, for the SMs, equal level-shifted carriers between 0 and 1 are created. The carriers at shifted levels, as shown, are in charge of inserting or bypassing the corresponding SMs in each arm, whereas the carriers at cell level are evenly shifted to operate the parallel cells. The purpose of phase shift is to equally distribute the switching state of cells in an SM, whereas level shift ensures that the number of SMs inserted into the circuit matches the required voltage level.

3.2. Current balancing control

As mentioned earlier, current sharing among parallel cell legs in each SM is a problem that must be addressed to ensure the performance and reliability of this topology. Figure 3 depicts a block diagram of the proposed current balancing control, while Figure 4 describes how current information is shared between cells to maintain balance. Instead of selecting the desired reference value for leg current (it could be altered when the number of parallel cells changes), the average of neighboring leg currents i_{m+1} and i_{m-1} is used as a reference input signal i_m^* for the considered current i_m in a parallel cell using the (13).

$$i_m^* = \frac{i_{m+1} + i_{m-1}}{2} \quad (13)$$

The computed value is compared to the local current i_m , and the difference is sent into a PI controller, which adjusts the i_m to the desired value i_m^* . This PI controller's output will determine the modified value $\Delta n, m_{u,l}$ which is added to the insert indices in classical control scheme. In this scheme, local controller regulates each cell current individually to the balance value. If a parallel cell fails, it is removed from the circuit, and the others use this approach to achieve a new balanced state. The advantage of this approach in terms of decentralized structure is that the redundancy concept is guaranteed when the number of cells or SMs could be changed. In the case of a reconfiguration process required, the deactivated cell or SM could be by-passed in order to keep a closed-loop communication chain.

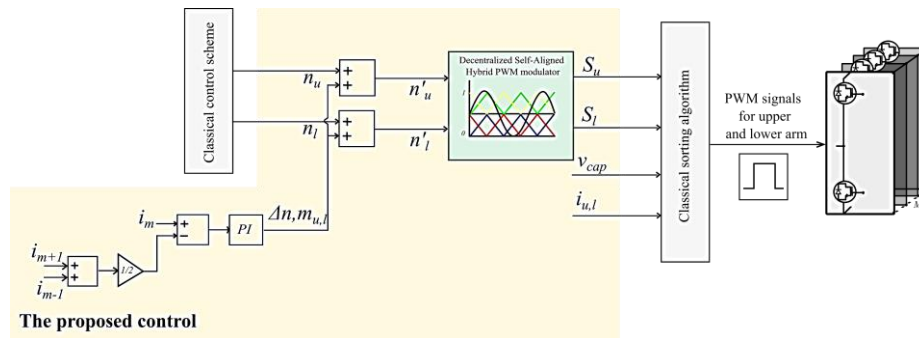


Figure 3. Proposed control scheme for the MMC with parallel cells in SM

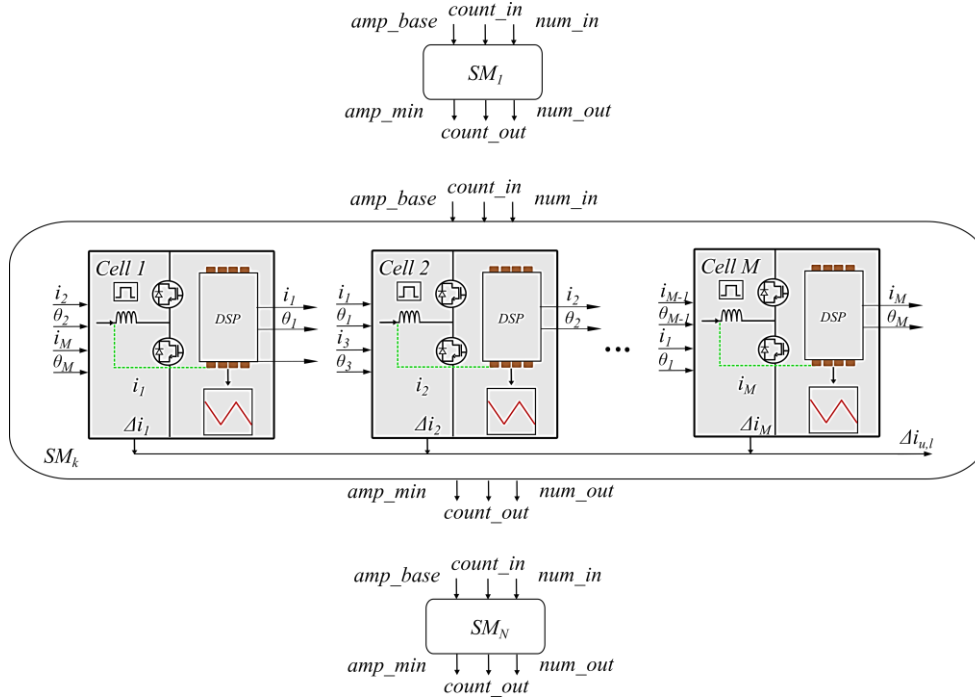


Figure 4. Communication scheme between SMs and cells

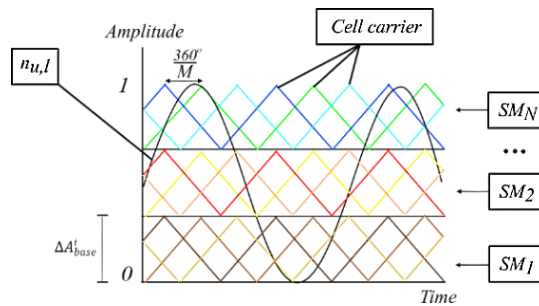


Figure 5. Hybrid carrier system combining level-shifted and phase-shifted carriers

4. SIMULATION RESULTS AND DISCUSSION

The proposed method is verified in PLECS by using MMC parameters shown in Table 2. There are two simulation scenarios presented. To begin, the operating characteristics of the MMC with parallel cells configuration are examined and compared to other configurations in the condition of steady state operation utilizing the self-aligning hybrid carrier and current balancing method. The functioning of the MMC in the scenario of system reconfiguration while changing the number of cells in each SM is then investigated to determine the system's reconfiguration capabilities.

Table 2. Simulation parameters

Parameter	Symbol	Value
DC-link voltage	V_{DC}	1000 V
Number of SM	N	2
Number of parallel cells per SM	M	3
Carrier frequency	f_c	1 kHz
Sorting frequency	f_s	1000 Hz
Capacitance in each SM	C	0.24 mF
Parallel cell resistor	R	2 Ω
Parallel cell inductor	L	64 mH
Modulation index	m	1
Grid line voltage (rms)	v_{grid}	400 V
Grid frequency	f_{grid}	50 Hz

4.1. Simulation results in steady state operation

The operational parameters of the MMC with parallel cells configuration are examined and compared to other configurations in steady-state operation using the self-aligning hybrid carrier and current balancing method in this scenario. Figure 6 indicates the hybrid carrier system created for MMC with two SMs per arm and three parallel cells per SM. It is noticeable that after some period of carrier wave, the required carrier system for modulation scheme is generated. It has six triangular carriers that are arranged vertically 0.5 amplitude apart for the SMs and horizontally 120 degrees apart in three cells.

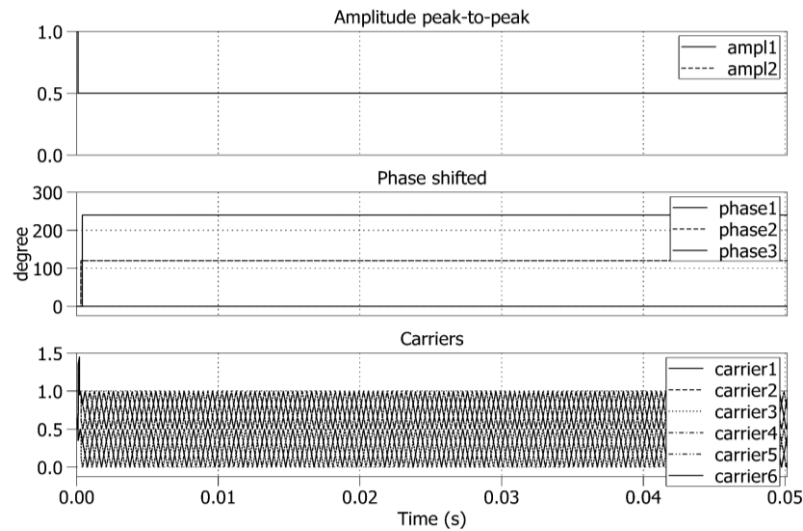


Figure 6. Hybrid carrier system for MMC with 2 SMs per arm and 3 parallel cells per SM

A classical MMC with two half-bridge SMs and six half-bridge SMs per arm was utilized to compare the operational characteristics of the MMC with parallel cells configuration. To maintain the equivalent arm resistor/inductor and SM capacitance, the parameters for the classical MMC remain unchanged. For the classical MMC, the modulation techniques are PD-PWM and APOD-PWM, whereas the self-aligned hybrid PWM is used for the MMC with three parallel cells per SM. It is noted that, the current balancing control methods are enabled during the simulation times. Table 3 shows the configurations to be compared.

Figure 7 depicts a comparison of arm voltages and output voltages for the classical MMC with conventional control techniques and the proposed self-aligned hybrid carrier PWM approach for MMC with parallel cells. In Figure 7(a), the MMC with two half-bridge SMs ($N=2$) is presented with PD-PWM modulation. In this case, 3 ($N+1$) voltage levels in the arm voltage are generated, and 5 ($2N+1$) output voltage levels are synthesized, with a THD of 31.5%. The output waveforms of the MMC with 6 half-bridge SMs ($N=6$) modulated by APOD-PWM and PD-PWM methods, are shown in Figures 7(b) and 7(c) respectively. The output voltage levels are 7 ($N+1$) and 13 ($2N+1$), respectively, with THD values of 18.5% and 10.8%. The last one, Figure 7(d) illustrates the output waveforms of the MMC with two SMs per arm and three parallel cells per SM ($N=2$ and $M=3$) controlled by the proposed method. It can be seen that the number of out voltage levels (13 voltage levels), which is synthesized by SM voltage levels, has been significantly increased as compared to the classical MMC with two half-bridge SMs. THD value of this topology with the proposed method is 12.1%, which is less than that of MMC with six SMs modulated by APOD-PWM. In terms of the number of power switches in each arm, this topology has the same number as classical MMC with $N=6$.

Table 3. Configurations to be compared

Configuration	N	M	Modulation
1	2	1	PD-PWM
2	6	1	PD-PWM
3	6	1	APOD-PWM
4	2	3	Proposed method

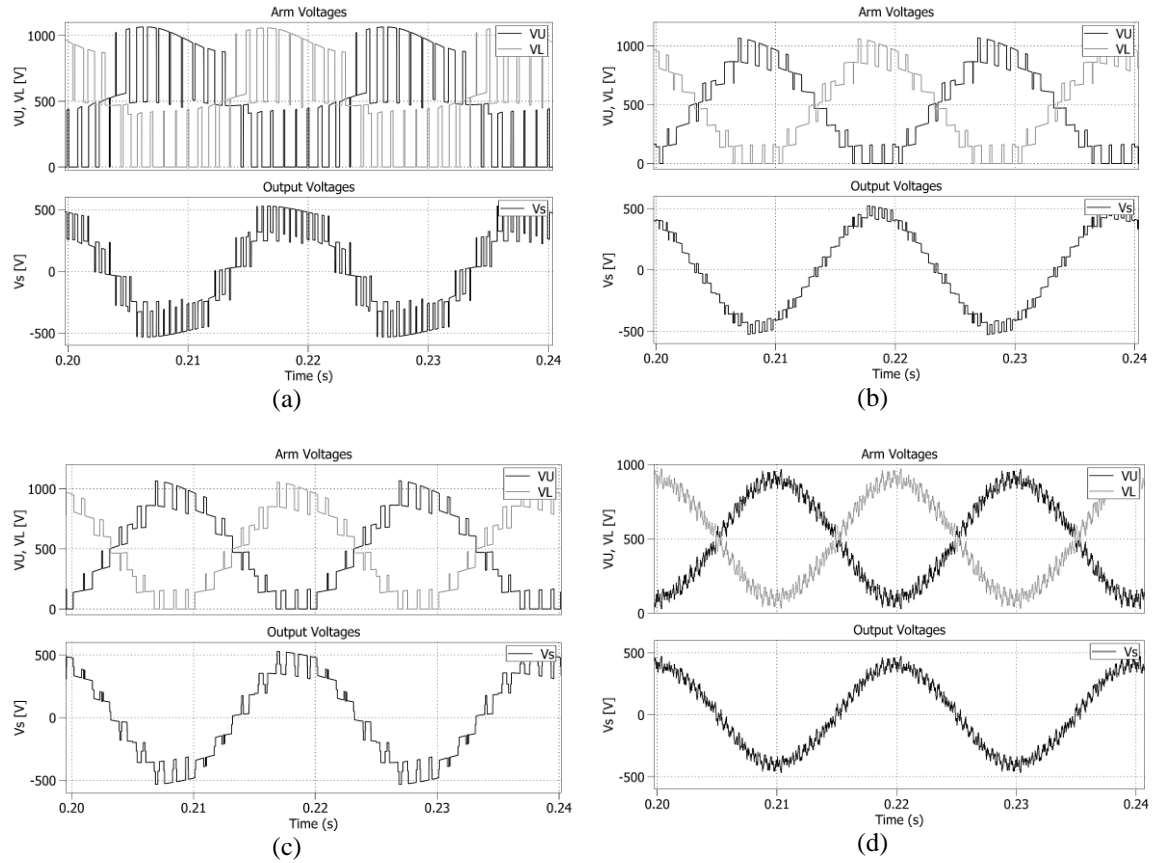


Figure 7. Arm voltages and output voltage of MMC with (a) configuration 1, (b) configuration 2, (c) configuration 3, and (d) configuration 4

Figures 8(a) and 8(b) show the arm current, output current, and circulating current of a classical MMC with two half-bridge SMs and an MMC with two SMs and three parallel cells using the proposed methods. According to FFT analysis, the output current THD of MMC with two SMs and three parallel cells utilizing the proposed methods is less than that of the classical MMC (12.2% versus 14.5%). Although the control strategies for dealing with circulating current are beyond the scope of this paper, it can be shown that the circulating form in the case of the proposed method is less polluted and has a lower amplitude than that of traditional MMC with two SMs per arm.

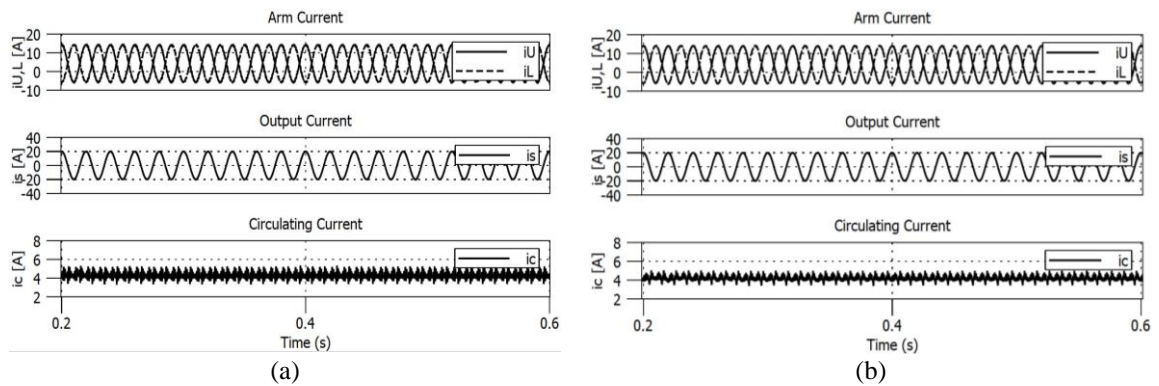


Figure 8. Arm current, output current and circulating current of MMC with (a) configuration 1 and (b) configuration 4

To demonstrate the cell current's response to the current balancing control approach, current balancing approach will be disabled in the simulation scenario with $t=0.4$ s as shown in Figure 9. Before the proposed method is turned off, the current in each cell leg is controlled and achieves the equilibrium value. When the current balancing technique is disabled, there is an unbalanced distribution of parallel cell currents in one SM, which may result in a change in total current THD (from 4.37% to 4.2%). The simulation results demonstrate that the proposed approach for the MMC works reliably in the state-state scenario.

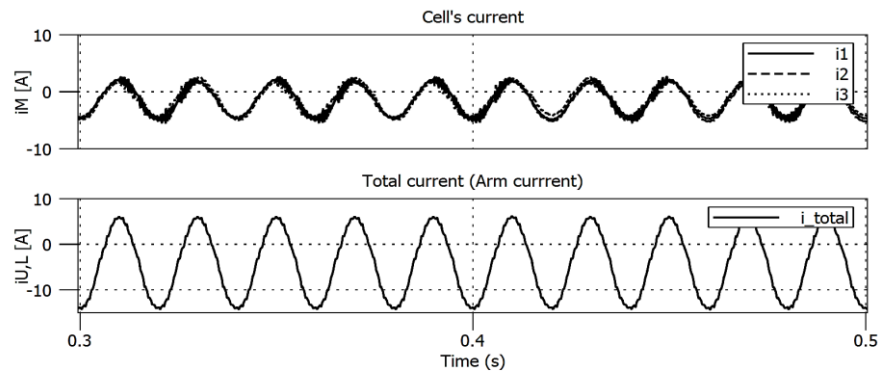


Figure 9. Cell current's response to the current balancing control approach

4.2. Simulation results in reconfiguration scenario

This scenario depicts the behavior of the MMC when one cell in an SM is removed or added. When a cell malfunctions and has to be replaced, the addition or removal of a parallel cell during operation is available by this scheme. This gives the system a sense of redundancy. The simulation process begins with all cells in an MMC SM activated. By using a current balancing control method, all cell currents reach a balanced condition in the steady state. At $t = 0.3$ s after reaching steady state, one cell (3rd cell) in an SM is removed. As a result, a new carrier system must be created for the modulation scheme. The capabilities of the re-aligned carrier technique have been illustrated in [23]. In this situation, an SM can only operate with two cells. It means that the total current flowing through that SM must be distributed equally. The cell current that passed through the removed cell must be shared by the remaining two cells. As shown in Figure 10, at $t = 0.3$ s, because the current through the deactivated cell is shared, the RMS value of the remaining cell increases from 2.8 A to 4.2 A. At $t = 0.5$, this cell is inserted (or replaced), and the SM returns to its initial state of three cells, the currents between them are recovered to balance. The time response is quite fast (0.015 s) and the overshoot is small. During the reconfiguration process, this control mechanism ensures that the system remains operating normally. The total current (arm current) waveform and quality remain unchanged. The simulation results demonstrate that the proposed method works well when the number of cells in each SM is changed. The proposed method works similarly as the number of cells in each SM increases. This ensures an increase in the converter's output current capacity.

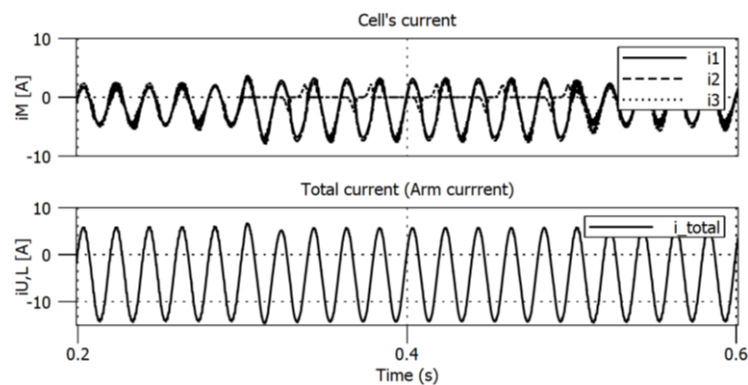


Figure 10. Cell current's response in the reconfiguration scenario

5. CONCLUSION

The self-aligned hybrid carrier-based PWM for the modular multilevel converters with parallel cells in submodule (SM) based on the decentralized control structure has been proposed in this study to increase the modularity and flexibility in case of system reconfiguration. In this structure, hybrid carriers self-align based on the information exchanged between each SM and each cell. The proposed method has the advantage that, because of the decentralized control structure, the SMs and cells could communicate with each other to exchange information, resulting in normal operation based on the number of cells and SMs connected, therefore increasing modularity and flexibility. Furthermore, when a cell is damaged and has to be removed, the system is immediately reconfigured thanks to the self-aligned carriers. The control loop also includes the current balancing method. The simulation results on PLECS show that the current across the cell legs in each SM is regulated and well balanced in the steady state and reconfiguration operating conditions, while the output voltage and current quality are ensured.

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