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Discontinuous conduction mode approach of ultra-lift DC-DC converter based on three windings coupled inductor

Saeed Hasanzadeh[1], Milad Asadi[1] , Tole Sutikno[2,3]
[1]Department of Electrical, and Computer Engineering, Qom University of Technology, Qom, Iran
[2]Department of Electrical Engineering, Faculty of Industrial Technology, Universitas Ahmad Dahlan, Yogyakarta, Indonesia
[3]Embedded System and Power Electronics Research Group, Yogyakarta, Indonesia

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ABSTRACT

These days, DC-DC boost converters play an essential role in a variety of applications. Therefore, a variety of techniques were proposed in the literature to achieve the highest voltage gain. A large number of passive elements are typically used in high-voltage DC-DC converters. Increasing the order of the system would make modeling and controlling the output voltage of the converter more complex. This paper examines an ultra-lift DC–DC converter using a three-winding inductor and a super-lift construction in discontinuous conduction mode (DCM). This converter provides substantial voltage gain by utilizing the three-winding coupling inductor topology without increasing the duty cycle or passive circuit parts. Because the DCM operation mode occurs in the converter, it is necessary to investigate and analyze it. The DCM operation mode of an Ultra-Lift converter is examined in this study, and then simulation results are shown to validate the equations.

Corresponding Author:

Saeed Hasanzadeh
Department of Electrical, and Computer Engineering, Qom University of Technology
Qom, Iran
Email: hasanzadeh@qut.ac.ir

1. INTRODUCTION

Recently, global warming, environmental issues, and the depletion of natural fuels such as gas, oil, and coal have led researchers worldwide to consider using renewable energy sources [1]–[7]. Since the voltage generated by the renewable energy sources is in DC form, it is necessary to use an inverter to convert the output voltage of these sources to the voltage required by consumers [8]–[11]. It should be noted that the required voltage of the DC link of single-phase and three-phase inverters is equal to 400 and 700 volts, respectively [12]–[14]. However, the voltage generated by renewable energy sources is not enough to power the DC inverter link. To attain a higher output voltage from these sources, it is mandatory to utilize DC-DC converters with high voltage gain [15]–[20].

In the literature, boost converters with various structures have been proposed so far. For example, the traditional boost converter is one of these converters. In this converter, high values of the duty cycle are required to attain high voltage gain values. So, this increases the voltage and current stress on the components and switches and restricts the dynamic response of the system, resulting in reduced converter [21], [22]. Also, increasing the duty cycle reduces the amount of converter controllability [23]–[25]. A variety of methods can be deployed to increase the output voltage. One of these methods is to consider switching capacitors to achieve high values of voltage gain. These converters have high voltage gains and are considered a subset of supercharged converters [23], [24]. However, the high number of switches, complex control, and high cost are among the disadvantages of these converters [15]. Using a voltage multiplier circuit

in low-frequency rectifiers is a solution for increasing the output voltage [26], [27]. Applying this technique to high-frequency, isolated DC-DC converters for high-voltage applications (up to a few kV), such as traveling wave tube amplifiers (TWTA), causes transmission wave amplifiers. It can reduce problems with high-frequency and high-voltage transmission power [28]. In this method, higher voltage gains can be achieved by expanding the voltage multiplier circuit.

Another well-known approach to increasing the output voltage is the voltage lift method [29], [30]. This method can be used normally or in layers. In this method, the amount of output voltage increases during an arithmetic process. In its n-floor structure, a switch, a 2n capacitor, and a 3n-1 diode are used. To increase the voltage as much as possible, a multi-stage circuit can be used, in which case the output of the first floor is the input of the second floor, and therefore its gain increases. The use of an inductor is another solution that has been proposed to attain a high voltage gain [31]. The consideration of a coupling inductor can dramatically reduce the problem of reverse converter recovery. When the switches are turned off, the leakage energy from the mating inductor causes sparks. One way to eliminate leakage energy and control sparks is to use a small resistor with a capacitor [32]. One of the disadvantages of converters that use inductance in their structure is the high current stress on the equipment at high power values, which significantly reduces the efficiency of the converter. The interleaved technique is a good solution to solve this problem and reduce the input current ripple [33].

In most cases, it is preferable to use inverters in parallel. This consideration aids in distributing both the current and heat transfer of the switch and achieving high output voltage and efficiency values [34]. One of the disadvantages of solar panels is the lack of power due to the limited number and connections of the solar panel series. Keep in mind that when connecting a series of solar panels, if a module fails, the system will fail. To solve this problem, DC-DC interlay converters can be used, increasing the efficiency and reliability of the system [35], [36]. If the discrete operation of DC-DC converters is guaranteed, as much output voltage as possible can be achieved without changing the structure of the converter. Discrete operating mode typically occurs in DC-DC converters, rectifiers, inverters, and other converters that use single-quad switches. Some converters are designed to operate in DCM mode at all loads. The amount of output voltage in this mode is determined by the load values. This is a defect from a control point of view because it may lose control of the output if the load is lifted. On the other hand, in converters operating in DCM mode, poles and zeros are located at high frequencies.

In this paper, the performance of an amplifier DC-DC converter is investigated, considering a three-winding inductor and voltage multiplier circuit. The structure of the paper is organized as follows: in section 2, the working modes of the converter in DCM are examined. In section 3, the steady-state analysis of the converter in discrete operating mode will be presented. In section 4, the optimal design of the circuit elements is presented. Section 5 also presents the simulation results performed in the MATLAB/Simulink software environment. Section 6 concludes the paper.

2. CONVERTER OPERATION ANALYSIS IN DISCONTINUOUS CONDUCTION MODE (DCM)

The topology of the converter under study is presented in Figure 1. The converter includes a constant voltage source V_g, a switch *S*, a three-winding coupling inductor, five capacitors, and five diodes. The coupled inductor is modelled as an ideal transformer with a primary winding, two secondary windings, and a L_m magnetizing inductor parallel to the primary transformer. The primary winding has N_1 turns while the secondary windings have N_2 and N_3 turns. The winding ratios of the inductor are $N_{21}= N_2/N_1$ and $N_{31} = N_3/N_1$. The converter in DCM mode consists of five modes in one switching period. The following hypotheses are considered: All equipment is ideal, and the converter is in a steady-state operation. The inductors and capacitors are of large values such that the inductor's current and capacitor voltage are constants (an assumption) for the switching period.

2.1. Switch on

2.1.1. Mode 1 [to-t1]

For this interval [*to-t1*], the switch S is on. Diodes 1 and 5 are in direct bias and are on. *Diodes 2, 3,* and *4* are reverse biased and off. In this operating mode, the magnetizing inductor current i_{lm} increases linearly. Capacitor C_1 is charged via diode 1. This operation ends when the switch current becomes equal to the magnetic inductor current. The current path of this model is shown in Figure 2.

2.1.2. Mode 2 [t1-t2]

As demonstrated in Figure 3, switch *S* is still on during the time interval [*t1-t2*]. The magnetizing inductor current continues to increase linearly by the power supply. In this mode, *diode 5* is in direct bias and is on, and *diodes 1, 2, 3,* and *4* are reverse bias and off. During this time, the output capacitor C_o is still charging via capacitors C_2, C_3, and C_4. This mode of operation terminates when the switch *S* is switched off.

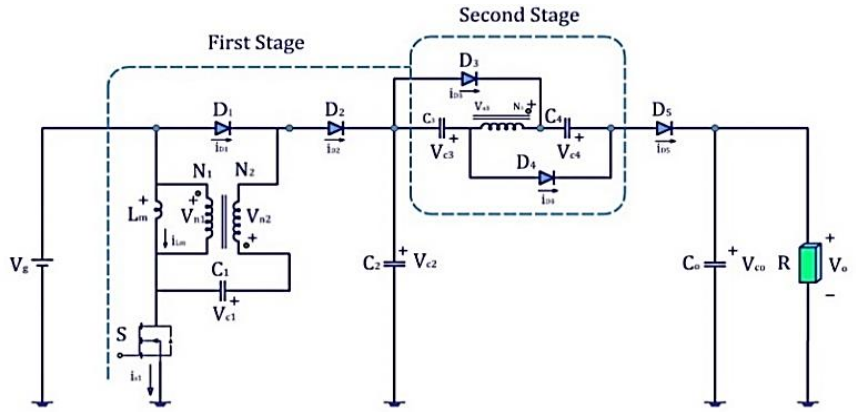

Figure 1. Schematic diagram of the DC-DC ultra-lift converter circuit [37]

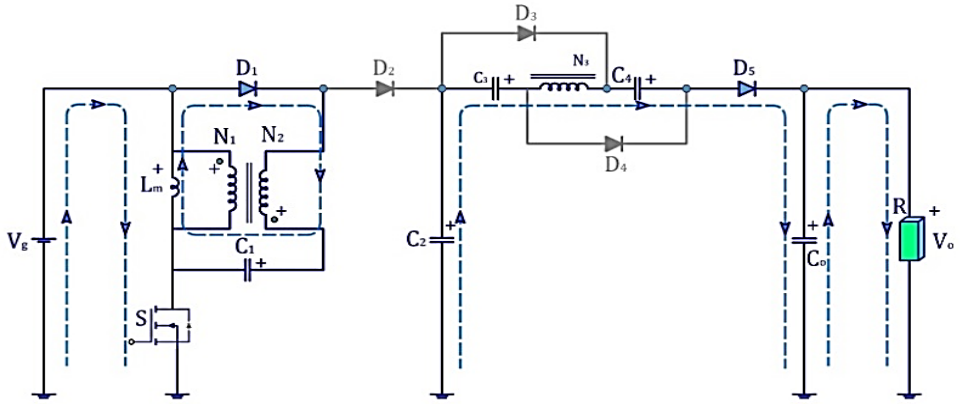

Figure 2. Converter current path in mode 1 DCM [38]

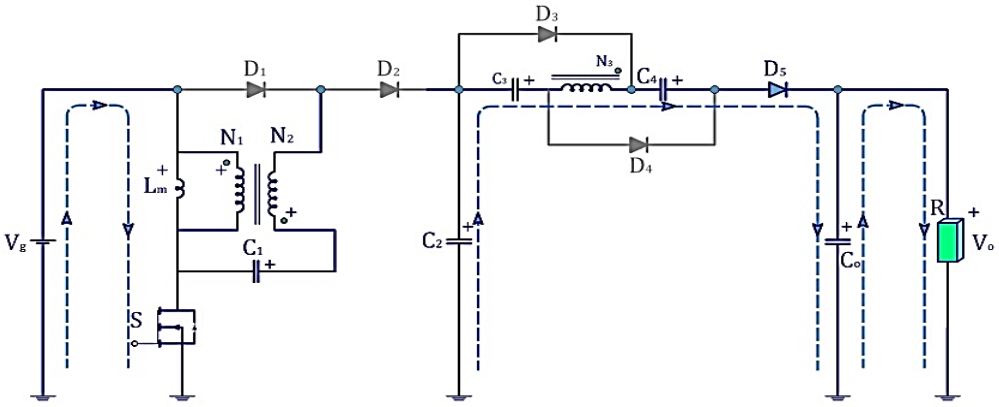

Figure 3. Converter current path in mode 2 DCM [39]

2.2. Switch off

2.2.1. Mode 3 [t2-t3]

At the start of [*t2-t3*] interval, the switch S turns off. Diodes 2, 3, and 4 are in direct bias and are on. Capacitor C_2 is charged by demagnetizing the magnetic inductor and discharging capacitor C_1. Capacitors C_3 and C_4 are being charged via *diodes 3* and *4* as well as tertiary of couple inductance. The current path during this mode of operation is given in Figure 4.

2.2.2. Mode 4 [t3-t4]

In this case, the switch *S* is still off. Capacitors C_3 and C_4 are charging as before, and diodes D1, D2, and D5 are all in reverse bias and are disconnected. At the end of this operation, the amount of magnetizing inductor current reaches zero. The current path in this model is presented in Figure 5.

2.2.3. Mode 5 [t4-t5]

At the time interval [*t4-t5*], switch *S* is still off. Diodes 1, 2, 3, 4, and 5 are disconnected in reverse bias. During this operation, the amount of magnetizing inductor current is still zero. The current path in this model is demonstrated in Figure 6. The process of switching described earlier is repeated at the end of this process. Figure 7 shows the waveform of the circuit elements in different modes from t_0 to t_5.

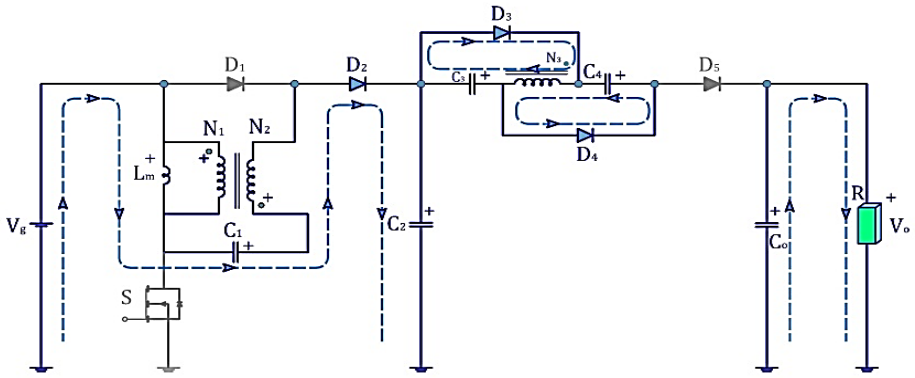

Figure 4. Converter current path in mode 3 DCM

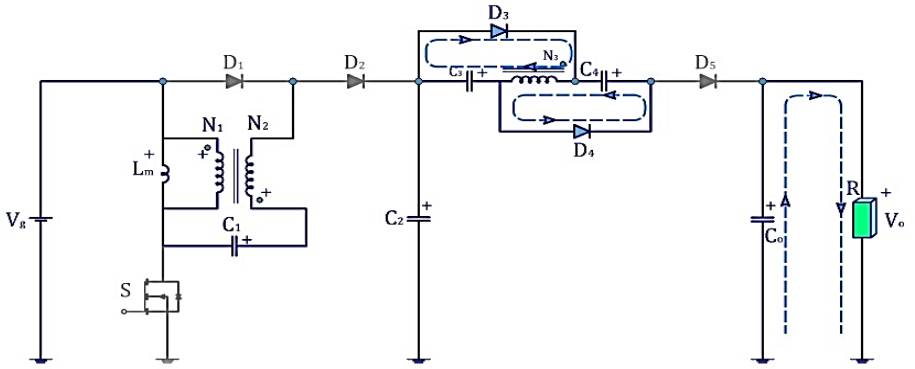

Figure 5. Converter current path in mode 4 DCM

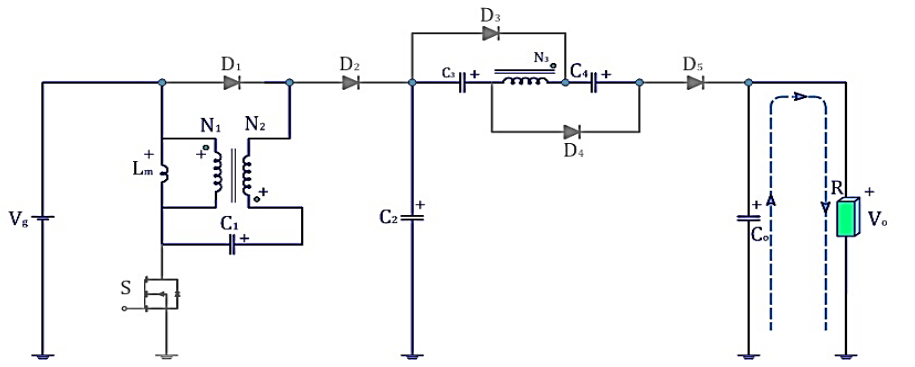

Figure 6. Converter current path in mode 4 DCM

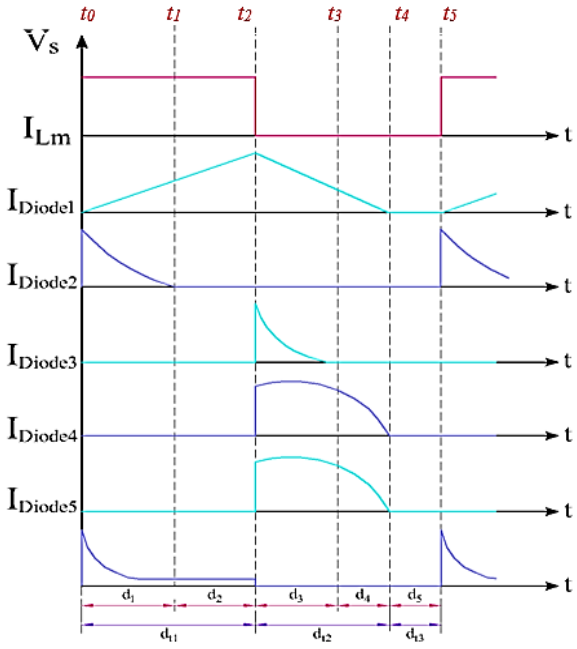

Figure 7. Waveform's current of switches, magnetic inductors, and diodes in DCM

3. STEADY-STATE ANALYSIS DURING DCM

According to Figure 2 and Figure, 3, the voltage across the primary winding of the coupled inductor and the magnetic inductor is equal to:

$$V_{N1}{}^{dt1} = V_{in} \tag{1}$$

In addition, the secondary and tertiary voltages across the coupling transformer (V_{N3}-V_{N2}) in modes 1 and 2 are equal to:

$$V_{N2}{}^{dt1} = N_{21}V_{in} \tag{2}$$

$$V_{N2}{}^{dt1} = N_{21}V_{in} \tag{3}$$

where N_{21} and N_{31} are the secondary and tertiary turn ratios of the coupled inductor, respectively, using the principal Volt-Second balance for the primary winding of the inductor, the average primary voltage of the transformer in modes 3 and 4 is equal to:

$$\langle V_{N1}\rangle_{Ts} = d_1T_sV_{N1}{}^{d1} + d_2T_sV_{N1}{}^{d2} + d_3T_sV_{N1}{}^{d3} + d_4T_sV_{N1}{}^{d4} + d_5T_sV_{N1}{}^{d5} = 0 \tag{4}$$

by placing (1) in (4) and knowing $V_{N1}{}^{d5} = 0$:

$$(d_1 + d_2)T_sV_{in} + (d_3 + d_4)T_sV_{N1}{}^{dt2} = 0 \tag{5}$$

by simplifying the (5) and considering $(d_1 + d_2) = d_{t1}$ and $d_3 = d_{t2}$ and $d_4 = d_{t3}$:

$$V_{N1}{}^{dt2} = \frac{-d_{t1}}{d_{t2}}V_{in} \tag{6}$$

where in:

$$(1 - d_{t1} - d_{t2} - d_{t3}) = 0 \tag{7}$$

The voltage across capacitors is assumed to be almost constant. Therefore, the voltage across the capacitors is approximately equal to its voltage in one mode. According to Figure 2, the voltage across capacitor C_1 can be determined as follows:

$$V_{c1} \approx {V_{c1}}^{d_{t1}} = (1 + N_{21}){V_{N1}}^{d_{t1}} = (1 + N_{21})V_{in} \quad (8)$$

according to Figure 2, the voltage across capacitor C_2 is:

$$V_{c2} \approx {V_{c2}}^{d_{t2}} = V_{in} - {V_{N1}}^{d_{t2}} + V_{c1} - N_{21}{V_{N1}}^{d_{t2}} \quad (9)$$

by placing the relevant equations and simplifying relation (9), V_{c2} would be given as in (10):

$$V_{c2} = V_{in} \times \frac{2d_{t2}+N_{21}d_{t2}+d_{t1}(1+N_{21})}{d_{t2}} \quad (10)$$

the voltage across capacitors C_3 and C_4 are equal and can be calculated using (11):

$$V_{c3} = V_{c4} \approx {V_{c3}}^{d_{t2}} = N_{31} \times V_{in} \times \frac{d_{t1}}{d_{t2}} \quad (11)$$

using KVL, the output voltage according to Figure 2 is equal to:

$$V_o \approx {V_o}^{d_{t1}} = V_{c2} + V_{c3} + V_{c3} + V_{c4} \quad (12)$$

finally, based on the Equations provided above, the converter gains in a DCM are equal to:

$$M_{DCM} = \frac{V_o}{V_{in}} = \frac{d_{t2}(2+N_{21}+N_{31})+d_{t1}(1+N_{21}+2N_{31})}{d_{t2}} \quad (13)$$

In (13), d_{t2} is unknown. To get its value for diode D5 in the first interval, we have:

$$i_{Diode5(t)} = i_c(t) + \frac{V(t)}{R} \quad (14)$$

using the principle of ampere-second balance, the capacitor's current at a steady state is zero. According to this principle, the current equation of the diode can be described as follows:

$$\langle i_{Diode5} \rangle_{T_s} = \frac{V(t)}{R} \quad (15)$$

the inductor current starts at zero, and at the end of time, d_{t1} T_s reaches i_{pk}. The value of i_{pk} is equal to:

$$i_{pk} = \frac{d_{t1}V_g T_s}{L_m} \quad (16)$$

in the second interval, the inductor current reaches zero and continues until the end of the third time interval. In this case, we will have:

$$\langle i_{Diode5} \rangle_{T_s} = \frac{1}{T_s}\int_0^{T_s} i_D(t)d(t) = \frac{1}{2} i_{pk} \frac{d_{t2}T_s}{(1+N_{21})} \quad (17)$$

by placing (16) in (17), we have:

$$\frac{V}{R} = \frac{d_{t1}V_g d_{t2}T_s}{4L_m(1+N_{21})} \quad (18)$$

wherein:

$$\frac{4L_m(1+N_{21})}{RT_s} = K \quad (19)$$

by placing (19) in (18) for the duration $d_{t2,}$ we have:

$$K\frac{V}{V_g d_{t1}} = d_{t2} \quad (20)$$

the voltage stress on the switch at times d_{t2} and d_{t3} are given by (21) and (22), respectively:

$$V_s{}^{d_{t2}} = V_{in} - V_{N1}{}^{d_{t2}} \quad (21)$$

$$V_s{}^{d_{t3}} = V_{in} \quad (22)$$

the voltage across *diode 1* at times d_{t2} and d_{t3} is:

$$V_{Diode1}{}^{d_{t2}} = V_{N1}{}^{d_{t2}} - V_{c1} + N_{21}V_{N1}{}^{d_{t2}} \quad (23)$$

$$V_{Diode1}{}^{d_{t3}} = -V_{c1} \quad (24)$$

the voltage across *diodes 2*, *3*, and *4*, at times d_{t1}, and d_{t3}, can be equal to:

$$V_{D2}{}^{d_{t1}} = V_{in} - V_{c2} \quad (25)$$

$$V_{D2}{}^{d_{t3}} = V_{in} + V_{c1} - V_{c2} \quad (26)$$

$$V_{D3}{}^{d_{t1}} = V_{D4}{}^{d_{t1}} = V_{c3} + N_{31}V_{N1}{}^{d_{t1}} \quad (27)$$

$$V_{D3}{}^{d_{t3}} = V_{D4}{}^{d_{t3}} = -V_{c3} \quad (28)$$

the voltage across the output diode can also be calculated using (29) and (30):

$$V_{D5}{}^{d_{t2}} = V_{c2} + V_{c3} + N_{31}V_{N1}{}^{d_{t2}} + V_{c4} - V_o \quad (29)$$

$$V_{D5}{}^{d_{t3}} = V_{c2} + V_{c3} + V_{c4} - V_o \quad (30)$$

4. SELECTING CIRCUIT ELEMENTS

4.1. Selecting passive elements

It is better to eliminate RHP zero to achieve the desired control [36]. As shown in Figure 8, the transfer of the poles along the imaginary axis causes a change in the natural damping frequency: low overshoot, too much overshoot and steady state as shown in Figures 8(a)-8(c), respectively. This is the case if the change in the value of capacitors C_1, C_2, C_3, and C_4 does not cause a shift to the right zero position of the system. In general, a change in the values of the circuit elements does not cause the system's RHP zero to be lost. Therefore, the change in the circuit elements is only done to improve the system's response and overshoot.

To select the values of passive elements properly, several things should be considered, and these are: i) The damping factor and quality factor must be adequate, ii) The number of passive elements should be as small as possible to minimize costs, and iii) The closed-loop system has an acceptable margin phase. In addition, the ripple value is also desired value. For this purpose, the amount of magnetizing inductor is increased. An increase in the amount of magnetic inductor slows down the system response. However, reducing the amount of output capacitor accelerates the system response and, on the other hand, causes minor uplift [35].

By compromising between technical and economic issues and considering the converter's small size, the magnetizing inductor and output capacitor values are set to $L = 10\ \mu H$, $C_o = 20\ \mu F$. Furthermore, because the use of capacitors with high capacity increases the cost, the value of capacitors C_1 through C_4 is considered equal to $48\ \mu F$. The effect of adjusting the amount of output capacitor and magnetic inductor on the output voltage is presented in Figure 9.

4.2. Selecting load

Selecting the amount of load resistance helps designers evaluate the system's characteristics. In general, a change in the amount of load resistance does not affect the constant value of the output voltage. In contrast, a change in load resistance causes a change in the amount of inductor current and the quality factor. The effect of changing the amount of load on the output voltage is demonstrated in Figure 10. The load resistance value of 500 ohms is considered to make sure that the converter operates in DCM mode.

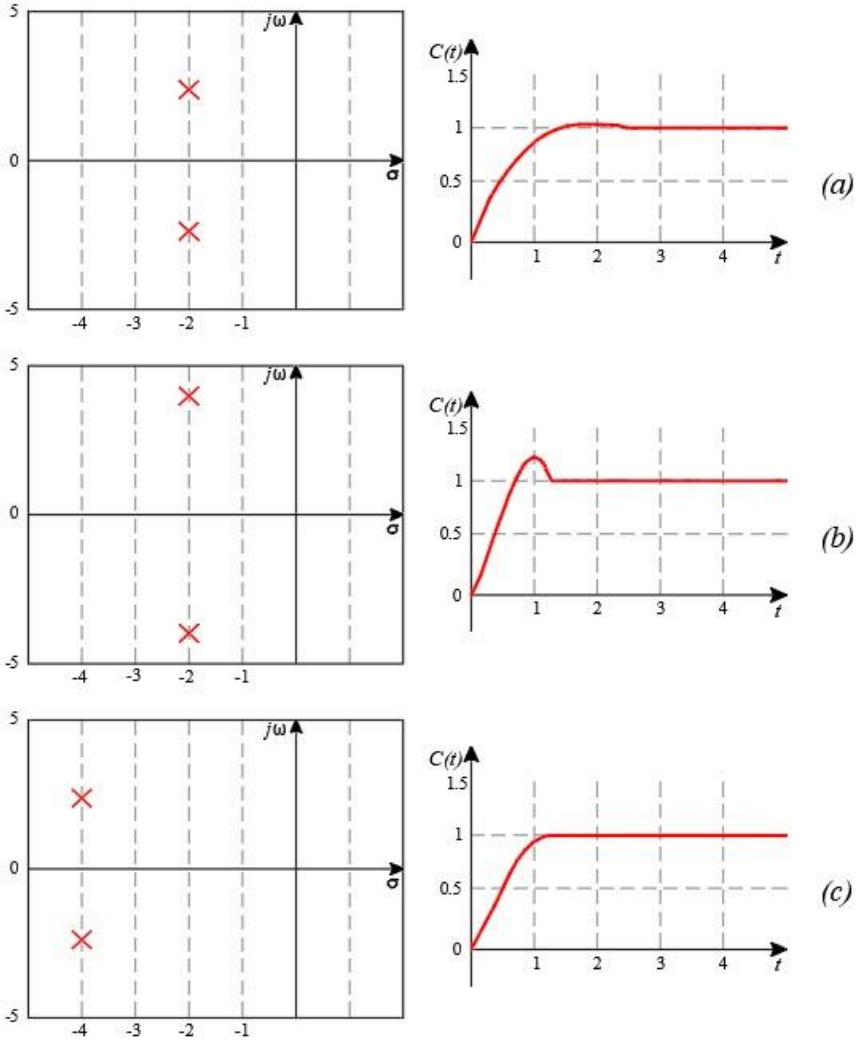

Figure 8. The effect of pole displacement on the transient response of the system, (a) low overshoot, (b) too much overshoot, and (c) steady state

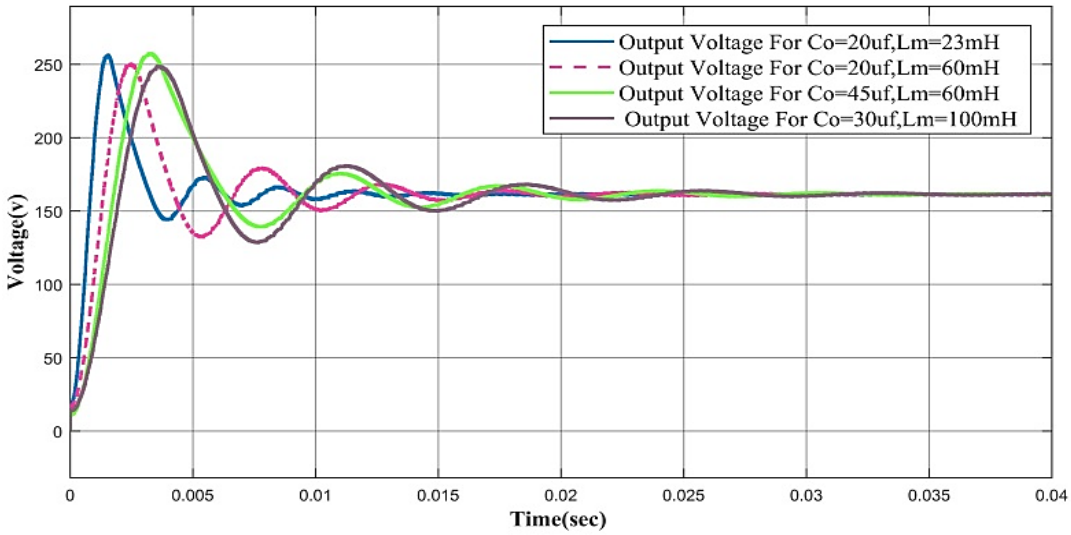

Figure 9. The effect of changing the amount of output capacitor and magnetic inductor on the output voltage

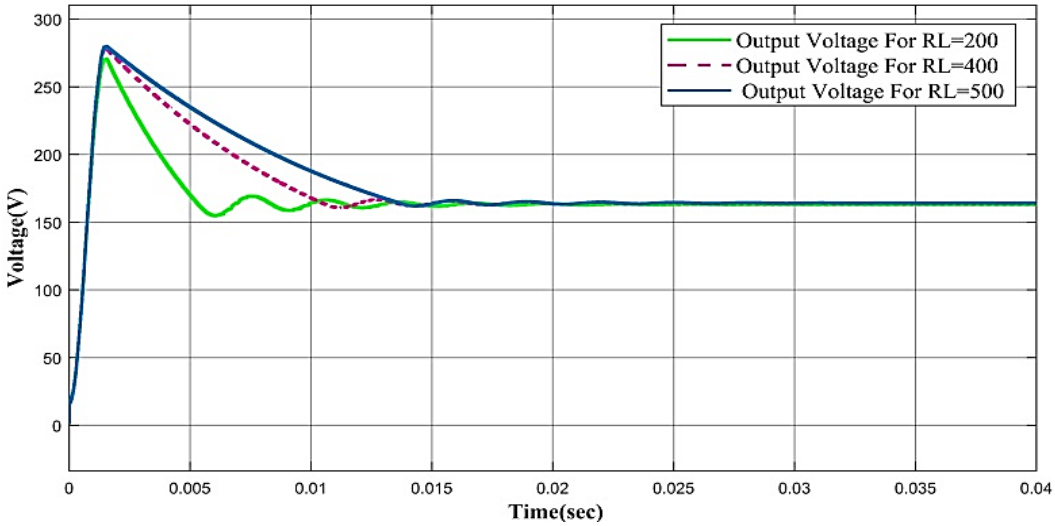

Figure 10. The effect of load resistance changes the output voltage

5. SIMULATION RESULTS

Simulation results are used to validate the relationships and equations presented in this paper. Table 1 shows the values used to simulate the proposed converter. The converter has an output power of 66.6 watts and an output voltage of 186 volts per input voltage of 10 volts. The simulation results confirm with an acceptable approximation the relationships and equations presented in section 3. The voltage across capacitors 1, 2, and 3 are shown in Figures 11(a)-(c) (see Appendix). According to relations (8), (10), and (11), the simulation results are confirmed. Figure 11(d) (see Appendix) shows the output voltage of the converter which is equal to their expected value from (13). From the values and results obtained from the simulation, it can be concluded that the voltage drop across the MOSFET is about 5 volts, which indicates the low $R_{DS\text{-}ON}$ choice for the MOSFET, given the amount of output voltage. Figure 11(e) (see Appendix) also shows the waveform of the magnetizing inductor current in a discontinuous conduction mode.

Table 1. Parameters of the converter employed in the modeling

Parameter		Value
Input voltage	V_g	10 V
Output voltage	V_o	186 V
Rated output power	P_{out}	66.6 W
Switching frequency	F_s	40 kHz
Load	R	500 Ω
Duty cycle	D	0.6
Coupled inductor turns ratio	N_{21} -N_{31}	1:2
Magnetizing inductor	L_m	10μH
Capacitor	C_1, C_2, C_3, C_4	48μH
Capacitor	C_o	20μH

6. CONCLUSION

The DCM of an ultra-lift converter considering a three-winding inductor and voltage multiplier circuit was investigated in this paper. The operating modes of the converter in DCM operation were thoroughly described. After that, the relations and equations that regulate the converter in this `working regime were presented. One of the advantages of the proposed converter is the use of a three-winding inductor in the converter structure, which can achieve the highest values of the output voltage without increasing the duty cycle. As observed, in this converter, using the value of low duty cycle $D = 0.6$ enabled achieving the output voltage value of 18.6 times the input voltage. In addition, the discontinuous operating regime of the converter was analysed in steady-state, which ensures easier control of the converter and also achieves the highest values of the output voltage without changing the input voltage, output cycle, and circuit elements.

APPENDIX

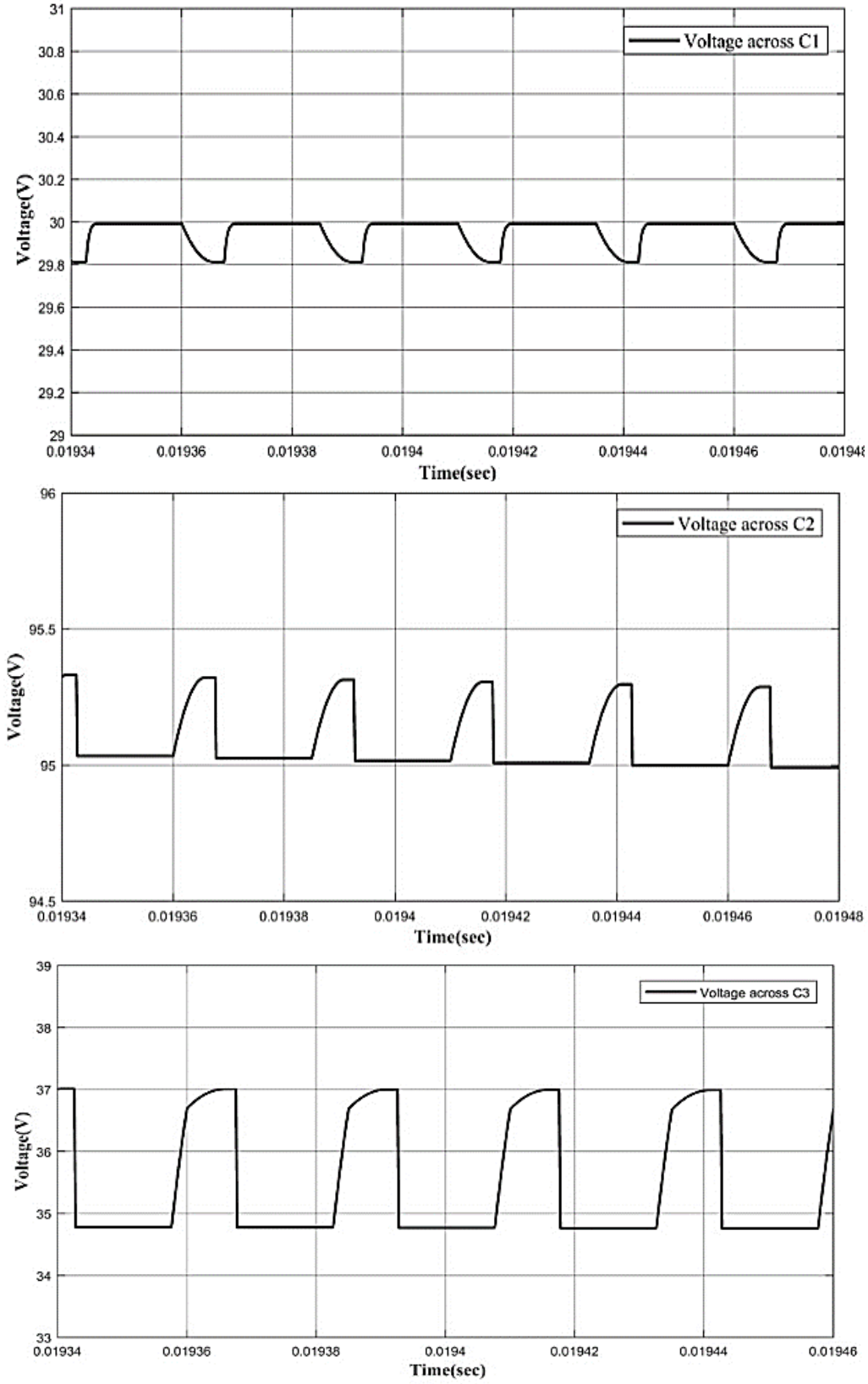

Figure 11. Simulation results: (a) C1 voltage, (b) C2 voltage, and (c) C3 voltage

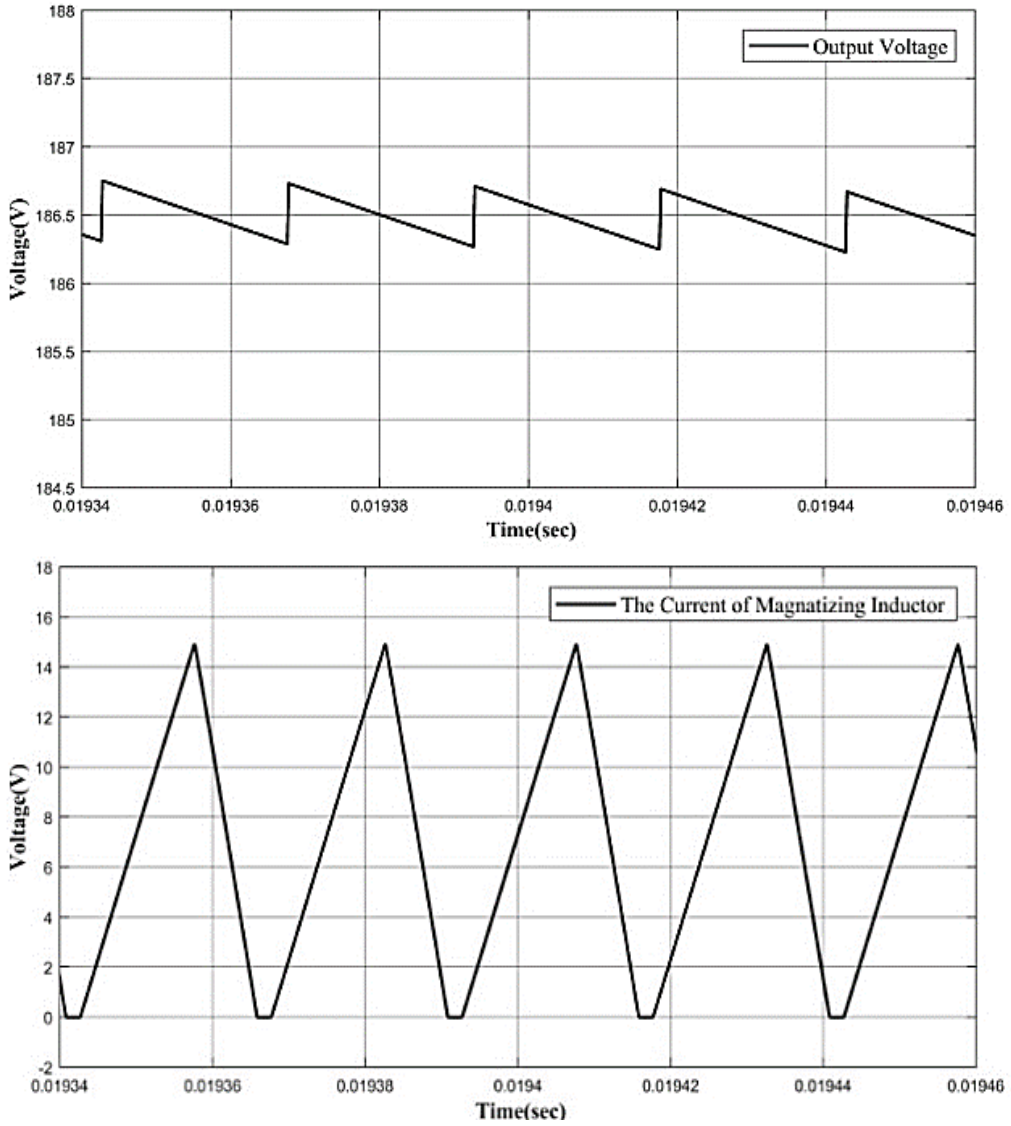

Figure 1. Simulation results: (d) output voltage and (e) magnetizing current (continue)

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BIOGRAPHIES OF AUTHORS

Saeed Hasanzadeh received the M.Sc. and Ph.D. degrees in electrical engineering from the University of Tehran (UT), Tehran, Iran, in 2006 and 2012, respectively. His M.Sc. thesis and Ph.D. dissertation have been conducted in the field of high voltage engineering and wireless power transfer (WPT), respectively. In 2013, he joined the Department of Electrical and Computer Engineering, Qom University of Technology, as an Assistant Professor. He is currently the Dean of the Department of Electrical and Computer Engineering (ECE), Qom University of Technology. His current research interests include power electronics, electrical machines, wireless power transfer, and high voltage engineering. He was a recipient of the Top Research Prize of Qom University of Technology, in 2019. He was also recognized as an Outstanding Lecturer with the Qom University of Technology, in 2020. He is a TPC Member of the IEEE Power Electronics & Drives: Systems and Technologies Conference (PEDSTC). He is an Editorial Board of the Power Electronics Society of Iran (PELSI). He can be contacted at email: hasanzadeh@qut.ac.ir.

Milad Asadi received the B.Sc. degree from Arak University, Arak, Iran, and the M.Sc. degree from Qom University of Technology, Qom, in 2012 and 2019, respectively, both in electrical engineering. His research interests include design, modeling, and control of power electronics converters and their applications electrical traction systems. He can be contacted at email: Milad021021.Asadi@yahoo.com.

Tole Sutikno is a lecturer in Electrical Engineering Department at the Universitas Ahmad Dahlan (UAD), Yogyakarta, Indonesia. He received his B.Eng., M.Eng. and Ph.D. degrees in Electrical Engineering from Universitas Diponegoro, Universitas Gadjah Mada and Universiti Teknologi Malaysia, in 1999, 2004 and 2016, respectively. He has been an Associate Professor in UAD, Yogyakarta, Indonesia since 2008. He is currently an Editor-in-Chief of the TELKOMNIKA and the Head of the Embedded Systems and Power Electronics Research Group (ESPERG). He is among the top 2% of researchers named by Stanford University and Elsevier BV as the most influential scientists in the world for 2021–present. His research interests include the field of digital design, industrial applications, industrial electronics, industrial informatics, power electronics, motor drives, renewable energy, FPGA applications, embedded system, artificial intelligence, intelligent control, information technology and digital library. He can be contacted at email: tole@te.uad.ac.id, tole@ee.uad.ac.id.