

Design and analysis of a high-gain dual-input single-output DC-DC converter for hybrid energy systems applications

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ABSTRACT

The high gain converters are one among the proven topologies that are found attractive for industrial and commercial applications. They deal with high power ratings like automobile headlamps, energy backup systems, and fuel cell electric vehicles (FCEV). In literature, most of the topologies were used a single duty ratio. This may not be reliable for high-duty cycle operation because to improve the voltage gain, the components will be increases. This paper proposes the time-sharing concept based on the non-isolated high step-up dc-dc converter. With the parallel-charged and series-discharged inductors, the proposed converter can produce high output voltage gains. The effectiveness of the proposed circuit configuration is verified in MATLAB/Simulink and the results are corroborated by theoretical analysis.

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1. INTRODUCTION

With the growth in the utilization of alternative energy resources in power generation systems like solar, wind turbines, and fuel cells, the DC-DC converters must be employed to modify the power given as usable power for power use from renewable sources [1]–[3]. Taking into account the role of alternative sources is delicate to environmental factors, it's important to create a power source that is both renewable and controlled output voltage [4].

The multi-input converters' (MIC) topologies have been the subject of numerous articles recently to solve the aforementioned issues. Hou *et al.* [5] proposed two architectures that offer high gain and lower blocking voltages on semiconductor components than standard boost converters and are dependent on the series/parallel arrangement of switched-diode-capacitor cells. Unfortunately, the capacitors and inductors number used in this converter is inversely proportional to the input sources number. Therefore, the growing size and price of converters should be taken into account. In [6], [7], a high-efficiency, low-voltage stress, two-input buck converter with one switch is proposed. The major disadvantage of this converter is its narrow output voltage range, which ranges between two input voltage levels. Authors of [8]–[10], introduce yet another non-isolated multi-input single-output (MISO) converter. In these converters, the output voltage gain is affected by the quantity of input sources. In fact, the output voltage can be increased by increasing the number of input cells.

A single stage multiport converter is suggested in [11] for auxiliary power supply in EV application. It has bidirectional functionality for battery charging. However, it has low voltage gain and independent control of output voltage may be difficult. Athikkal *et al.* [12] presented the bridge type MISO converter for energy

sources integration. It is the improved MISO configuration structure and it improves the voltage output. However, the MISO operation of the converter may not be performed if the the voltage source V_2 is higher than the voltage source V_1 . Azmoon-asmarood *et al.* [13] designed a multi-input multi-output (MIMO) converter topology developed with high voltage gain for the application of renewable energy. However, the performance of the converter may get affected due to its greater number of passive elements and diodes. Zaid *et al.* [14] introduced a non-isolated MISO converter with voltage multiplier cell. Never less, it has more diodes and passive elements it may affect the converter size and efficiency of the system. In [15], dual-input dual-output converter is introduced for EV charger. It has single inductor and low power devices which results in an enhanced system power density. However, inductor is switched between the outputs due to this converter may suffer with cross regulation problems.

MIMO topologies have recently drawn increasing attraction due to their ability to obtain multiple output voltage levels, maximize power point tracking (MPPT), and share power among many input sources simultaneously. For use in micro-grid applications, the high step up converters are useful which comprise of diode and capacitors in the voltage multiplier, in [16] it has been described. When one or more of the input sources are experiencing a failure, the converter can still function. In actuality, the converter's volume and price are increased by its large number of components. A modular multiport converter is suggested in [17] that feature bidirectional operation, but the arrangement cannot work simultaneously in the buck or boost mode and step-up mode because they differ from each other. The interleaved boost converter suggested in [18] has lessened input current ripple. But in this structure, one input source should be more valuable than the other. In [9], [19] two dual-input dual-output converters for EV applications were presented. Semiconductor components are under low voltage stress in the converter [19]. However, there are many inductors, and the control scheme is complicated. Single-inductor MIMO (SI-MIMO) topology has drawn increasing attention recently because of its high-power density, low cost, and straightforward control strategy. A straightforward method based on typical conventional converters has been provided in [9] to derive various SI-MIMO topologies. MISO converters are presented in the literature with the reduced part which are of low cost and have high power density. However, it has low voltage gain. This problem is overcome in [20]–[24] with improved voltage gain for grid-connected EV and hybrid energy system applications.

The rest of the paper is organized as follows: i) Section 2 describes the proposed topology and its functioning; ii) Small-signal modeling of the proposed modeling is dealt in section 3; iii) In section 4, design considerations of parameter, stress analysis, power loss calculations, and comparative assessment are presented; iv) Results and discussions are described in section 5 and section 6 presents a conclusion.

2. PROPOSED CONFIGURATION OPERATING PRINCIPLE AND MODES OF OPERATION

The proposed multi-input high gain configuration is shown Figure 1. It has five power IGBTs (S_1 – S_5), five diodes (D_1 – D_5), inductors (L_1 , L_2), and capacitors (C , C_1). In this topology, the gain is improved through energy-stored elements which are charged in parallel by the input source during the turn-on time, and the energy is discharged to the load in series during the OFF time. In the proposed structure, switches are operated based on a time-sharing scheme which in turn gives high step-up voltage and also improves the utilization of energy sources.

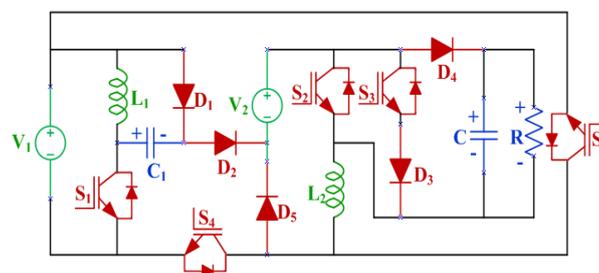


Figure 1. Schematic of proposed configuration

The proposed structure is suitable for solar battery chargers, and fuel cell electric vehicles. It has the following advantages: i) Simple structure and fewer components lead to low cost and compact size; ii) High voltage gain; iii) It can execute multi-input boost, buck, buck-boost operations; iv) Improves the utilization of energy sources with two distinct duty ratios. Modes of operation:

- i) Mode 1: The L_1 , L_2 are energized and C_1 is charged by input source through the switches S_1 , S_2 , and D_1 respectively. And C has discharged its stored energy to the load. Figure 2(a) illustrates the circuit for mode 1. The corresponding equations are as below:

$$V_{L_1} = L_1 \frac{di_{L_1}}{dt} = V_1 \tag{1}$$

$$V_{L_2} = L_2 \frac{di_{L_2}}{dt} = V_2 \tag{2}$$

$$V_{C_1} = V_1 \tag{3}$$

ii) Mode 2: In mode-2 operation, S1 and S2 are turned OFF while S3 is ON and D1 and D3 are reverse biased which is depicted in Figure 2(b). The inductors are in series through the switch S3 and the corresponding inductor voltage is as (4).

$$V_{L_1} = V_{L_2} = \frac{V_1+V_2+V_{C_1}}{2L} \tag{4}$$

iii) Mode 3: In mode-3 operation, the dc input source, L1, L2 and C1 are in series with the load. The energy stored in previous modes is supplied to load through D3 as shown in Figure 2(c) and the inductor voltage in this mode as (5).

$$V_{L_1} = V_{L_2} = \frac{V_1+V_2+V_{C_1}-V_0}{2L} \tag{5}$$

The output voltage equation in terms of duty ratio is in (6),

$$V_0 = \frac{2V_1+V_2(1+d_1)}{(1-d_1-d_2)} \tag{6}$$

where ‘d₁’ and ‘d₂’ are the duty ratio of the corresponding switches.

Figures 3(a)-3(c) and Figures 4(a)-4(b) depicts the equivalent circuits for the proposed structure in buck-boost and buck operation respectively. The voltage gain of the proposed configuration is theoretically tested using (6) by varying duty ratio d₁ against different values for duty ratio d₂. The corresponding plot is represented in Figure 5(a). The voltage gain of the configuration is verified at a different set of duty cycles. In this case, the maximum operating duty ratio is considered as d₁+d₂ = 0.9. In Figure 5(a), duty ratio d₂ is kept constant and d₁ varied, the output voltage is observed to be increased with the increment of d₁. It is also tested at constant d₁ and d₂ varied at a different set of duty ratios and is presented Figure 5(b). From Figure 5(b), the output voltage is decreased if d₂ is increased and is validated with output voltage expression i.e. (6).

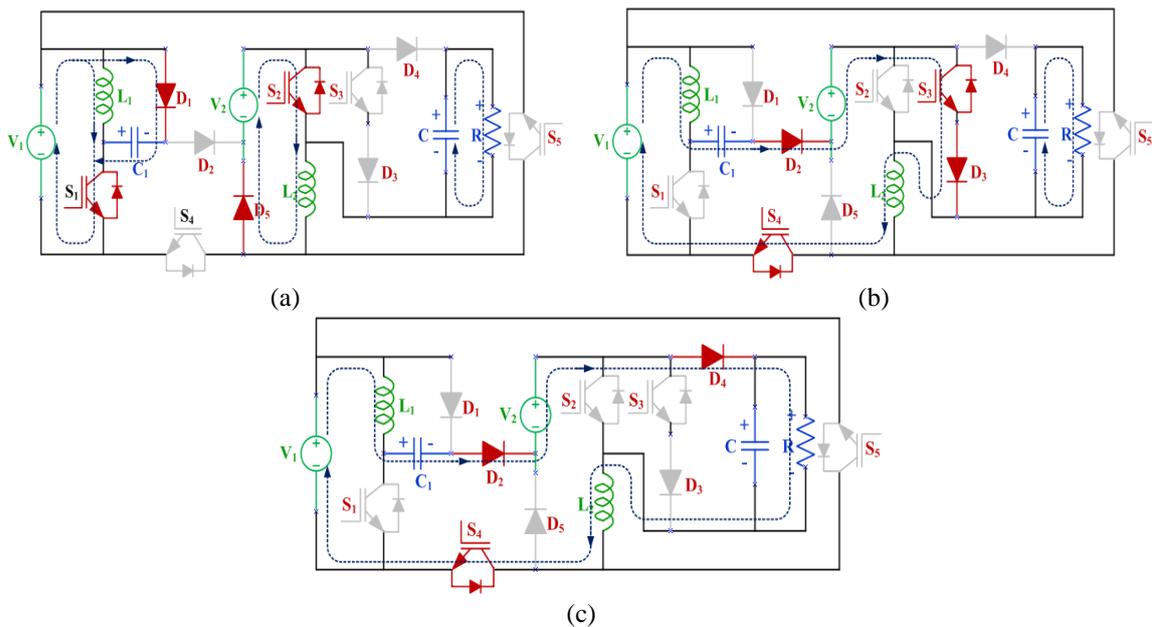


Figure 2. Circuit model in boost operation: (a) state-1, (b) state-2, and (c) state-3

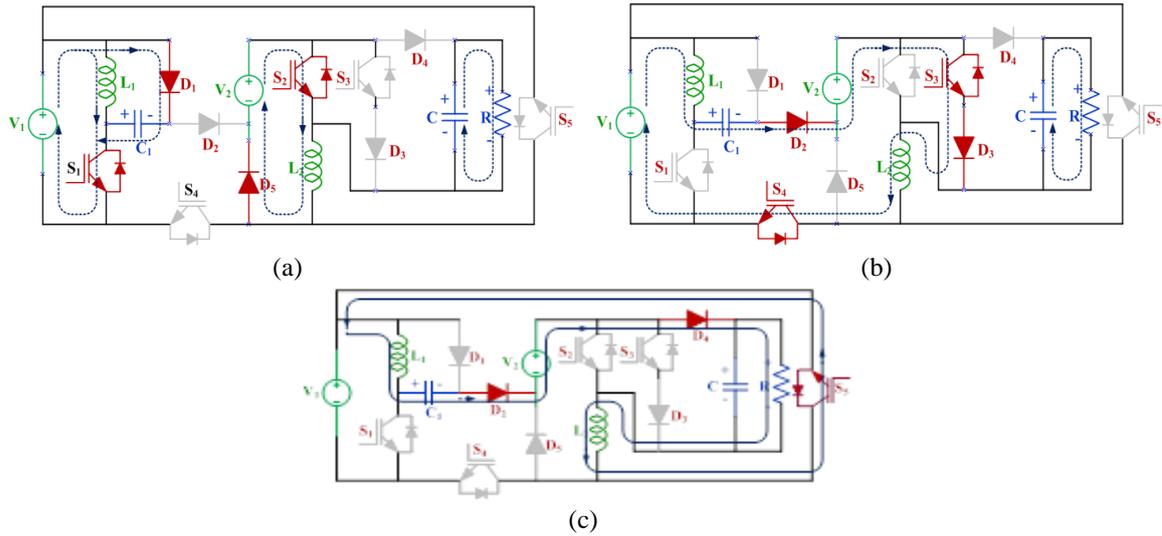


Figure 3. Circuit model in buck-boost operation (a) mode-1, (b) mode-2, and (c) mode-3

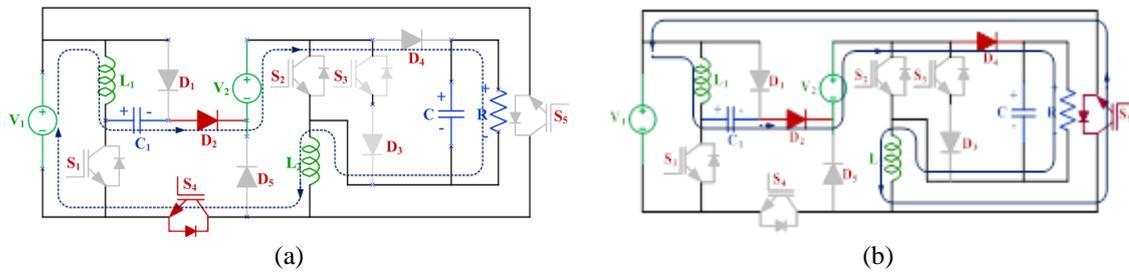


Figure 4. Current paths in buck mode (a) state-1 and (b) state-2

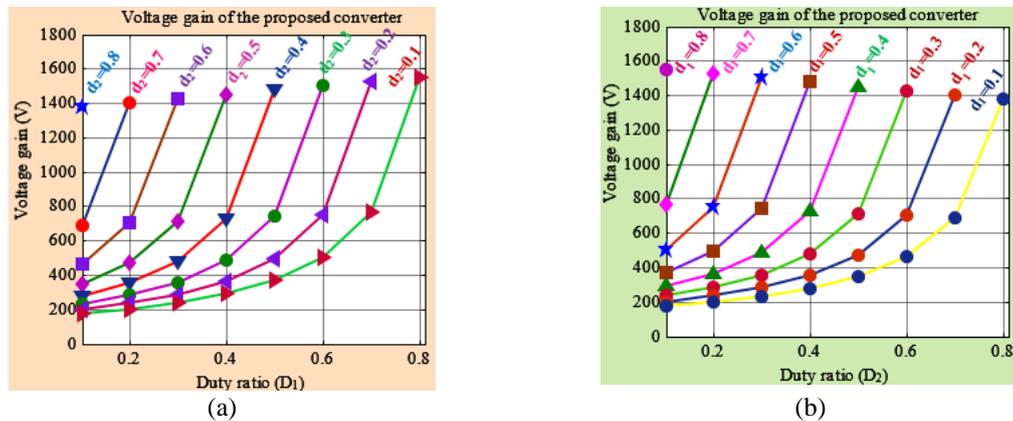


Figure 5. Duty ratios effect on voltage gain (a) voltage gain vs d_1 for different values of d_2 and (b) voltage gain vs d_2 for different values of d_1

3. SMALL-SIGNAL MODELING

In [25] presents the details of small- signal modeling of the converter. Generally, the two parts of the state variables are a DC value (\bar{x}, \bar{d}) and a perturbation (\tilde{x}, \tilde{d}). The state-space equations and transfer function are as follows in (7)-(15).

$$\begin{aligned}
 x &= \bar{x} + \tilde{x} \\
 d &= \bar{d} + \tilde{d}
 \end{aligned}
 \tag{7}$$

In (8), the small-signal models' matrix form is given.

$$\begin{aligned} \dot{\tilde{x}} &= A\tilde{x} + B\tilde{u} \\ \tilde{y} &= C\tilde{x} + D\tilde{u} \end{aligned} \tag{8}$$

The average model of the proposed converter is in the form as follows, where \tilde{x} , \tilde{u} , and \tilde{y} are control variables vector, state variable vector, and system output vector respectively.

$$A = \begin{bmatrix} 0 & 0 & 0 & \frac{-(1-d_1-d_2)}{L_1} \\ 0 & 0 & 0 & \frac{-(1-d_1-d_2)}{L_2} \\ \frac{1}{C_1} & 0 & 0 & 0 \\ \frac{(1-d_1-d_2)}{C_0} & 0 & 0 & \frac{-(1-d_1-d_2)}{RC_0} \end{bmatrix} \tag{9}$$

$$B = \begin{bmatrix} \frac{2}{L_1} \\ \frac{2}{L_2} \\ 1 \\ 0 \end{bmatrix}, C = [0 \quad 0 \quad 1 \quad 1], D = 0 \tag{10}$$

$$\tilde{x} = \begin{bmatrix} i_{L_1} \\ i_{L_2} \\ V_{C_1} \\ V_0 \end{bmatrix}, \tilde{u} = [\tilde{d}] \tag{11}$$

The control transfer function is as (12)-(14).

$$\frac{\tilde{V}_0}{\tilde{d}} = C[SI - A]^{-1}f \tag{12}$$

$$f = AX + BV_{in} \tag{13}$$

$$X = A^{-1}bV_{in} \tag{14}$$

The frequency response is depicted in Figure 6. From the bode plot, it is found that phase margin is 155°, and the gain margin is infinite dB.

$$\frac{\tilde{V}_0(s)}{\tilde{d}(s)} = \frac{s^3(RC_0(L_1+L_2)) - s^2(-2(L_1+L_2) - 8RC_0) - RC_0(D_1^2 + D_2^2) - 2(L_1+L_2)C_0 + 4RC_0(D_1+D_2)}{s^4(2RC_0(L_1+L_2)) + s^3(2C_0(L_1+L_2)(1-D_1-D_2)) - s^2RC_0((1-D_1^2 - D_2^2) + 2(D_1+D_2-D_1D_2)) + RC_0(L_1+L_2)(1-D_1-D_2)} \tag{15}$$

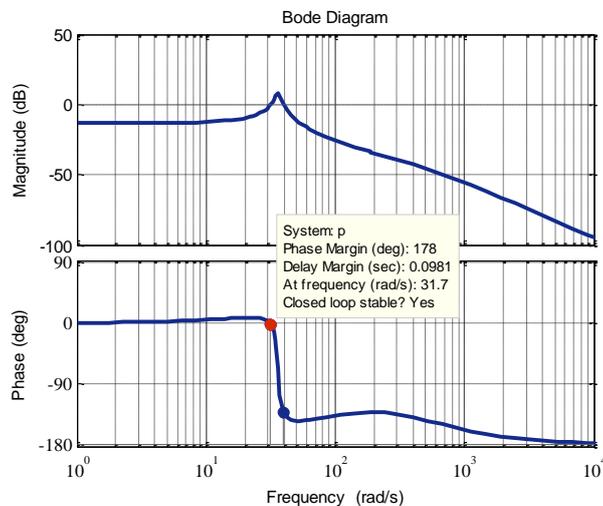


Figure 6. Bode plot

4. PERFORMANCE ANALYSIS

4.1. Effect of parasitic

The converter with parasitic resistances is shown Figure 7. Where R_{DS} is the on-state resistance, r_{D1} , r_{D2} , and r_{D3} are the forward resistance of the diodes D_{1-3} respectively. For the inductor L_1 - L_2 , the equivalent series resistance (ESR) is r_{L1-2} .

- i) Mode 1: In mode-1 with the time duration of $d1T_s$, the devices $S1$ and $S2$ are ON and $S3$ are OFF, the equations for average capacitor current I_{C0} and the inductor voltage V_{L1} are given in (16)-(18).

$$V_{L1} = V_1 - i_{L1}(r_{S1} + r_{L1}) \tag{16}$$

$$V_{L2} = V_2 - i_{L2}(r_{S2} + r_{L2} + r_{D5}) \tag{17}$$

$$i_{C0} = \frac{-V_0}{R_0} \tag{18}$$

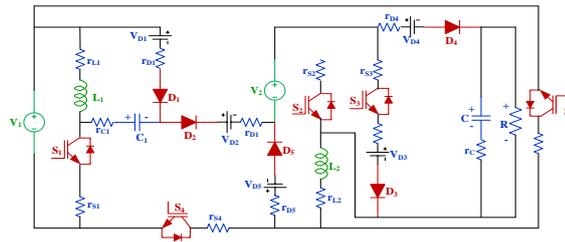


Figure 7. Proposed converter with parasitic

- ii) Mode 2: In mode-2 with time interval $d2T_s$, the devices $S1$ and $S2$ are OFF and $S3$ is ON. Then the average capacitor current I_{C0} and the inductor voltage V_{L1} are given in (19) and (20).

$$V_{L1} = \frac{V_1 + V_2 + V_{C1} - i_{L1}(r_{S3} + r_{L1} + r_{L2} + r_{D2} + r_{D3} + r_{S4}) - V_{D2} - V_{D3}}{2} \tag{19}$$

$$i_{C0} = \frac{-V_0}{R_0} \tag{20}$$

- iii) Mode 3: In mode-3 operation with time interval $(1-d1-d2)T_s$, the devices $S1$, $S2$, and $S3$ are kept OFF, and the average capacitor current I_{C0} , and the inductor voltage V_{L1} are given in (21) and (22).

$$V_{L1} = \frac{V_1 + V_2 + V_{C1} - i_{L1}(r_{S4} + r_{L1} + r_{L2} + r_{D2} + r_{D4}) - V_{D2} - V_{D4}}{2} \tag{21}$$

$$i_{C0} = i_{L1} - \frac{V_0}{R_0} \tag{22}$$

Were,

$$i_{L1} = \frac{V_0}{R_0(1-D_1-D_2)} \tag{23}$$

4.2. Power loss analysis

The switch conduction loss is (24).

$$P_{rDS} = \frac{r_{DS} D P_0}{(1-D)^2 R_L} \tag{24}$$

The switching losses is (25).

$$P_{SW} = \frac{1}{6} R_L f (t_{on} + t_{off}) \tag{25}$$

The diode power loss is (26),

$$\begin{aligned} P_{VF} &= V_F I_{0max} \\ P_{RF} &= R_F I_{D_{rms}}^2 \end{aligned} \tag{26}$$

$$I = \frac{I_{0max}}{\sqrt{(1-D_{max})D_{max}}} \quad (27)$$

where, R_F is diode forward resistance and V_F is offset voltage of the diode. The inductor loss is (28).

$$P_{rL} = r_L I_{rms}^2 = r_L I_0^2 = \frac{r_L}{R_L} P_0 \quad (28)$$

The capacitor loss is given in (29), and overall power loss is given in (30).

$$P_{rC} = r_C \frac{\Delta i_L^2}{12} \quad (29)$$

$$P_{loss} = P_{rDS} + P_{SW} + P_{VF} + R_{RF} + P_{rL} + P_{rC} \quad (30)$$

$$\eta = \frac{P_0}{P_0 + P_{loss}} \quad (31)$$

4.3. Calculation of voltage stress

The voltage stress on the switch S_1 is $V_0/2$. And for the switches S_2, S_3, S_4 and S_5 the voltage stress is same which is equal to V_0 . In (32), the voltage stress on the power devices of the converter is presented.

$$\begin{aligned} V_{S_1} &= \frac{V_0}{2} \\ V_{S_2} = V_{S_3} = V_{S_4} = V_{S_5} &= V_0 \end{aligned} \quad (32)$$

4.4. Comparative analysis

The comparative analysis of the proposed configuration is presented in Table 1. In Table 1 the comparison is made with the literature [5], [9], [20]–[23]. The comparison is done in different aspects such as number of switches, diodes, inductors, capacitors and voltage gain.

Table 1. Comparison of proposed converter with the high gain converters in literature

Comparison	[5]	[9]	[20]	[21]	[22]	[23]	proposed
Switch count	3	4	2	2	3	2	5
Diode count	4	6	3	1	5	8	4
Inductor count	2	4	3	4	2	2	2
Capacitor count	5	5	4	2	1	6	2
Total components	14	19	12	8	11	18	13
Possible modes of operation	boost	boost	boost	boost	boost	boost	Boost and buck-boost
Input power flow	Shared	Shared	Shared	Shared	Shared	Shared	Shared
Output voltage	$\frac{V_0}{3(U_{in1} + U_{in2})} = \frac{V_0}{(1-D)}$	$\frac{V_0}{V_{in}(2-d+d^2)} = \frac{V_0}{(1-d)^2}$	$\frac{V_0}{\frac{2V_{i1}}{D(1-D)} + \frac{(2-D)V_{i2}}{D}} = \frac{V_0}{(1-2D)}$	$\frac{V_0}{(1-D)V_{in}} = \frac{V_0}{(1-d_m)}$	$\frac{V_0}{V[2d(1-k) + k(1+d_m)]} = \frac{2V_{in2}}{(1-d_2)}$	$\frac{V_0}{\frac{2V_{in1}}{(1-d_1)} + \frac{2V_{in2}}{(1-d_2)}} = \frac{2V_1 + V_2(1+d_1)}{(1-d_1-d_2)}$	$\frac{2V_1 + V_2(1+d_1)}{(1-d_1-d_2)}$

4.5. Design of converter parameters

The converter parameters are followed from [26]. The Inductance calculation is given in (33), and ripple current through the inductor is given in (34). The calculation of capacitance value is given in (35).

$$L = \frac{2}{27} \frac{R_{Lmax}}{f_s} 2min_{1min} \quad (33)$$

$$\Delta i_{L_{i_{max}}} = \Delta i_{L_{2max}} = \frac{d_{min}(1-d_{min})V_0}{f_s L} \Delta i_{L_{imax}} = \Delta i_{L_{2max}} = \frac{d_{min}(1-d_{min})V_0}{f_s L} \quad (34)$$

$$C = \frac{d_{0max}}{V_{cpp} R_{SLmax} min} \quad (35)$$

Where, d_{max} = Maximum duty ratio, V_0 = Output voltage, f_s = Switching frequency, V_{cpp} = Peak-to-peak value of the capacitor, R_{Lmax} = Maximum load resistance.

$$V_{cpp} = \frac{V_r}{2} \quad (36)$$

The ripple voltage (V_r) is 1% V_0

5. RESULTS AND DISCUSSIONS

5.1. Simulation verification

The proposed converter is simulated with $V_1 = 55$ V, $V_2 = 25$ V, duty ratio is considered as d ($d_1 = 50\%$, $d_2 = 35\%$) and 50 kHz is the switching frequency. The details of the converter parameter are presented in Table 2. Figure 8 presents the switching controlling gate pulses. Figure 9, shows the output voltage (V_0), the voltage across the capacitor, and the load current. The output voltage is validated with derived output voltage expression as (6). The voltage across C_1 is illustrated in Figure 9 which is equal to the input voltage.

Table 2. Parameter specifications

Parameter	Simulation
Input voltage (V_1, V_2)	55, 25 V
Inductors (L)	1.5 mH
Switching frequency (f)	50 kHz
Capacitor (C_1, C)	470, 1000 uF
Output voltage (V_0)	966 V
Output currents (I_0)	1.25 A

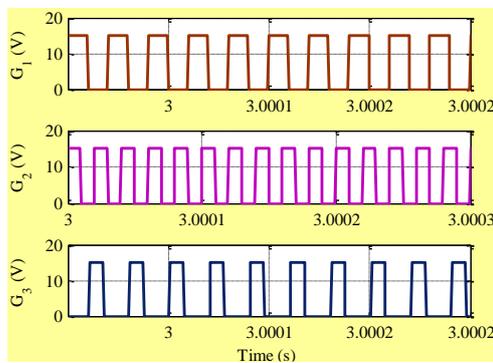


Figure 8. Simulation gate pulses of the switches

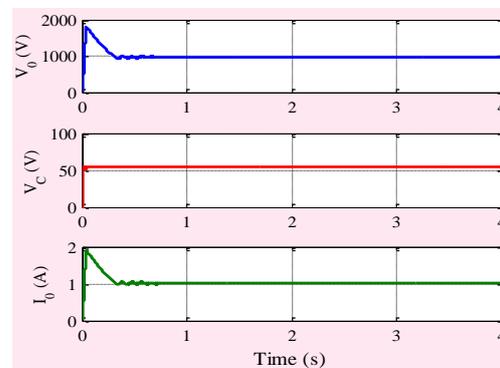


Figure 9. Simulation output voltage, capacitor (C_1) voltage and load current

In mode-1, both the inductors are magnetized parallel up to 50% of duty ratio, and the inductor is magnetized in series with 35% of duty ratio in mode-2, through the active switches of $S_1, S_2,$ and S_3 respectively. The corresponding current through inductor is illustrated in Figure 10. The power devices $S_1, S_2,$ and S_3 voltage stress are shown in Figure 11. The maximum voltage stress is equal to the output voltage. The proposed converter is also verified in buck-boost operation. The corresponding output voltage, inductor currents, and capacitor voltage are depicted in Figure 12. The power loss distribution of the power devices, inductor, and capacitor are illustrated in Figure 13(a). The efficiency vs output power in boost operation is shown in Figure 13(b). The maximum efficiency of the proposed converter is 97.93% at output power of 700 W.

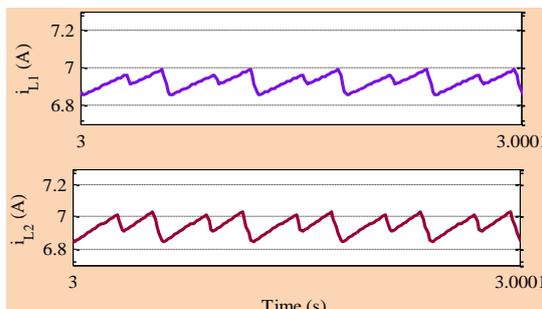


Figure 10. Simulation inductor currents

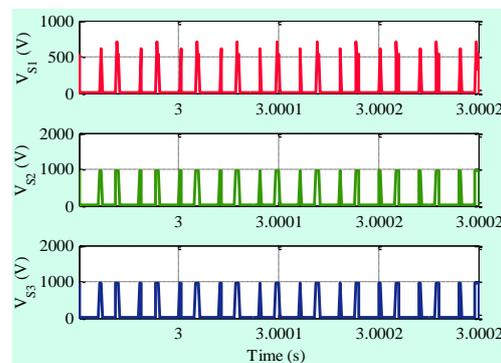


Figure 11. Simulation voltage stress of the switches

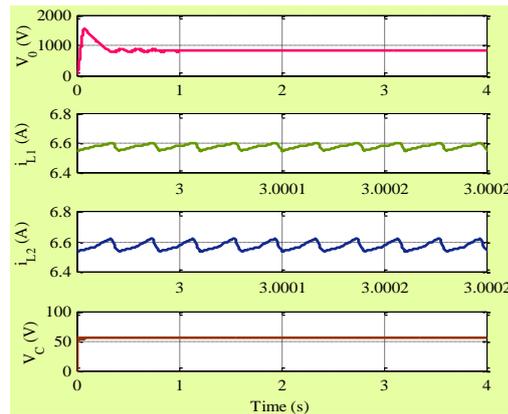


Figure 12. Simulation results in buck-boost operation

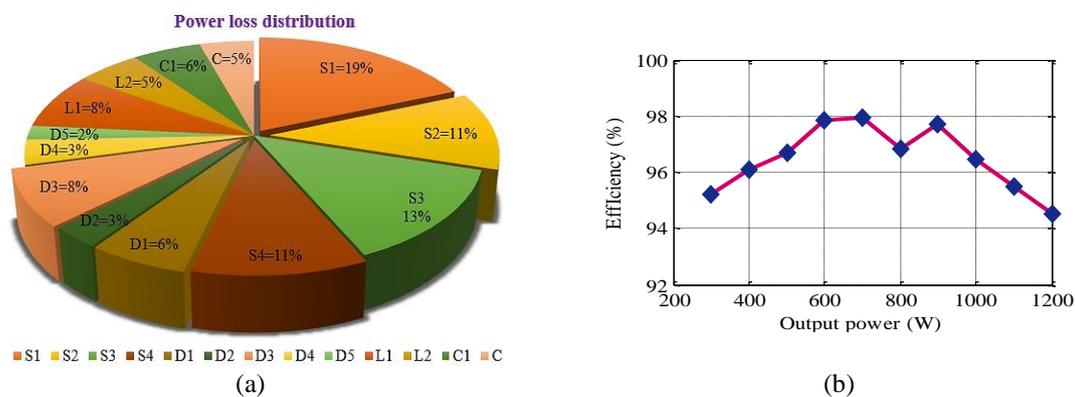


Figure 13. Power loss and efficiency of the proposed converter (a) power loss distribution and (b) efficiency vs output power

6. CONCLUSION

A high-gain non-isolated multi-input DC-DC converter is proposed for EVs' application in this paper. The proposed configuration has improved voltage gain without using of voltage multiplier unit, transformer, and coupled inductor. And also, it has a smaller number of components. In this study, the time-sharing scheme is used in the proposed configuration to achieve a wide range of duty cycle operations which leads to, improved converter performance and utilization of input source. Finally, the performance of the proposed configuration is verified in MATLAB/Simulink environment and results are validated with theoretical analysis.

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