International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 14, No. 3, September 2023, pp. 1624~1632
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v14.i3.pp1624-1632

Optimal design of BiCMOS second generation current conveyor using the genetic algorithm

El Beqal Asmae, Benhala Bachir, Zorkani Izeddine
Faculty of Sciences Dhar El Mahraz, University of Sidi Mohamed Ben Abdellah, Fez, Morocco

Article Info

Article history:

Received Nov 21, 2022
Revised Mar 21, 2023
Accepted Mar 31, 2023

Keywords:

Band pass filter
BiCMOS
Current conveyor
Genetic algorithm
Optimization

ABSTRACT

This article presents an innovative implementation of the plus-type second-generation current conveyor (CCII+) using BiCMOS technology, which combines the benefits of bipolar and CMOS technologies. The optimization problem of minimizing the X-port input resistance and maximizing the current cut-off frequency value was solved using genetic algorithm (GA). The proposed approach allows the optimization of the BiCMOS CCII+ to achieve better performance compared to previous designs. As a practical application, a second-order band-pass filter using the optimized BiCMOS CCII+ was successfully realized. The performance of the proposed design was evaluated using SPICE simulations and compared with previously published works. This study shows that the BiCMOS CCII+ can be effectively optimized using GA to improve its performance, which has potential applications in various analog and mixed-signal circuits.

Corresponding Author:

El Beqal Asmae
Faculty of Sciences Dhar El Mhraz, University of Sidi Mohamed Ben Abdllah
Fez, Morocco
Email: asmae.elbekkal@gmail.com

1. INTRODUCTION

There are currently four viable integrated technologies for analog circuits, known as bipolar, complementary metal–oxide–semiconductor (CMOS), GaAs, and BiCMOS technology. Gallium arsenide (GaAs) technology is maturing very rapidly and offers many possibilities as a niche technology. This technology is well developed for microwave analog circuits, however it's less developed for analog signal processing [1]. GaAs technology's cost and processing time are more important than those of other technologies.

Technology mixed silicon bipolar and complementary metal oxide semiconductor (BiCMOS) comes to combine the main advantages of both bipolar and CMOS technologies in a single integrated circuit. CMOS gives this technology low power dissipation, high input resistance, and small silicon manufacturing area while by using bipolar, high transconductance and high-frequency performance are achieved [2], [3]. With the growing interest in the current mode approach to analog circuit design, the current conveyor is considered as the most prominent current-mode building block which has received huge attention from researchers, academics and circuit designers from around the world.

Since the 1970s, second-generation current conveyors (CCIIs) introduced by Sedra and Smith [4] started to be adapted and utilized in various applications as building blocks with a few other components like diodes, capacitors, resistors. Some of those applications are: Full-wave precision rectifiers, current-mode op-amp, integrators, differentiators, summers [5], filters [6]–[9], inductance simulators [10], [11], Oscillators [12], [13]. By the end of the millennium current-controlled conveyors (CCCIIs) based on BiCMOS technology are utilized to design a high-frequency current mode band-pass filter [10], [14]. Analog circuits

design is a hard task that relies on the designer's experience [15]. In [16], [17], and [18], some optimization techniques have been used named the statistic-based sizing approaches. These techniques are time consuming and require a 'good' starting quiescent point [16].

A few years ago, some (meta-) heuristics were proposed in the literature to deal with the optimal sizing of analog circuits efficiently, including: tabu search (TS) [19], simulated annealing (SA) [20], genetic algorithms (GA) [21]–[23], particle swarm optimization (PSO) [24], [25] ant colony optimization (ACO) [26]–[29] and artificial bee colony (ABC) [30], [31]. The GA is a popular metaheuristic technique known for its ease of use and ability to handle a wide range of optimization, design and application areas [32]. Thus, this research aims to examine how the GA can be utilized to determine the optimal size of BiCMOS plus-type second-generation current conveyors (BiCMOS-CCII+), specifically focusing on achieving minimal parasitic input resistance at port X (R_X) and maximizing the frequency for the current waveform (f_{ci}).

This article is structured as follows: Section 2, presents the proposed method; Section 3, details the circuit topic of the optimization; Optimization/simulation results and a comparison with some published works are highlighted in Section 4; and Section 5, presents the BiCMOS-CCII based second order pass band filter architecture and finally the last section presents the general conclusions of this research.

2. GENETIC ALGORITHM

The genetic algorithm (GA) is a metaheuristic inspired by the process of natural selection [33]. It is used to generate high-quality solutions to optimization and search problems by utilizing biologically-inspired operators such as mutation, crossover, and selection. The process of the genetic algorithm is depicted in Figure 1, which illustrates the flowchart of the algorithm [34].

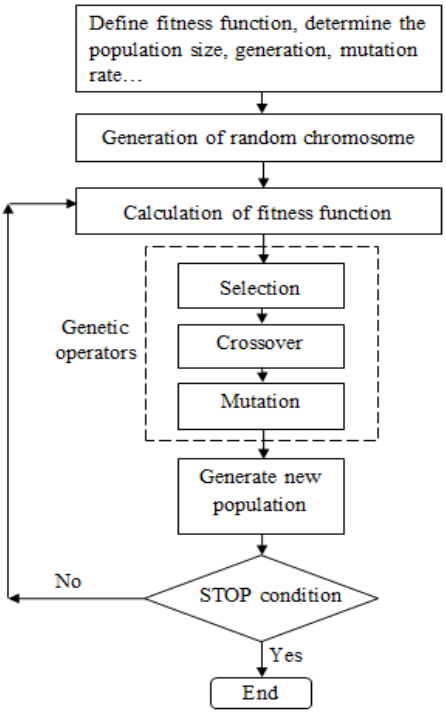


Figure 1. Flowchart of the genetic algorithm

The GA begins by randomly generating a set of solutions (chromosomes) to form the initial population. Each individual in the first population is then evaluated using a fitness function to rank a specific chromosome against all the others. The fittest chromosomes are then selected for reproduction, which involves combining portions of two or more solutions to create new offspring. This process is known as crossover. After crossover, the new offspring may undergo mutation, which involves randomly changing the value of one or more genes in a chromosome with a low probability. This introduces additional variation into the population and can prevent the algorithm from getting stuck in local optima.

Finally, the fittest solutions from the current population are selected to form the next generation, and the process repeats until a satisfactory solution is found or a stopping criterion is met, such as the maximum number of iterations. The genetic algorithm has found applications in numerous domains. Mitchell and Forrest identified nine categories of problems that can be tackled using GA [35], including optimization, machine and robot learning, automated programming, immune system, ecological models, economic models, population genetics models, models of social systems, and interactions between evolution and learning.

3. BICMOS SECOND GENERATION CURRENT CONVEYOR (BiCMOS-CCII+)

The current conveyor is a current mode equivalent of OPAMP in voltage mode circuits. It is a three terminals device as shown in Figure 2 with a describing matrix given in (1) [5].

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \quad (1)$$

Thus, the voltage at port X follows that applied to port Y and the current supplied to X (I_X) is conveyed to the output terminal Z where it is supplied with either positive polarity (in CCII+) or negative polarity (in CCII-). Ideal CCIIs are commonly characterized by low impedance on port X and high impedance on ports Y and Z [36].

The BiCMOS positive second-generation current conveyor circuit is shown in Figure 3 [37]. The two main parts of this circuit are the cascode current mirror formed by bipolar transistors Q1- Q4, and Q5-Q8 and the CMOS translinear loop formed by transistors Ml-M4. The use of CMOS transistors instead of bipolar ones to build the mixed translinear loop provides a very high input resistance at terminal Y while reducing the required silicon area and the power dissipation. On the other hand, the cascode current mirror is more suitable to give a wide dynamic range to operate at low voltage and reduce the power supply as well. It also has a high output resistance, which reduces the load effect.

It has been confirmed that the frequency application range is limited by the current bandwidth, since the current is intrinsically lower than the voltage. Thus, for high-frequency current mode applications, current conveyors (CCs) have to be well sized. Furthermore, due to the non-ideality of CCs, it has been proven that the parasitic X-port resistance (R_X) is one of the most dominant parasitic components that affects CCs' performances. Hence, in this work, we focus on optimizing these two influent performances, i.e. the resistance (R_X) and the current high cut-off frequency (f_{ci}). The small-signal analysis of the circuit yields the following parasitic X-port resistance expression:

$$R_X \cong \frac{1}{gm_3+go_3+gm_4+go_4} \quad (2)$$

where, g_m and g_o are the transconductance and the conductance of the corresponding MOS transistor, respectively.

According to the study of the high-frequency equivalent circuit of BiCMOS CCII+ where C_{gd}, C_μ and ro have been neglected during the analysis, we have obtained the following current transfer function:

$$A_i = \frac{I_Z}{I_X} = \frac{g_m^2(g_{m4}+g_{o4})}{s^3 2C_{gs4}C_\pi^2+s^2(2(g_{m4}+g_{o4})C_\pi^2+2C_{gs4}C_\pi(\frac{1}{r_\pi}+2g_{mQ}))+s((g_{m4}+g_{o4})(2C_\pi(\frac{1}{r_\pi}+2g_{mQ})+g_{mQ}C_{gs4}(g_{mQ}+g_{o4}+\frac{2}{r_\pi}))+g_{mQ}(g_{m4}+g_{o4})(g_{mQ}+\frac{2}{r_\pi})} \quad (3)$$

The equation above is a transfer function of 3rd order low pass filter and the expression for the upper 3 dB frequency of this filter is given as [38]:

$$\omega_H \cong \frac{1}{\sqrt{\left(\frac{1}{\omega_{P1}^2}+\frac{1}{\omega_{P2}^2}+\cdots\right)-2\left(\frac{1}{\omega_{Z1}^2}+\frac{1}{\omega_{Z2}^2}+\cdots\right)}} \quad (4)$$

where, ω_{P1}, ω_{P2},..., and ω_{Z1}, ω_{Z2},..., are respectively the location of poles and zeros appearing in the transfer function. The approximate current high cut off frequency for a BiCMOS CCII+ is given as:

$$f_{ci} \cong \frac{1}{2\pi\sqrt{\left(\frac{1}{\omega_{P1}^2}+\frac{1}{\omega_{P2}^2}+\frac{1}{\omega_{P3}^2}\right)}} \quad (5)$$

The approximate pole locations P1, P2 and P3 are calculated by using (3) and MATLAB, but their expressions are not mentioned because of their huge number of terms.

In the following section, we adopted the GA to minimize R_X and to maximize f_{ci}, those two objective functions are limited by specific constraints, which ensure that the CMOS transistors of the BiCMOS-CCII+ operate in the saturation mode. Where, C_{OX}, μ_N, μ_P, V_T, I_{SN} and I_{SP} are technological parameters.

$$\frac{V_{DD}}{2} + \sqrt{\frac{2I_0}{\mu_P C_{ox}\frac{W_4}{L_4}}} \geq 2V_T \, ln\left(\frac{I_0}{I_{SN}}\right) \tag{6}$$

$$\sqrt{\frac{2I_0}{\mu_N C_{ox}\frac{W_3}{L_3}}} - \frac{V_{DD}}{2} \leq 2V_T \, ln\left(\frac{I_0}{I_{SP}}\right) \tag{7}$$

The first objective function, R_X, has decision variables that involve the sizes of the NMOS and PMOS transistors, which include the lengths of the channels (LN and LP) and the widths of the gates (WN and WP) and for the second function, f_{ci}, we add to the geometric dimensions above, the current gain (β) and the base-emitter junction capacitance (Cπ) of bipolar transistors.

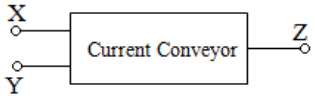


Figure 2. Current conveyor block diagram

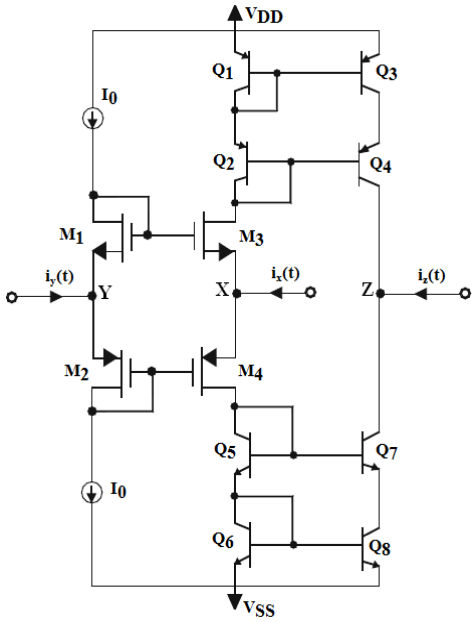


Figure 3. A positive second-generation current conveyor (BiCMOS CCII+)

4. OPTIMIZATION/ SIMULATION RESULTS

In this section, the GA algorithm was performed to optimize the BiCMOS CCII+ with the parameters given in Table 1. This algorithm is implemented in MATLAB and linked to SPICE software to measure performances. The simulation conditions are listed in Table 2 and the way to set the hybrid parameters of the BJT-transistor in the spice platform is detailed in [21]. Table 3 presents the optimal geometric measurements for the MOS transistors and hybrid parameters achieved using the GA. The comparison between the theoretical and simulation values reveals that the two results are in good agreement.

Table 1. The parameters of GA

Parameter	Value
Population size	800
Iteration cycles	1000
Crossover	Arithmetical Crossover
Mutation rate	0.01
Selection probability	50%

Table 2. The simulation conditions of the circuit

Condition	Value
Technology	CMOS AMS 0.35 µm
Bias current	100 µA
Voltage Supply	-2.5v/+2.5v
NPN transistor	Q2N2222A
PNP transistor	Q2N2907

Table 3. Optimization and simulation results for R_X and f_{ci}

	LN (µm)	WN (µm)	LP (µm)	WP (µm)	β	Cπ (fF)	Optimal value	Simulation value
R_{X_min} (Ω)	0.56	174.86	0.35	296.33	__	__	150.13	213.54
f_{ci_max} (GHz)	0.37	04.10	0.35	11.50	650	74	1.833	1.979

We present in Figures 4 and 5 spice simulation results using the optimal values presented in Table 3, respectively, of R_X and f_{ci}. In Table 4, we present a comparison of performances according to the technology and the metaheuristic used. It can be clearly noticed that the GA outperforms the other metaheuristics for both technologies (BiCMOS and CMOS) while the CCII based on BiCMOS technology reached the best performances.

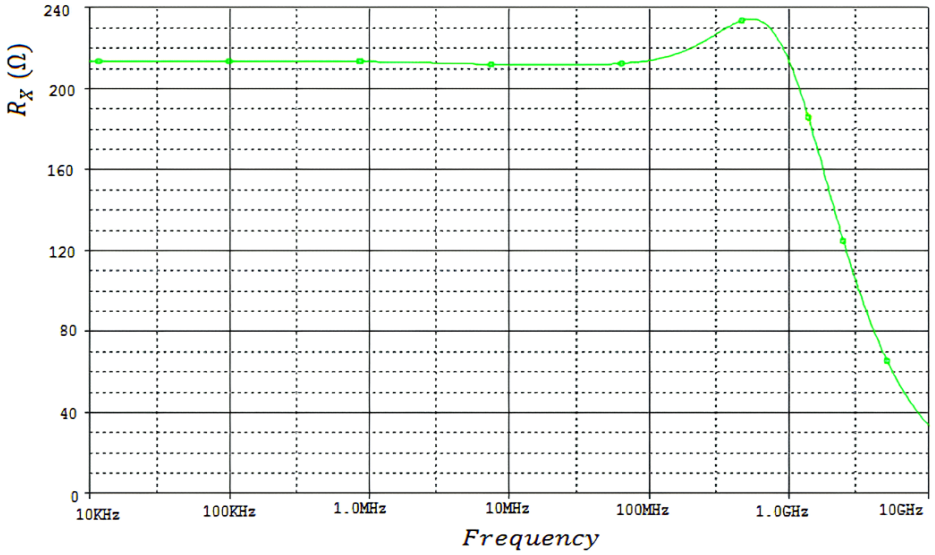


Figure 4. Variation of R_X (ohm) vs frequency (Hz) using GA

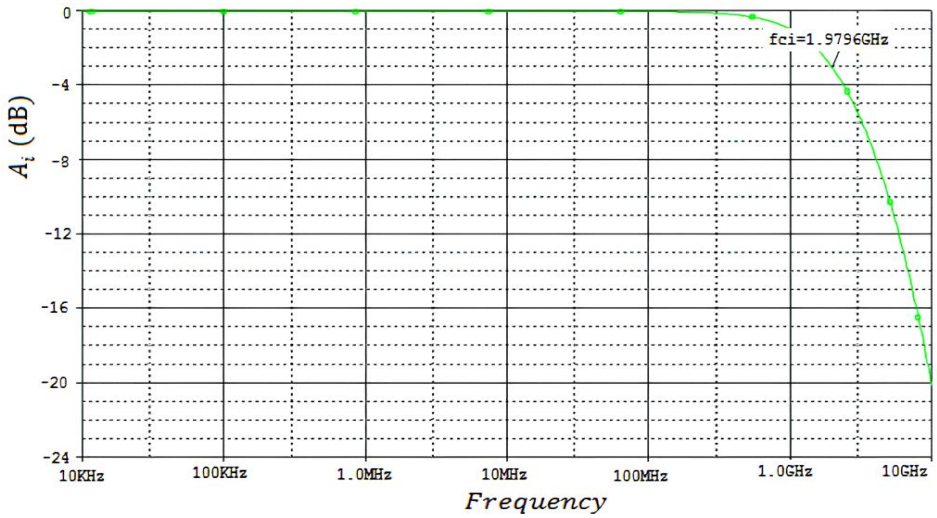


Figure 5. Current gain A_i (dB) vs frequency (Hz) using GA

Table 4. Comparison of performances

	Technology	f_{ci_max} (GHz)	R_{X_min} (Ω)
GA	BiCMOS	1.833	150.13
GA [39]	CMOS	1.841	435.19
ACO [22]	CMOS	1.792	443.00
PSO [40]	CMOS	1.751	464.00

5. APPLICATION: CURRENT-MODE SECOND ORDER BAND PASS FILTER BASED ON BICMOS CCII+

In this section, we present a second-order current-mode band-pass filter based on impedance simulation [10]. The Figure 6 shows the implementation of this filter by using four plus-type current conveyors and two capacitors [36]. The two current conveyors (CCII+ (1) and CCII+ (2)) and capacitor (C1) are equivalent to the non-ideal inductance (i.e., an inductance having a parasitic positive resistance in parallel, see Figure 7. The connection of the third CCII+ as shown in Figure 8 builds a controlled negative resistor used for nulling the effects of the parasitic shunt resistors (R_{x1} and R_{x2}), while the fourth builds the output current source. Therefore, by considering C2 equal to the shunt capacitor C, the studied filter is equivalent to a shunt RLC circuit, where its transfer function is given by [36]:

$$H(s) = \frac{I_{\text{out}}}{I_{\text{in}}}(s) = \frac{\left[\left(\frac{R_{x1}R_{x2}C_1}{R_{x4}}\right)\right]s}{1+\left[\left(\frac{R_{x1}R_{x2}C_1}{R_G}\right)\right]s+(R_{x1}R_{x2}C_1C_2)s^2} \quad (8)$$

with:

$$\frac{1}{R_G} = \frac{1}{R_{x1}} + \frac{1}{R_{x2}} - \frac{1}{R_{x3}} + \frac{1}{R_{x4}}$$

where Rx1, Rx2, Rx3 and Rx4 are the X-port parasitic resistances of the corresponding CCII+. The expression of the resonance frequency is given by:

$$f_o = \frac{1}{2\pi}\sqrt{\frac{1}{R_{x1}R_{x2}C_1C_2}} \quad (9)$$

The second-order band pass filter was simulated using SPICE software, where the optimized CCII+ with the optimal parameters shown in Table 3 was used. Therefore, two filters are considered: the first is based on CCII+ which provides the lowest R_X, while the second is based on CCII+ which provides the highest f_{ci}. Figure 8 illustrates the simulated transfer response obtained for the two filters, with C1= C2 = 0.1pF. We can notice from Table 5 that the GA gives the highest resonance frequency in the case of the filter based on BiCMOS CCII+ giving the maximum of f_{ci} and for the filter giving the lowest R_X based on CMOS technology.

Table 5. The obtained resonance frequencies

		R_{X_min}	f_{ci_max}
fo (MHz)	GA (BiCMOS)	319.257	694.586
	GA (CMOS) [39]	736.643	639.397
	ACO (CMOS) [41]	497.896	641.389

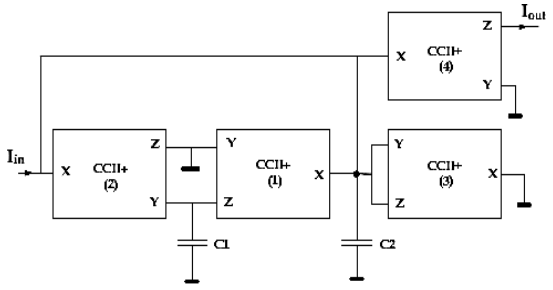


Figure 6. Current-mode second order band pass filter

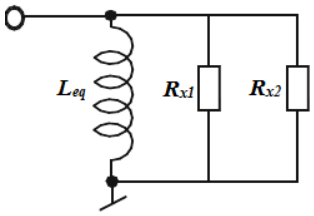


Figure 7. Non-ideal inductance with Leq=R_{x1}.R_{x2}.C, where C is the sum of the capacitor C1 and the shunt parasitic input–output capacitors on ports Y and Z of the CCII+

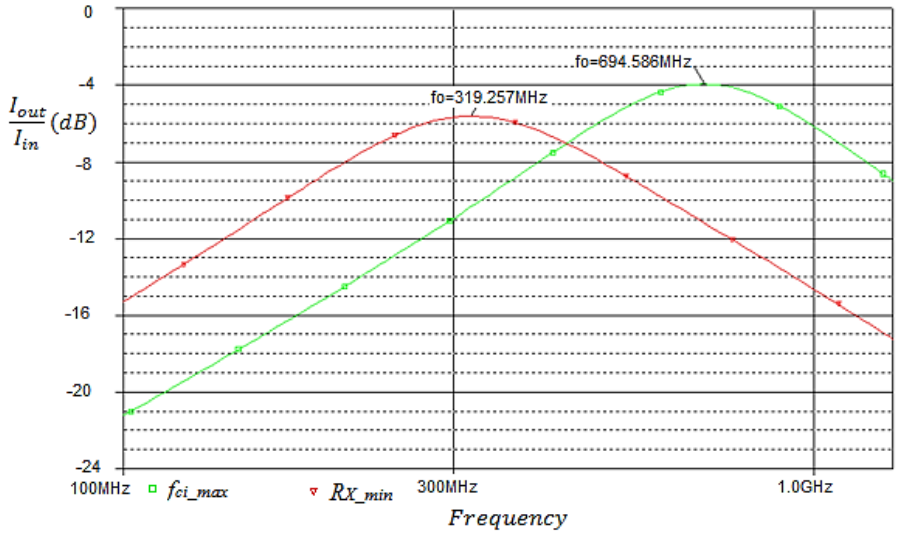


Figure 8. Resonance frequency of the second order current mode band-pass filter

6. CONCLUSION

In this work, an optimal design of BiCMOS CCII+ has been given by using the genetic algorithm (GA). The proposed CCII has a very low input resistance at terminal X compared to his counterpart in technology CMOS and a high current cut off frequency exceeding the GHz. The obtained results prove that the GA is capable of producing better results in comparison with other metaheuristics. As an application, a BiCMOS CCII+ based current mode second order band pass filter was proposed. The proposed algorithm's viability is demonstrated by SPICE simulation results.

REFERENCES

[1] C. Toumazou and D. G. Haigh, "Design of A high-gain, single-stage operational amplifier for GaAS switch ed-capacitor filters," *Electronics Letters*, vol. 23, no. 14, pp. 752–754, 1987, doi: 10.1049/el:19870533.

[2] H. Ercan and M. Alçi, "A new design for a BiCMOS controlled current conveyor," *Elektronika ir Elektrotechnika*, vol. 19, no. 1, pp. 56–60, 2013, doi: 10.5755/j01.eee.19.1.3257.

[3] W. Tangsrirat, "Simple BiCMOS CCCTA design and resistorless analog function realization," *Scientific World Journal*, vol. 2014, 2014, doi: 10.1155/2014/423979.

[4] A. Sedra and K. Smith, "A second generation current conveyor and its application," *IEEE Transactions on circuit theory*, vol. 17, no. 1, pp. 132–134, 1970.

[5] R. Senani, D. R. Bhaskar, and A. K. Singh, "Current conveyors: Variants, applications and hardware implementations," *Current Conveyors: Variants, Applications and Hardware Implementations*, pp. 1–560, 2015, doi: 10.1007/978-3-319-08684-2.

[6] H. Aminzadeh, "Nano-scale area-efficient Gm–C filters using MOS capacitors," *International Journal of Electronics Letters*, vol. 7, no. 3, pp. 311–320, 2019, doi: 10.1080/21681724.2018.1494319.

[7] C. Zhu, C. Wang, H. Chen, X. Zhang, J. Sun, and S. Du, "A novel CMOS CCCII with wide tunable Rx and its application," *Journal of Circuits, Systems and Computers*, vol. 27, no. 13, 2018, doi: 10.1142/S0218126618501980.

[8] A. Ranjan, M. Ghosh, and S. K. Paul, "Third-order voltage-mode active-C band pass filter," *International Journal of Electronics*, vol. 102, no. 5, pp. 781–791, 2015, doi: 10.1080/00207217.2014.942803.

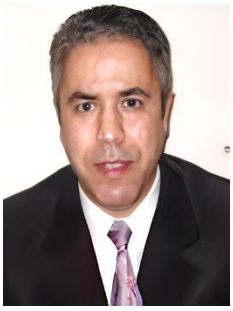
[9] N. Herencsar, A. Kartci, J. Koton, G. Tsirimokou, and C. Psychalinos, "Voltage gain-controlled third-generation current conveyor and its all-pass filter verification," *2017 European Conference on Circuit Theory and Design, ECCTD 2017*, 2017, doi: 10.1109/ECCTD.2017.8093273.

[10] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "High-frequency high-Q BiCMOS current-mode bandpass filter and mobile communication application," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 4, pp. 614–625, Apr. 1998, doi: 10.1109/4.663567.
[11] S. Ben Salem, D. S. Masmoudi, and M. Loulou, "A novel CCII-based tunable inductance and high frequency current-mode band pass filter application," *Journal of Circuits, Systems and Computers*, vol. 15, no. 6, pp. 849–860, 2006, doi: 10.1142/S0218126606003386.
[12] J. W. Horng, "A sinusoidal oscillator using current-controlled current conveyors," *International Journal of Electronics*, vol. 88, no. 6, pp. 659–664, 2001, doi: 10.1080/00207210110044369.
[13] S. Ben Salem, A. Ben Saied, and D. S. Masmoudi, "High-performance current-controlled quadrature oscillator using an optimized CCII," *Informacije MIDEM*, vol. 46, no. 2, pp. 91–99, 2016.
[14] A. Fabre, O. Saaid, F. Wiest, and C. Boucheron, "Current controlled bandpass filter based on translinear conveyors," *Electronics Letters*, vol. 31, no. 20, pp. 1727–1728, 1995, doi: 10.1049/el:19951225.
[15] A. R. Conn, P. K. Coulman, R. A. Haring, G. L. Morrill, and C. Visweswariah, "Optimization of custom MOS circuits by transistor sizing," in *The Best of ICCAD*, Boston, MA: Springer US, 2003, pp. 347–364. doi: 10.1007/978-1-4615-0292-0_28.
[16] M. Loulou, S. Ait Ali, M. Fakhfakh, and N. Masmoudi, "An optimized methodology to design CMOS operational amplifier," *Proceedings of the International Conference on Microelectronics, ICM*, vol. 2002-Janua, pp. 14–17, 2002, doi: 10.1109/ICM-02.2002.1161486.
[17] F. Silveira, D. Flandre, and P. G. A. Jespers, "A gm/ID based methodology for the design of CMOS analog circuits and its application to the synthesis of a silicon-on-insulator micropower OTA," *IEEE Journal of Solid-State Circuits*, vol. 31, no. 9, pp. 1314–1319, 1996, doi: 10.1109/4.535416.
[18] F. Medeiro, R. Rodríguez-Macías, F. V. Fernández, R. Domínguez-Castro, J. L. Huertas, and A. Rodríguez-Vázquez, "Global design of analog cells using statistical optimization techniques," *Analog Signal Processing*, pp. 3–19, 1994, doi: 10.1007/978-1-4757-4503-0_1.
[19] F. Glover, "Tabu Search—Part I," *ORSA Journal on Computing*, vol. 1, no. 3, pp. 190–206, 1989, doi: 10.1287/ijoc.1.3.190.
[20] J. Dreo, A. Petrowsdki, P. Siarry, E. Taillard, and A. Chatterjee, "Metaheuristics for hard optimization: methods and case studies," 2003.
[21] E. B. Asmae, B. Benhala, and I. Zorkani, "A genetic algorithm for the optimal design of a multistage amplifier," *International Journal of Electrical and Computer Engineering*, vol. 10, no. 1, pp. 129–138, 2020, doi: 10.11591/ijece.v10i1.pp129-138.
[22] B. Benhala and O. Bouattane, "GA and ACO techniques for the analog circuits design optimization," *Journal of Theoretical and Applied Information Technology*, vol. 64, no. 2, pp. 413–418, 2014.
[23] N. Elmouhi, A. Essadki, and H. Elaimani, "Robust control of wind turbine based on doubly-fed induction generator optimized by genetic algorithm," *International Journal of Power Electronics and Drive Systems*, vol. 13, no. 2, pp. 674–688, 2022, doi: 10.11591/ijpeds.v13.i2.pp674-688.
[24] B. Abdelkader, A. Merabti, and B. Yamina, "Using PSO algorithm for power flow management enhancement in PV-battery grid systems," *International Journal of Power Electronics and Drive Systems*, vol. 14, no. 1, pp. 413–425, 2023, doi: 10.11591/ijpeds.v14.i1.pp413-425.
[25] B. Benhala, P. Pereira, and A. Sallem, "Focus on swarm intelligence research and applications," *Focus on Swarm Intelligence Research and Applications*, pp. 1–284, 2017.
[26] B. Benhala, "Sizing of an inverted current conveyors by an enhanced ant colony optimization technique," *2016 Conference on Design of Circuits and Integrated Systems, DCIS 2016 - Proceedings*, pp. 49–54, 2017, doi: 10.1109/DCIS.2016.7845271.
[27] B. Benhala *et al.*, "Application of the ACO technique to the optimization of analog circuit performances," *Analog Circuits: Applications, Design and Performance*, pp. 235–255, 2012.
[28] B. Benhala, A. Ahaitouf, A. Mechaqrane, and B. Benlahbib, "Multi-objective optimization of second generation current conveyors by the ACO technique," *Proceedings of 2012 International Conference on Multimedia Computing and Systems, ICMCS 2012*, pp. 1147–1151, 2012, doi: 10.1109/ICMCS.2012.6320142.
[29] D. Yadav and A. Verma, "Comperative performance analysis of PMSM drive using MPSO and ACO techniques," *International Journal of Power Electronics and Drive Systems*, vol. 9, no. 4, pp. 1510–1522, 2018, doi: 10.11591/ijpeds.v9.i4.pp1510-1522.
[30] B. Benhala, H. Bouyghf, A. Lachhab, and B. Bouchikhi, "Optimal design of second generation current conveyors by the Artificial Bee Colony technique," *Intelligent Systems and Computer Vision, ISCV 2015*, 2015, doi: 10.1109/ISACV.2015.7106172.
[31] H. Bouyghf, B. Benhala, and A. Raihani, "Analysis of the impact of metal thickness and geometric parameters on the quality factor-Q in integrated spiral inductors by means of artificial bee colony technique," *International Journal of Electrical and Computer Engineering*, vol. 9, no. 4, pp. 2918–2931, 2019, doi: 10.11591/ijece.v9i4.pp2918-2931.
[32] M. A. A. Albadr, S. Tiun, M. Ayob, and F. T. AL-Dhief, "Spoken language identification based on optimised genetic algorithm–extreme learning machine approach," *International Journal of Speech Technology*, vol. 22, no. 3, pp. 711–727, 2019, doi: 10.1007/s10772-019-09621-w.
[33] R. L. Haupt and S. E. Haupt, "Practical GeneticAlgorithms," *John Wiley & Sons*, 2004.
[34] M. Mitchell, "Genetic Algorithms: An Overview," *An Introduction to Genetic Algorithms*, 2020, doi: 10.7551/mitpress/3927.003.0003.
[35] M. Mitchell and S. Forrest, "Genetic algorithms and artificial life," *Artificial Life*, vol. 1, no. 3, pp. 267–289, 1994, doi: 10.1162/artl.1994.1.267.
[36] A. Sallem, M. Fakhfakh, and M. Loulou, "Optimizing CMOS current conveyor through MOGA and high frequency applications," pp. 1–5, 2009.
[37] M. A. Yakout, A. I. Abdelfattah, and A. S. Elbazz, "BiCMOS current conveyor: Design and application," *Proceedings - IEEE International Symposium on Circuits and Systems*, vol. 3, pp. III-463-III–466, 2000, doi: 10.1109/ISCAS.2000.856097.
[38] A. S. Sedra, K. C. (Kenneth C. Smith, and A. N. Chandorkar, "Microelectronic circuits : theory and applications," p. 1384, [Online]. Available: https://oup.com.pk/microelectronic-circuits-sixth-edition.html
[39] E. B. Asmae, B. Bachir, G. Amel, K. Mouna, F. Mourad, and Z. Izeddine, "Synthesis of a current mode second order band pass filter using the Genetic Algorithm," *International Conference on Optimization and Applications, ICOA*, 2019, doi: 10.1109/ICOA.2019.8727706.
[40] B. Benhala, "Metaheuristic techniques for the analog circuits performances optimization -a comparison issue- overview on," *WSEAS Transactions on Circuits and Systems*, vol. 14, pp. 174–182, 2015.
[41] K. Loubna, B. Bachir, and Z. Izeddine, "Advanced design of current-mode pass-band filter using ant colony optimization technique," *Advances in Science, Technology and Engineering Systems*, vol. 5, no. 6, pp. 995–1000, 2020, doi: 10.25046/AJ0506119.

BIOGRAPHIES OF AUTHORS

El Beqal Asmae was born in Sefrou, Morocco, in 1991. She received Master degree in industrial engineering at Faculty of Sciences and Technologies (FST Fez), Sidi Mohamed Ben Abdellah University in 2015. She is currently a PhD student at Faculty of Sciences Dhar el Mahraz, Fez, Morroco. She can be contacted at email: asmae.elbekkal@gmail.com.

Benhala Bachir is Professor at Faculty of Sciences Dhar el Mahraz, Fez, Morroco. He received the Master degree in microelectronics and telecommunication systems and the Ph.D degree in electronics and microelectronics, both from the faculty of science and technology (FST) of Fez, Morocco. His current research interests are in the fields of Metaheuristics optimization techniques, analog design automation and digital/analog VLSI architecture. He is the author of several books/ book chapters and more than 60 articles in universally referenced Journals. He is regularly served as a reviewer in international journals and conferences. He was the General Chair of the ICOA2017/IEEE IRASET2020/2022/ICEGC2021. He can be contacted at email: bachir.benhala@usmba.ac.ma.



Zorkani Izeddine is Professor at Faculty of Sciences Dhar el Mahraz, Fez, Morroco. He has 30 years of experience in Nanosciences with a focus on solar energy applications. Previous interests include Low Dimensional Systems and Nano-materials. Dr Zorkani has produced numerous formal scientific publications & scientific reports. He has co-initiated the Moroccan association of nanotechnology (AMANAT), the North Africa of the nanoscience African network (NANOAFNET), the African network of solar energy (ANSOLE), the Moroccan society of renewable energies and the renewable energy University Network (REUNET). He is member of the African Laser Centre, member of the African Future Earth Committee-ICSU and Responsible of a Federation Scheme with the Abdus Salam International Centre for Theoretical Physics (ICTP, Trieste – Italy). He is Responsible of a Research Group “Nanomaterials and Renewable Energies”, Solid state Laboratory, Faculty of Sciences Dhar Mehraz, University Sidi Mohamed Ben Abdellah. He can be contacted at email: izorkani@hotmail.com.