Optimization of switching losses of the Weinberg converter

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Article Info	ABSTRACT
	DC-DC converters are widely used in hybrid power supply systems. A buffer source of electrical energy (most often a battery bank) and its charging and discharging devices are integral parts of such systems. In systems where the battery bank voltage is less than the DC-bus voltage and galvanic isolation is not required, the Weinberg converter is widely used as a discharge device, for example, in spacecraft power supply systems. The current trend in the development of hybrid power supply systems is to increase the power density of the system. Increasing the operating frequency is the simplest and most effective way to increase the power density of converter. A differential characteristic of this converter is the zero-current switching (ZCS) of transistors, which occurs due to the influence of the leakage inductance of coupled-inductors and the leakage inductance of the transformer. The paper presents an analysis of the influence of leakage inductances on the operation of the converter and a method of determining a level of turn on switching losses of transistors, which allows to ensure the necessary level of efficiency of the converter. The results of simulation modeling of the converter confirm the effectiveness of this method.

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1. INTRODUCTION

PWM DC-DC converters are widely used in various energy conversion systems [1], [2]. One of the most common applications of these converters are hybrid power supply system's [3]–[13]. A buffer source of electrical energy, most often a battery bank, is an integral part of hybrid power supply systems. It provides power supply to the system when the power of the main source of electrical energy is reduced or it is turned off. Often, the main source of electricity of hybrid power supply systems are renewable source of electric energy, such as solar panels and wind generators. Uninterrupted power supply cannot be provided, because the generation of electric energy depends on external factors. The direct current generated by renewable sources of electrical energy is in good agreement with the storing of energy in the battery bank.

Most often, to reduce the overall dimensions of the system, the battery bank voltage is chosen to be less than the main DC-bus voltage of the system. To charge the battery bank in such systems, step-down DC-DC converters are used. And for the discharge, step-up DC-DC converters are used. In power supply system's where galvanic isolation of electrical sources is not required, non-isolated DC-DC converters are used, an example of such systems is the spacecraft power supply system. The Weinberg converter is widely used as the battery discharge device and it is characterized by a higher power density and reliability than the

initially used step-up DC-DC converter [14]. Increasing the frequency of the converter is the easiest way to increase its power density. However, as the frequency increases, the switching losses of transistors increase too, they are the main losses of the converter. One of the ways to reduce switching losses is application of soft switching methods [15]–[17].

The differential characteristic of this converter is zero-current switching (ZCS) of transistors, when they are turn on. Which is a result of the effect of the leakage inductance of coupled-inductors and the leakage inductance of the transformer [18]. This factor allows to achieve higher efficiency values in comparison with existing analogues [14], [19]. In this paper, the operational analysis of the Weinberg converter with account for the leakage inductance of coupled-inductors and the leakage inductance of the transformer was presented. A method of determining a level of turn on switching losses of transistors had been developed. Analytical expressions for determining the basic parameters of the converter have been deduced. The basis of the developed method is to set the necessary leakage inductance of coupled-inductors, calculated based on a given level of switching losses. Finally, the proposed work has been validated through simulation.

2.   OPERATING PRINCIPLE

In this section the description of the operating principle of the converter, taking into account the influence of leakage inductances of the coupled-inductors and transformer is given. Figure 1 shows the Weinberg converter [20]–[23]. The converter has one input and it is powered by an independent source of electrical energy – the battery bank. The output of the converter is the load power DC-bus. For this converter, the transformer ratio $K_T=1$. The inductance values of coupled-inductors are equal ($L_{1.2}=L_{1.1}$). C_1 is input capacitor filter, it provides filtering of the input voltage of a nonideal source. C_2 is output capacitor filter, it provides the required output voltage quality. MOSFETs are used as main power switches, because the switching frequency is high. The full operation cycle of the converter consists of 8 switching stages of power switches. Figure 2 shows the waveforms of the converter. Figure 3 shows circuit stages.

i) Stage 1 (t_1): This stage starts when the transistor VT_1 turns on, the diode VD_2 turns on too. This is the soft turn on stage zero-current switching (ZCS), leakage inductances of coupled-inductors ($L_{S(L1)}$) and the transformer ($L_{S(TV1)}$) provide more slowly rise of the transistor current. This stage ends when the diode VD_1 turns off. The stage duration as (1) [20]:

$$t_1 = \frac{L_{S(L1)}+L_{S(TV1)}}{U_{in}} I_{load}   \tag{1}$$

where $I_{load} = \frac{P_{out}}{U_{out}}$ – load current, U_{in} – input voltage, P_{out} – output power, U_{out} – output voltage.

ii) Stage 2 (t2): During this stage the transistor VT1 and the diode VD2 are on. The stage duration as (2):

$$t_2 = D \cdot T_S - t_1   \tag{2}$$

where D – duty cycle, $T_S = 1/2 \cdot f_{sw}$ – operating period, f_{sw} – switching frequency.

iii) Stage 3 (t3): During this stage the transistor VT1 is off, diodes VD1 and VD3 turns on, the diode VD2 is on, the leakage inductance of coupled-inductors provide the flow of current through the diode VD1. As the inductor current L1.2 rises the inductor current L1.1 falls at the same rate to keep a constant ampere-turns in the core. In this transition the inductor current L1.1 keeps flowing to the output through VD2 and VD3, producing a spike in the output current. The stage duration as (3) [20]:

$$t_3 = \frac{L_{S(L1)}}{U_{out}-U_{in}} \cdot I_{load}   \tag{3}$$

iv) Stage 4 (t4): During this stage the diode VD1 is on. The stage duration as (4):

$$t_4 = \left(\frac{1}{2} - D\right) \cdot T_S - t_3   \tag{4}$$

v) Stage 5 (t5): This stage starts when the transistor VT2 turns on, the diode VD3 turns on too. This stage ends when diode VD1 turns off. This stage is similar to stage 1. The stage duration follows by (1). Stage 6 (t6): During this stage the transistor VT2 and the diode VD3 are on. This stage is similar to stage 2. The stage duration by (2). Stage 7 (t7): During this stage the transistor VT1 is off, diodes VD1 and VD3 turns on, diode VD3 is on. This stage is similar to stage 3. The stage duration by (3). Stage 8 (t8):

During this stage the diode VD1 is on. This stage is similar to stage 4. The stage duration by (4). Hard switching converter works without stages 1, 3, 5 and 7 (LS(L1) = LS(TV1) ≈ 1 nH).

Based on Figure 3, analytical expressions for determining the basic parameters of the converter are obtained. The inductance value of coupled-inductors ($L_{1.1}=L_{1.2}$):

$$L_{1.1} = \frac{D \cdot (2 \cdot U_{in} - U_{out})}{2 \cdot \Delta I_{L1.1} \cdot f_{sw}} \tag{5}$$

The value of the output capacitance C_2 taking into account the influence of stages 3 and 7:

$$C_2 = \frac{P_{out}^2 \cdot L_{S(L1)}}{2 \cdot \Delta U_{out} \cdot U_{out}^2 \cdot (U_{out} - U_{in})} \tag{6}$$
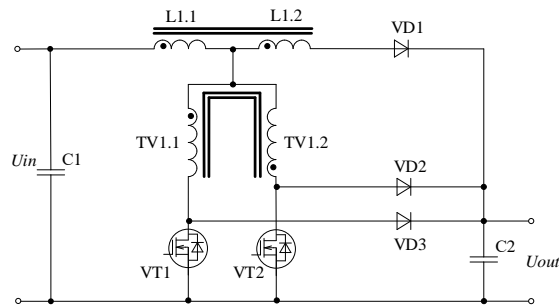

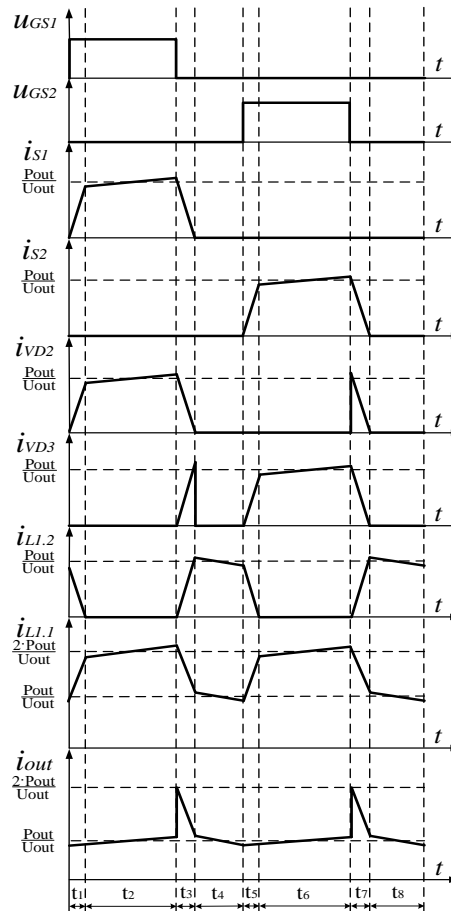Figure 1. Weinberg converter

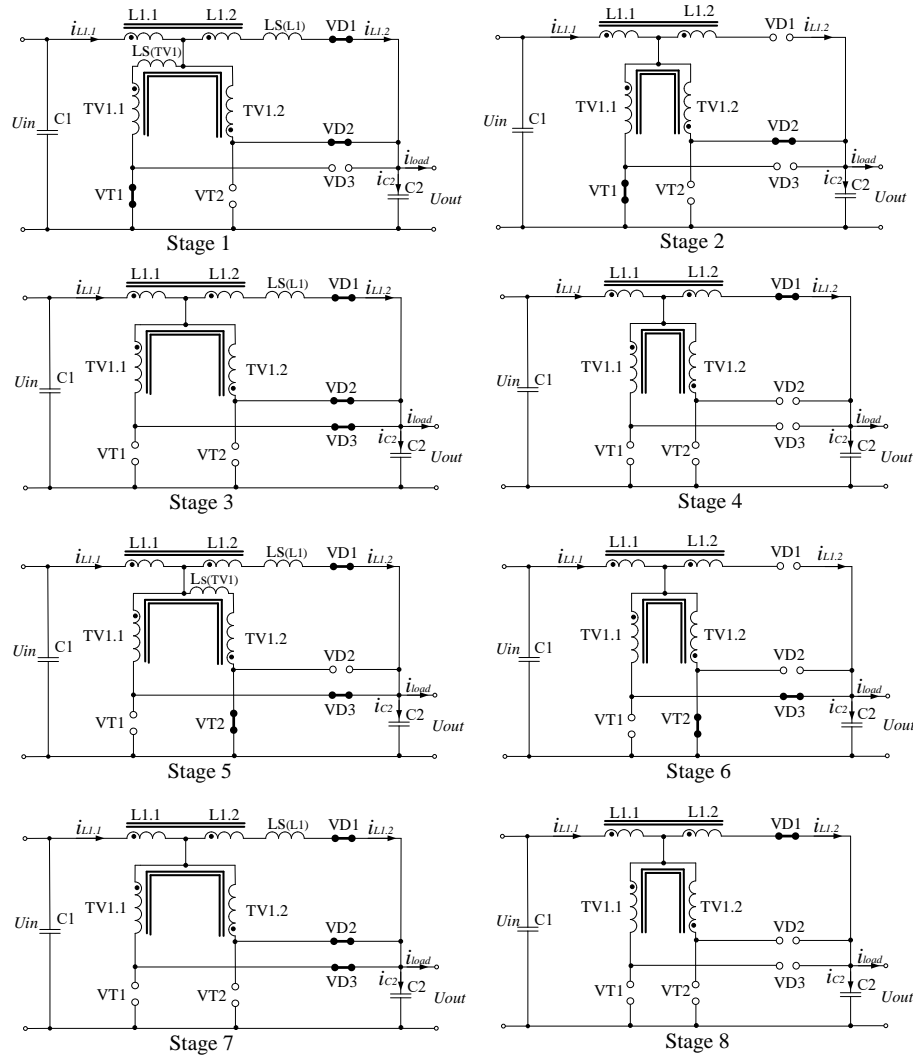
Figure 2. Theoretical waveforms of the converter

Figure 3. Equivalent circuits of converter stages

3.   THE PROPOSED METHOD

The leakage inductance of coupled-inductors L_1 and the leakage inductance of the transformer TV_1 provide the appearance of stages 1, 3, 5 and 7. Stages 1 and 5 are soft turn on stages of transistors VT_1 and VT_2. Stages 3 and 7 are stages of spike in the output current, these stages increase the current stress of the output capacitor C_2, the rms value of the capacitor current is determined by (7).

$$I_{C2(rms)} = \frac{2 \cdot U_{in} - U_{out}}{4 \cdot \sqrt{12} \cdot L_{1.1}} \cdot D \cdot T_S + I_{load} \cdot \sqrt{\frac{t_3 \cdot f_{sw}}{6}} \qquad (7)$$

Turn on switching losses depend on the leakage inductance value of coupled-inductors L_1 ($L_{S(L1)}$ is the total leakage inductance of coupled-inductors) and the leakage inductance value of the transformer ($L_{S(TV1)}$ is the leakage inductance of one winding of the transformer), simplifying of calculation $L_{S(TV1)}$ is accepted as a constant and $L_{S(TV1)} << L_{S(L1)}$. Then the duration of stages 1 and 5 will be determined by the value $L_{S(L1)}$. Figure 4 shows drain-source voltage and drain current waveforms of the transistor in consideration with hard and soft switching.

The duration t_1 is determined according to (1), durations t_r, t_{ir} and t_f, t_{vr} are determined by parameters and drain-source voltages of transistors VT_1 and VT_2. Formulas for the switching transients are given in [24], [25]. Leakage inductances effect the drain-source voltage of the transistor, the transistor is turned on with an input source voltage that is less than the output voltage applied during hard switching, when $L_{S(TV1)} = L_{S(L1)} \leq 1$ nH.

A transistor loss is determined as (8):

$$P_{SW(on)hard} = P_{cond} + P_{SW(on)} + P_{SW(off)} \qquad (8)$$

Where P_{cond} – a transistor conduction losses, $P_{SW\,(on)}$ – a transistor turns on losses, $P_{SW\,(off)}$ – a transistor turns off losses. A transistor turns on losses with hard switching is determined as (9):

$$P_{SW(on)hard} = 0.5 \cdot I_{S(\min)} \cdot U_{out} \cdot (t_r + t_{ir}) \cdot f_{sw} \tag{9}$$

where if $\Delta I_{L1.1} << I_{load}$ then $IS_{(min)} = I_{load}$.

As displayed earlier, the value of the leakage inductance $L_{S(L1)}$ determines the value of the transistor turn on losses in this converter. At the turn on stage the transistor current waveform is determined not only by leakage inductances, but also by transistor parasitic parameters and a gate resistance. Taking account of these factors' transistor turn on losses with soft switching is determined as (10):

$$P_{SW(on)soft} = 0.05 \cdot \frac{U_{in}^2}{L_{S(L1)}+L_{S(TV1)}} \cdot t_r^2 \cdot f_{sw} \tag{10}$$

The value of the loss parameter K_P can be determined from in (9) and (10). K_P determines the proportion of soft switching losses from hard switching losses $K_P = P_{SW\,(on)soft} / P_{SW\,(on)hard}$. Hard switching waveforms shown in Figure 4(a). To obtain the waveforms shown in Figure 4(b), the condition must be satisfied $t_1 > t_r$, and for the normal operation of the converter, that is shown in Figure 1 the next condition must be satisfied $t_1 < D \cdot T_S$ (D is a minimum value for hard switching). As a result, the duration of the first stage should be in the time range $t_r < t_1 < D \cdot T_S$. Based on this, the loss parameter K_P is also limited based on the time range.
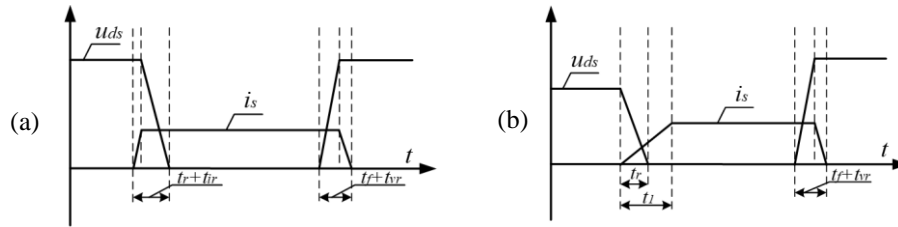

Figure 4. Theoretical (a) hard switching and (b) soft switching (turn on) waveforms

The loss parameter K_P is determined from (9) and (10):

$$K_P = 0.1 \cdot \frac{U_{in}^2}{(L_{S(L1)}+L_{S(TV1)}) \cdot P_{out}} \cdot \frac{t_r^2}{t_r+t_{ir}} \tag{11}$$

In (1) and (11) determine the limit values of the parameter:

$$K_{P(max)} = 0.1 \cdot K_{POWER} \cdot \frac{t_r}{t_r+t_{ir}} \tag{12}$$

where $K_{POWER} = \frac{U_{in}^2}{(L_{S(L1)}+L_{S(TV1)}) \cdot P_{out}}$.

$$K_{P(min)} = 0.1 \cdot K_{POWER} \cdot \frac{t_r^2}{(t_r+t_{ir}) \cdot D \cdot T_S} \tag{13}$$

The necessary value $L_{S(L1)}$ to reduce turn on losses by $1-K_P$ is determined from (11).

$$L_{S(L1)} = 0.1 \cdot \frac{U_{in}^2}{K_P \cdot P_{out}} \cdot \frac{t_r^2}{t_r+t_{ir}} - L_{S(VT1)} \tag{14}$$

Therefore, a loss value assignment determines a necessary leakage inductance value $L_{S(L1)}$.

Since a minimum transistor current value across the entire input voltage range is a constant (without current ripples), the transistor drain-source voltage (for soft switching this is the input voltage) determines a turn on losses value. Based on that the maximum turn on losses operation is the minimum input voltage operation. The calculation of the necessary leakage inductance value should base on the worst operation. Then (14) become:

$$L_{S(L1)} = 0.1 \cdot \frac{U_{in(max)}^2}{K_P \cdot P_{out}} \cdot \frac{t_r^2}{t_r+t_{ir}} - L_{S(VT1)} \tag{15}$$

From in (10) and (15) follows that at the maximum input voltage the turn on losses is determined by a given loss parameter. In the rest of the operating range of input voltages, losses are reduced by an amount exceeding K_P, because the transistor turns on with lower voltages.

4. RESULTS AND DISCUSSION

Simulation modeling of the converter to confirm the correctness of the obtained equations was performed in the software package PSIM 2022.1. The simulation model of the converter is shown in Figure 5. The static and dynamic parameters of transistors VT_1 and VT_2 were taken into account in the model to estimate switching losses (these are level-2 MOSFET models of transistor). The parameters of the IRFP250PBF transistor (n-channel MOSFET) were used in the simulation.

The input DC voltage source (U_{in}) is model of battery bank; the output DC-bus represented by a resistor (R_{out}) with resistance (R_{out}) with resistance $R_{out} = \frac{U_{out}^2}{P_{out}}$. Voltage-controlled voltage sources are simplified driver model, converts a logical signal into an analog one, also gate resistances are connected. Additional control-to-power interface block allows a control circuit quantity to be passed unchanged to the power circuit. Single-phase transformer model includes magnetizing inductance. The simulation was performed with a fixed step of 0.1 ns. The parameters of the simulation model are given in Table 1. The value of L_1 was calculated using (5). The value C_1 was selected in accordance with the impedance of the input source.
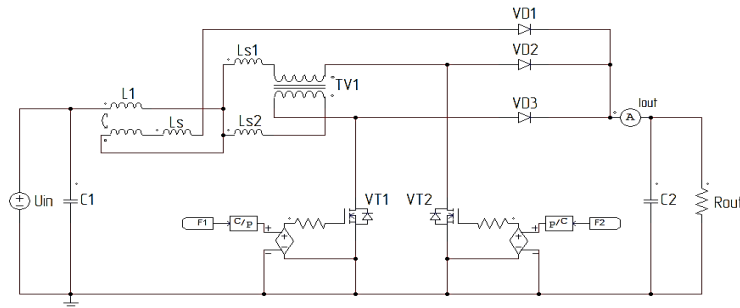

Figure 5. Simulation model

Table 1. The parameters of model

Parameter	Value	Parameter	Value
Input voltage range	55-95 V	Switching frequency	150 kHz
Output voltage	100 V	Coupled-inductors inductance	14.3 uH
Output voltage ripple	0.5 V	Input capacitor capacitance	6 uF
Output power	1 kW		

The value of the leakage inductance of the transformer $L_{S(TV1)}$ was adopted equal to 1 nH. Values of the leakage inductance of coupled-inductors $L_{S(L1)}$ and output capacitor C_2 were calculated based on the set value K_P in accordance with in (6) and (7). Values of K_P were selected in accordance with conditions (12) and (13) in paragraph 3. The simulation was performed for three conditions: i) $K_P = 1$, $L_{S(L1)} = 1$ nH, $C_2 = 1.7$ uF; ii) $K_P = 0.050$, $L_{S(L1)} = 0.36$ uH, $C_2 = 7.1$ uF; and iii) $K_P = 0.025$, $L_{S(L1)} = 0.71$ uH, $C_2 = 13.9$ uF. The 1st condition corresponds to the hard switching of transistors, stages 1, 3, 5 and 7 (Figure 2) are absent. C_2 was selected according to the output current ripples. The 2nd and 3rd conditions correspond to zero-current turn on of transistors.

At a given inductance the maximum rms value of the current of the primary winding is 18.6 A ($U_{in} = 55$ V), the current of the secondary winding is maximum at $U_{in} = 95$ V and is 9.7 A. The amplitude of the transistor current is maximum at $U_{in} = 71$ V and is 10.5 A. The maximum average value of the diode current is 9.5 A (VD_1) at $U_{in} = 55$ V and 4.1 A (VD_2, VD_3) at $U_{in} = 95$ V. The maximum rms value of the input capacitor current is 4.3 A at $U_{in} = 55$ V. The rms values of the output capacitor currents are maximum at $U_{in} = 95$ V and can be theoretically calculated by (8). For the considered values of the leakage inductance are: 0.32 A ($L_{S(L1)} = 1$ nH); 1.42 A ($L_{S(L1)} = 0.36$ uH) and 1.97 A ($L_{S(L1)} = 0.71$ uH). The value of the leakage inductance does not affect the current loading of the elements, except for the output capacitor. The element base should be selected according to the maximum load. Figure 6(a) shows the transistor VT_1 drain currents and the drain-source voltages waveforms for three conditions, the current scale is increased by 5 times. Figure 6(b) shows the output capacitor C_2 current waveforms.
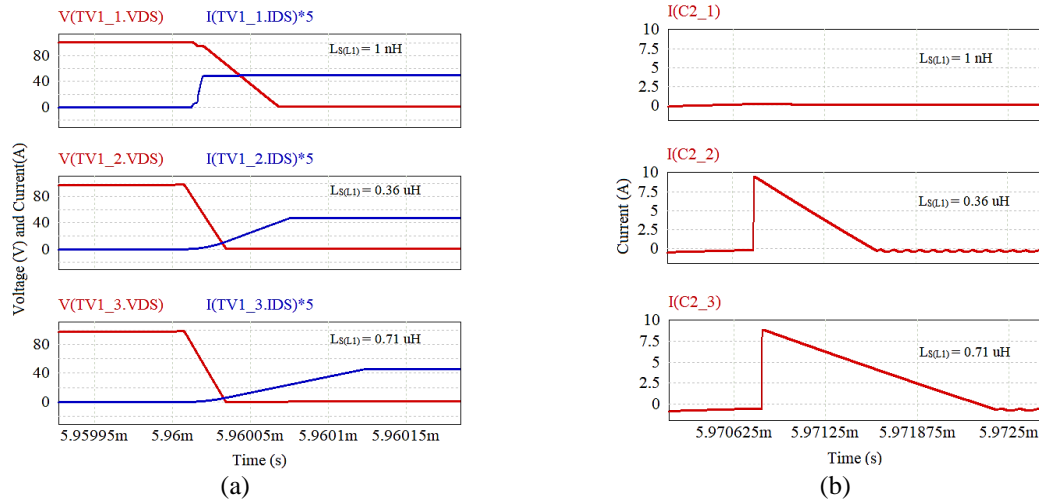
Figure 6. Waveforms of (a) switch turn on current/voltage and (b) output capacitor current

Figure 7 shows output waveforms of the converter (load current and voltage), Figure 7(a) at U_{in} =55 V, Figure 7(b) at U_{in} =95 V for different leakage inductance (3 conditions). The duration of the switching intervals does not affect the ripple of current and voltage. The average value of the load current for all cases is 10 A, the average value of the output voltage is 100 V, voltage ripples do not exceed the set value.
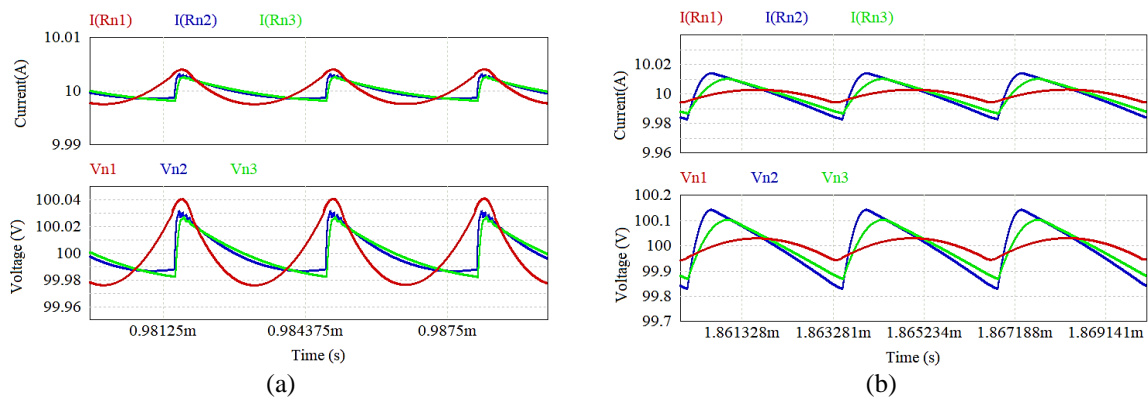

Figure 7. Waveforms of (a) output currents and (b) output voltages for different $L_{S(L1)}$ values

The Figure 8 shows dependence turn on switching losses from input voltage. Figure 8(a) shows hard switching losses, for this situation the transistor turns on with the output voltage of the converter, so switching losses do not depend on input voltage directly. The graph is not straight, because the transistor current ripples depend on input voltage and this is changing the turn on current value in the input voltage range. The theoretical graph was obtained from (9). Theoretical results correspond with the simulation results with engineering accuracy. Figure 8(b) shows soft switching losses for conditions 2 and 3. The theoretical graph was obtained from (10). Theoretical results correspond with the simulation results with engineering accuracy. Losses at the maximum input voltage was reduced in accordance with the specified loss parameter K_P, at the minimum voltage it was reduced by $0.1 \cdot K_P$.

The Figure 9(a) shows dependence durations of stages 1 from input voltage. The Figure 9(b) shows dependence durations of stages 3 from input voltage. Theoretical graphs were obtained from (1) and (3). Theoretical results correspond to simulation results, which confirms the correctness of the obtained equations. The simulation results confirm the correctness of the developed method for setting the turn on switching loss. A negative factor of this method is the deterioration of the output voltage quality and an increase of the output capacitor current stress. The choice of the output capacitor in accordance with (6) allows you to ensure the specified quality of the output voltage. So, in the designing this converter, two factors must be taken into account: loss reduction and deterioration of the output voltage quality. The choice of optimal values should be

made based on the specific requirements for the device being developed. It should be noted that the value of the leakage inductance of coupled-inductors is determined by the results of the design. Therefore, the use of special design methods is necessary to obtain the necessary leakage inductance.
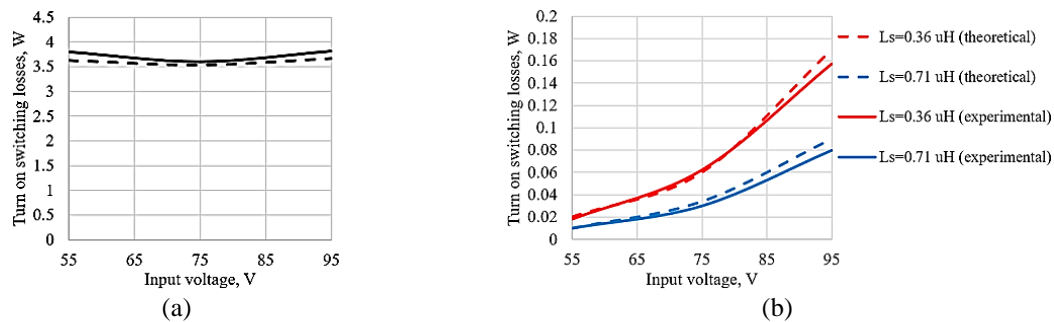

Figure 8. Turn on switching losses (a) hard switching and (b) soft switching versus input voltage
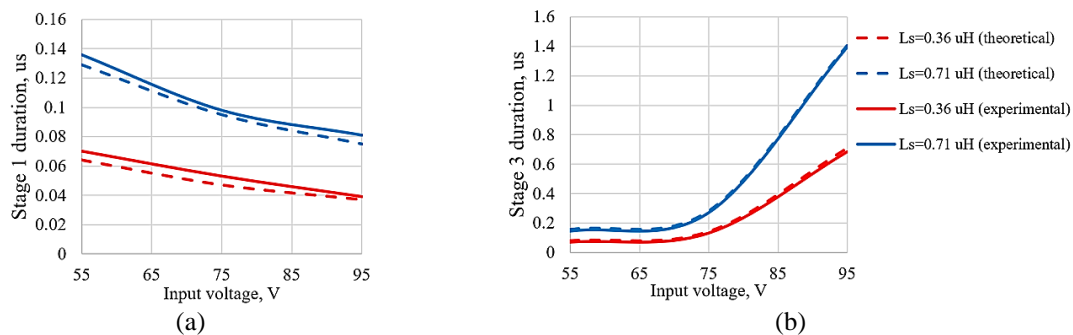

Figure 9. Durations of (a) 1 stage and (b) 3 stages versus input voltage

5.   CONCLUSION

A method of determining a level of turn on switching losses of transistors of the Weinberg converter was presented in this paper. The basis of the method consists in the providing the leakage inductance of coupled-inductors calculated based on the required loss level. The method of calculating the necessary parameters for the selection of the output capacitor, taking into account the negative influence of leakage inductances, was also given. The developed method requires optimization of the loss parameter K_P for the requirements of a specific system. With an increase in the loss parameter K_P, and consequently an increase in efficiency, the weight of the system increases due to the larger capacity of the output capacitor. The correctness of the obtained equations was supported by the results of simulation modeling, the model took into account the static and dynamic parameters of the transistor.

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