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Novel complementary Sziklai pair based high gain low noise small-signal amplifiers

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ABSTRACT

A new paired configuration of opposite polarity BJTs, the "complementary Sziklai pair" is introduced in the series of multi-BJT-based devices like Darlington and Sziklai pair, and its viability is tested in small-signal common emitter (CE) and common collector (CC) amplifier configurations. The Darlington and Sziklai both face the problem of poor frequency response at a higher frequency which is addressed by the proposed configuration. The proposed pair with CE amplifier holds class-A amplification property with a high voltage gain of 200.05, a high current gain of 11.62, wider bandwidth of 1.64 MHz, and a low total harmonic distortion (THD) of 1.29E-6%, hence supports the potential of wide applicability in analog communication. Similarly, the proposed pair with CC configuration produces approximately a unit current gain of 0.99 with wider bandwidth of 1.90 MHz and low THD of 1.76E-6%, therefore it can be used as a current buffer in a generalized current follower circuit. Conclusively, the device structure of this new BJT pair may be considered the third consecutive member of the series of Darlington pair and Sziklai pair. The layout of the proposed CE and CC amplifier occupy small areas of 158.30 μm^2 (10.23×15.47 μm) and 141.16 μm^2 (10.20×13.84 μm) respectively in 180 nm process technology.

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1. INTRODUCTION

A new topology has been introduced about BJT configuration as a device having the potential to be used in multiple applications requiring high gain with wide bandwidth [1]. Distinct from the Darlington and Sziklai pair, a new paired unit of opposite polarity BJT is proposed and its feasibility is examined on small-signal CE and CC amplifier circuits [2]. In the electronics industry, the Darlington pair is a popular device for audio range small-signal and power amplifiers whereas the Sziklai pair (also known as complementary Darlington pair) with opposite polarity BJTs is a suitable candidate for power amplifiers [3]. The use of the Sziklai pair in small-signal amplifiers is still under the phase of research and investigations [4]. Apart from other parametric features, the current gain factor of both the paired devices is approximated to $\beta_1.\beta_2$ (the product of independent current gains of constituent BJTs). By virtue of BJT's positions, this paired unit is named a 'complementary Sziklai pair'. The present discussion covers the modeling of this new BJT pair under a common emitter (CE) and emitter follower/common collector (CC) biasing environment [5].

It is to note that the Darlington pair accommodates matched BJTs of similar polarity with the emitter of the first feeding the base of second and the collector of both BJTs share the same current whereas the assembly of Sziklai pair holds BJTs of opposite polarity with collector of the first feeds the base of second

and emitter of first BJT joins the collector of second [6]. However, in the novel device structure of 'complementary Sziklai pair', collector of first BJT feeds the base of the second BJT of opposite polarity and the emitter of first BJT joins the emitter of second. The schematic structure of the proposed BJT pair is depicted in Figure 1.

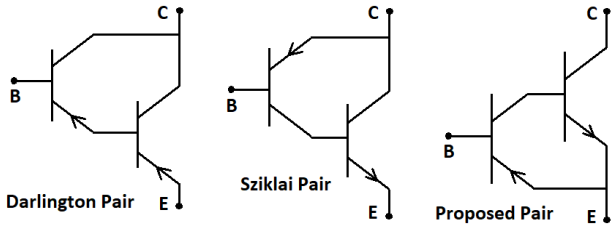


Figure 1. Schematic structure of Darlington pair, Sziklai pair, and proposed BJT pair

Various works have been reported with OTA based CMOS transconductance amplifier but the design approach for BJT based high gain amplifiers are limited to Darlington and Sziklai pairs which suffers performance degradation at higher frequencies. To cope with this problem, an adaptive biasing technique is proposed in [7] for enhanced operation speed of class AB CMOS based amplifier design. A 65 nm CMOS OTA based High gain; high speed folded cascode amplifier suitable for analog communication is proposed in [8]. Another approach for extended bandwidth in OTA based CMOS amplifiers is inclusion of very high speed modified regulated cascade circuit using transimpedance amplifier which supports 10 Gbps suitable for high-speed optical communication [9]. Another approach of low power CMOS OTA is the reduction of operating voltage by employing bulk driven (BD) CMOS [10]. Although these CMOS based amplifiers offer power reduction to a great extent with increased area saving; still BJT based amplifier carry multiple advantages of designs especially in high current and high power gain applications. The CMOS based technology has almost blew away the analog based circuits but the increased noise at higher frequencies limits its use in many applications.

This paper proposes and investigates a novel BJT based structure "complementary Sziklai pair"; which could be a breakthrough in the series of multi BJT based high gain configurations. The comparative study with respect to latest CMOS based analog and digital amplifiers show very promising results. Rather than just the device characteristics study, this paper covers the complete study by evaluating the performance of proposed device in the applied circuit. It is to note that amplifier performance is compared with the circuit of NPN Sziklai pair and PNP Sziklai pair taken from [11] and [12] respectively.

The rest of this paper is organized as follows: i) Section 2 discusses the circuit description part; ii) Results and discussion part is discussed in section 3 which includes performance, layout, post-layout simulation, plots of various performance parameters and performance summary and comparison of the proposed amplifiers with recently reported amplifiers; and iii) Finally, section 4 concludes the paper highlighting major contribution and main findings of the proposed amplifiers.

2. CIRCUIT DESCRIPTION

Circuit simulation of the proposed pair of opposite polarity BJTs in small-signal CE and CC amplifier is done using cadence virtuoso tool. Figure 2(a) depicts the schematic of proposed pair in CE amplifier whereas Figure 2(b) shows the schematic of proposed pair in CC amplifier [13]. Lateral types of BJTs (npn BJT and pnp BJT) are extracted from analog (spectre) foundry under bipolar.net file available at GPDK 180 nm technology (where GPDK stands for generic process device kits). Object properties of both lateral types BJTs are-emitter width = 0.6 nm, area = 0.36 nm^2, and multiplier = 1 [14].

The proposed topology is being studied using two different modes of operations namely, common emitter (CE) and common collector (CC). Due to the fact that both proposed amplifiers demonstrate innovative BJT pairs, parameters relating to them are shown in tabular form [15]. To verify the proposed amplifiers, post-layout simulation and small-signal AC analysis are also carried out. Comparisons among the proposed amplifier, PNP Sziklai, NPN Sziklai, and recently reported amplifiers are the key studies that demonstrate its applicability in the audio range small-signal amplifier [16].

Proposed pair with CE and CC amplifier uses-15 V DC power supply under voltage divider biasing. With CE amplifier, proposed BJT pair uses AC input sin wave of 1 V magnitude and 1 mV amplitude at 1 KHz frequency but produces distortion less output for 10 μV-1 mV range of AC input wave at 1 KHz

frequency whereas this pair with CC amplifier uses AC input sin wave of 1 V magnitude and 10 mV amplitude at 1 KHz frequency and produces fair response for 1 µV-30 mV range of AC input wave at 1 KHz frequency. Table 1 lists out the model parameters of the proposed BJTs used in designing the amplifiers.

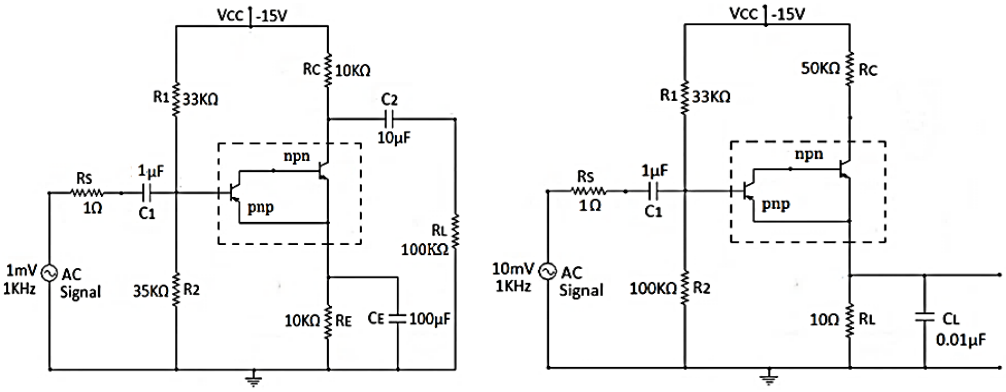


Figure 2. Proposed BJT pair in (a) CE amplifier and (b) CC amplifier

Table 1. Model parameters of the proposed pair with CE and CC amplifiers

Model parameters	BJT models of cadence at 180 nm technology (NPN BJT)	(PNP BJT)
IS (p-n saturation current)	3.26E-16	3.28E-16
BF (ideal maximum forward beta)	100	35
BR (ideal maximum reverse beta)	6	6
IKr (corner for reverse bate high-current roll-off)	100 m	100 m
Vje (base-emitter built-in potential)	0.7	0.7
Cje (base-emitter zero-bias p-n capacitance)	1E-12	0.7E-12
Fc (forward-bias depletion capacitor coefficient)	0.5	0.5
Cjc (base-collector zero-bias p-n capacitance)	0.7E-12	1E-12
Itf (transit-time dependency on I_C)	0.03	0.03
Vtf (transit-time dependency on V_{bc})	7	7
Xtf (transit-time base dependency coefficient)	2	2
RC (collector ohmic resistance)	1	1
TF (ideal forward transit time)	25E-12	25E-12
TR (ideal reverse transit time)	200E-12	200E-12
NC (base-collector leakage emission coefficient)	2	2

3. RESULTS AND DISCUSSION

3.1. Performance

Table 2 represents the performance parameters of the proposed pair with CE and CC amplifier with the aid of cadence virtuoso tool at room temperature. It is also clear that proposed pair with CE amplifier produces higher amplifier voltage gain, higher amplifier current gain at the expense of narrower bandwidth than CC amplifier [17]. Apart from this, proposed pair with CE and CC amplifier also consumes very low amount of power in mW range. In addition, total power consumption can be further reduced to µW range by reducing supply voltage, at the cost of decreased voltage gain, current gain and bandwidth [18]. It is also found that total harmonic distortion (THD) of CE amplifier is lower than CC amplifier, however range of operation of CC amplifier (1 µV-30 mV) is higher than CE amplifier (10 µV-1 mV). Moreover, unity gain bandwidth and phase margin of the CC amplifier can't be computed because voltage gain is found to be less than unity.

Refer Table 2, proposed pair with CE amplifier holds class-A amplification property with higher voltage and current gain along with higher power gain, thus it may be used as voltage-cum-power amplifier for various analog communication applications [19], [20]. Similarly, this pair with CC amplifier generates unity current gain with wider bandwidth than CE amplifier, therefore it may be used in impedance matching and current buffer amplifier [21]. Frequency response curve of CC amplifier also looks like low pass filter with lower cut-off frequency of 1.59 MHz. Conclusively, proposed pair with both amplifiers exhibit better frequency response than small-signal Sziklai and Darlington pair amplifiers of this class [22]. Proposed pair with CE and CC amplifiers also eliminates the poor response problem of small-signal Darlington pair

amplifiers at higher frequency and narrow bandwidth response problem of PNP small-signal Sziklai pair amplifiers. In this way, proposed BJT pair could be a better replacement of small-signal Sziklai and Darlington pair amplifiers in audio range amplifiers [23].

Table 2. Performance parameters of the proposed pair with CE and CC amplifiers

Performance Parameters	Proposed pair with CE amplifier	Proposed pair with CC amplifier
Amplifier voltage gain	200.05	0.13
Upper cut off frequency	1.64 MHz	1.90 MHz
Lower cut off frequency	58.72 Hz	2.26 KHz
Band-width	1.64 MHz	1.90 MHz
Unity gain band-width	459.66 MHz	Immeasurable
Amplifier current gain	11.62	0.99
Upper cut off frequency	102.28 KHz	1.59 MHz
Lower cut off frequency	12.72 Hz	--
Band-width	102.26 KHz	--
Device voltage gain	200.14	0.14
Device current gain	194.22	0.99
Power gain	33.66 dB-Watt	-8.57 dB-Watt
Output phase difference	-176.44°	+65.86°
Phase margin	164.59°	Immeasurable
Total harmonic distortion	1.29E-6%	1.76E-6%
Total power consumption	13.60 mW	10.63 mW
Input signal voltage	1mV (1 KHz)	10 mV (1 KHz)
Range of Input Signal Voltage	10μV-1mV (at 1KHz)	1μV-30 mV (at 1 KHz)
Slew rate of output voltage	0.0092 V/us	Immeasurable
Current across Source Resistance	259.67 nA	59.33 uA
Input referred noise	2.15 nV/$\sqrt{Hz}$	7.26 nV/$\sqrt{Hz}$
Output referred noise	430.43 nV/$\sqrt{Hz}$	0.40 nV/$\sqrt{Hz}$
Current across Load Resistance	1.68 uA	-652.21 uA
Voltage across source resistance	1 mV	10 mV
Voltage across load resistance	185.04 mV	-6.52 mV

Figure 3(a) shows the voltage gain of CE amplifier and Figure 3(b) shows the current gain of CE amplifier. Similarly, Figure 4(a) exhibits the voltage gain and Figure 4(b) shows the current gain of CC amplifier. The response curves show better performance than Sziklai and Darlington pair small-signal amplifier of this class [24]. Frequency response curve of this amplifier produces undistorted output than small-signal Sziklai and Darlington pair of same class. In addition, total power consumption of CE amplifier and CC amplifier is very low i.e., 13.60 mW and 10.63 mW respectively. Both amplifiers dissipate very low amount of power as compared to Sziklai and Darlington pair small-signal amplifiers. It can be further reduced by reducing DC supply voltage within permissible limits without disturbing the biasing of the constituent transistors.

Frequency response of the proposed BJT pair with CE amplifier in the permissible frequency band looks as fair as other CE amplifiers of this class with class-A amplification pattern. However, like Darlington pair, the response becomes mildly poor beyond higher cut-off frequency, and with CC amplifier almost resembles with Darlington pair amplifier of this class [25]. It is to note that small-signal CC with Sziklai pair is yet to be authentically announced but the proposed BJT pair proves its applicability in CC configuration.

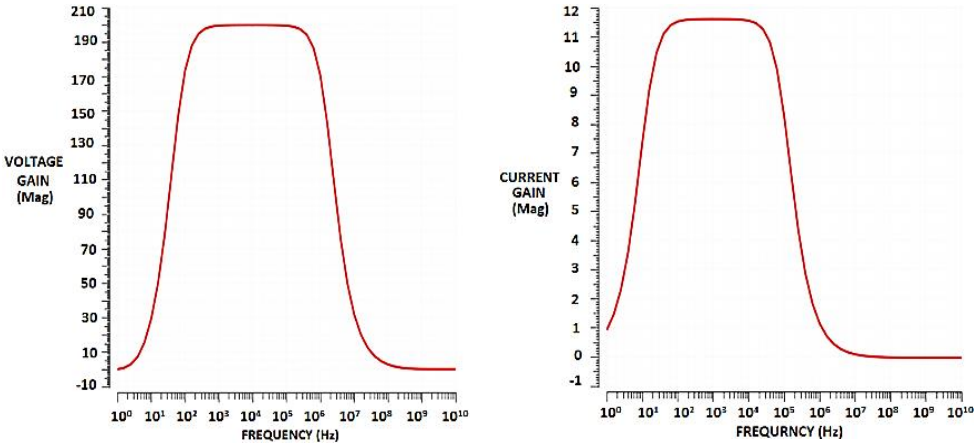
Proposed complementary Sziklai pair in CE amplifier configuration shows it's applicability in high gain wide band frequency applications and behaves as voltage cum power amplifier having better response than Darlington and Sziklai pair amplifiers of this class. In CC amplifier configuration the proposed device generates unit current gain and low voltage gain therefore this amplifier configuration acts as a current buffer and low pass filter circuit [20]–[25]. Based on the equivalent circuits (not shown), the voltage gain in (1) for CE amplifier may be estimated as (1).

$$A_{VGA-CE} = \frac{-\beta_1\beta_2 R_L}{r_{\pi 1}(1-\frac{R_C}{r_{o2}})(1+\frac{r_{\pi 2}}{r_{o1}})} \quad (1)$$

Similarly, voltage gain in (2) for CC amplifier may be approximated as (2).

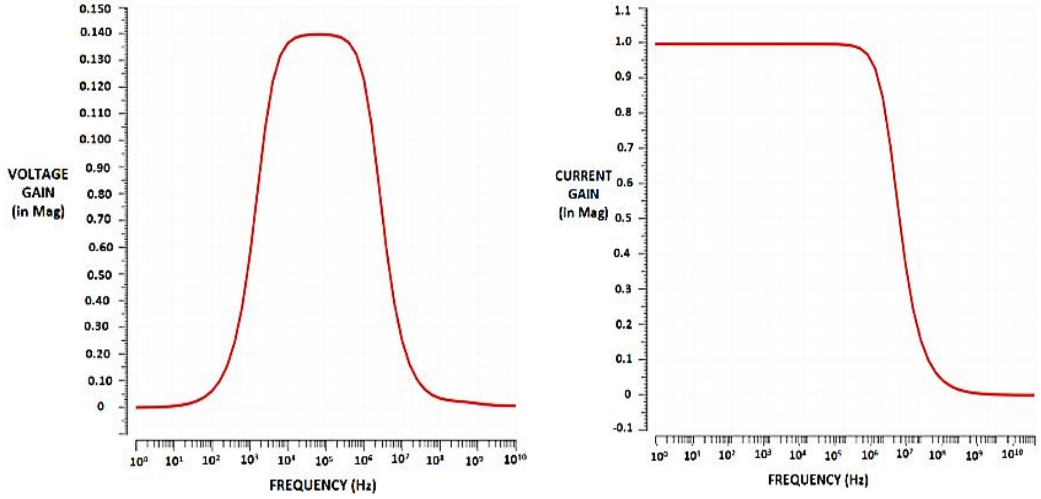
$$A_{VGA-CC} = \frac{\beta_1\beta_2(2R_C-r_{o2})}{r_{\pi 1}(1+\frac{r_{\pi 2}}{r_{o1}})} \quad (2)$$

Respective expressions advocate that the current gain factor of the proposed paired unit to be $\beta_1.\beta_2$.



(a) (b)

Figure 3. Response curve of CE amplifier of (a) voltage gain and (b) current gain

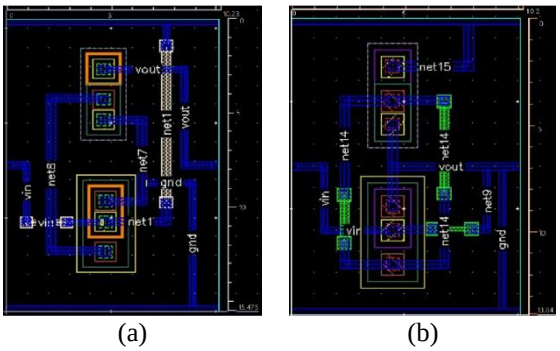


(a) (b)

Figure 4. Response curve of CC amplifier of (a) voltage gain and (b) current gain

3.2. Layout of the proposed designs

Figures 5(a) and 5(b) shows the layout of CE amplifier and CC amplifier using cadence virtuoso tool at 180nm technology. In Figures 5(a) and 5(b), upper cell indicates NPN transistor whereas lower cell indicates PNP transistor. The entire boundary surrounded the layout is known as PR (placement and routing) boundary. Layout design of CE and CC amplifier occupies a small area of 158.30 square unit (10.23×15.47 µm) and 141.16 square unit (10.20×13.84 µm) respectively.



(a) (b)

Figure 5. Layout of (a) CE amplifier and (b) CC amplifier

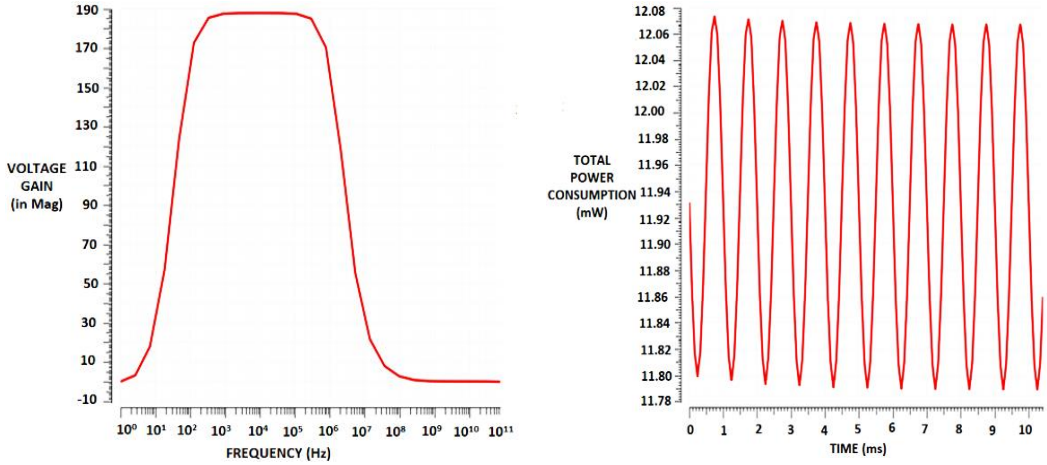
3.3. Post-layout simulation

Table 3 shows the performance parameters of CE amplifier in pre and post layout simulation. Minor variation in post-layout simulation results is reported in voltage gain (6% decrease), bandwidth (1.03% increase) and power consumption (13.28% increase). Thus, it can be inferred that the percentage variation of the performance parameters before and after layout are within the acceptable limits, hence it verifies the design of CE amplifier in 180 nm technology. Figures 6(a) and 6(b) shows the voltage gain and total power consumption of CE amplifier in post layout simulation.

Similarly, Table 4 enlists performance parameters of CC amplifier before and after layout whereas Figures 7(a) and 7(b) shows voltage gain and total power consumption of CC amplifier in post-layout simulation. Similar to CE amplifier, CC amplifier also produces nearly the same pre and post layout simulation parameters which validate the proposed design at 180 nm technology.

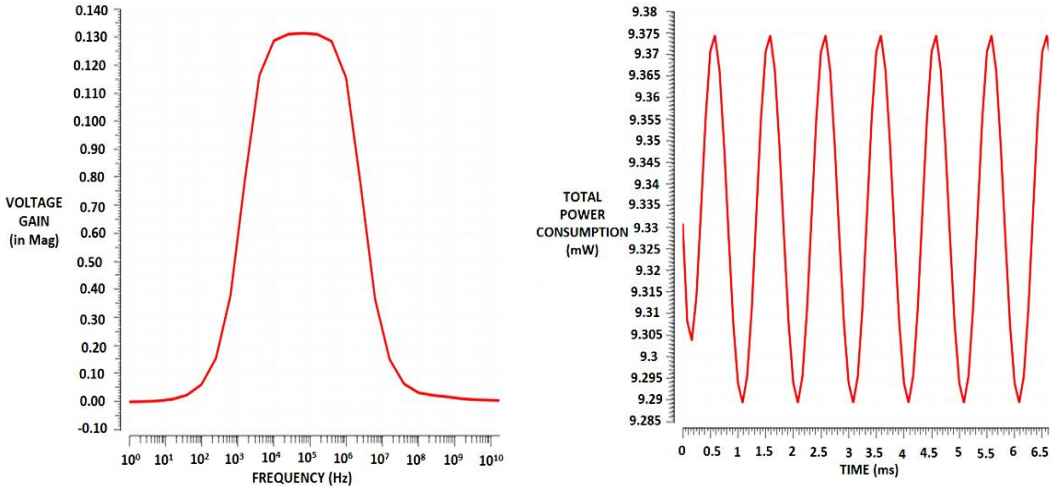
Table 3. Performance parameters of CE amplifier before and after layout

Performance parameters	Before layout (pre-layout simulation)	After layout (post-layout simulation)
Voltage gain, A_{VG}	200.05	188.03
Lower cut-off frequency, F_L	58.72 Hz	61.39 Hz
Upper cut-off frequency, F_H	1.64 MHz	1.66 MHz
Bandwidth, B_W	1.64 MHz	1.66 MHz
Total power consumption, P_W	13.60 mW	11.79 mW



(a) (b)

Figure 6. Post-layout simulation of CE amplifier of (a) voltage gain and (b) total power consumption



(a) (b)

Figure 7. Post-layout simulation results of CC amplifier of (a) voltage gain and (b) total power consumption

Table 4. Performance parameters of CC amplifier before and after layout

Performance parameters	Before layout (pre-layout simulation)	After layout (post-layout simulation)
Voltage gain, A_{VG}	0.13	0.13
Lower cut-off frequency, F_L	2.26 KHz	2.45 KHz
Upper cut-off frequency, F_H	1.90 MHz	1.90 MHz
Bandwidth, B_W	1.90 MHz	1.90 MHz
Total power consumption, P_W	10.63 mW	9.28 mW

3.4. Plots of various performance parameters

Figures 8(a), 8(b), and 8(c) shows the voltage gain, band width and power consumption of CE and CC amplifier in pre and post layout simulation. Figures 9(a), 9(b), and 9(c) shows the voltage gain, total power consumption, and THD of complementary Sziklai pair, NPN Sziklai pair, and PNP Sziklai pair in CE configuration. It is clear that complementary Sziklai pair produces low THD with low power consumption than NPN Sziklai and PNP Sziklai. However, its voltage gain is greater than NPN Sziklai but lower than PNP Sziklai [24].

Figure 10(a) shows the voltage gain, Figure 10(b) shows the THD, and Figure 10(c) shows the output referred noise of complementary Sziklai pair, NPN Sziklai pair, and PNP Sziklai pair in CC amplifier configuration respectively. It is clear that THD and output referred noise of complementary Sziklai pair is lower than PNP and NPN Sziklai pair. However, bandwidth of complementary Sziklai pair is higher than NPN Sziklai pair and lower than PNP Sziklai pair. This poses strong justification for this amplifier as a replacement of PNP and NPN Sziklai in "low-power low-noise wideband amplifiers".

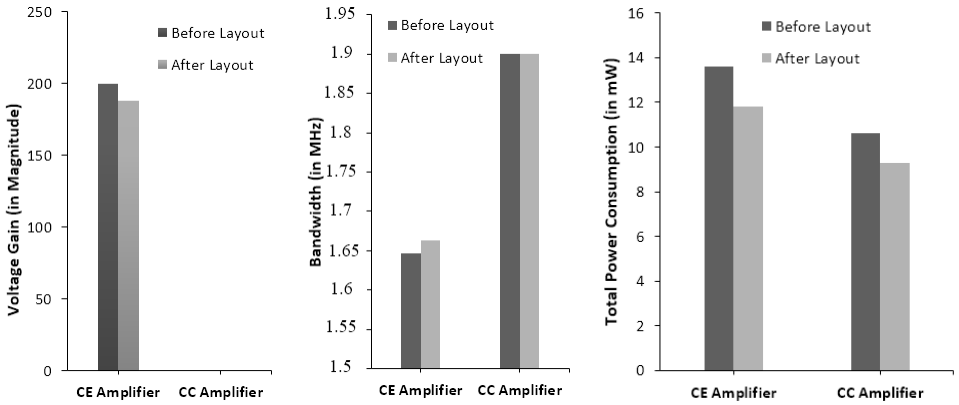


Figure 8. Plots before and after layout of (a) voltage gain, (b) bandwidth, and (c) total power consumption

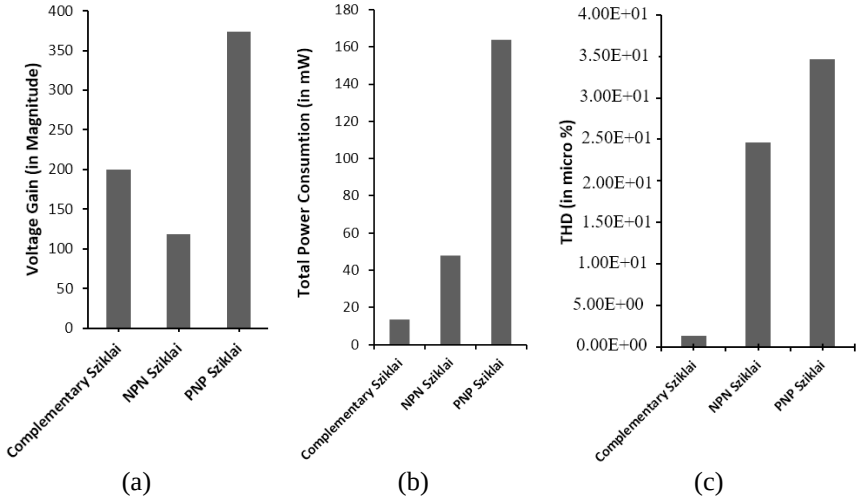
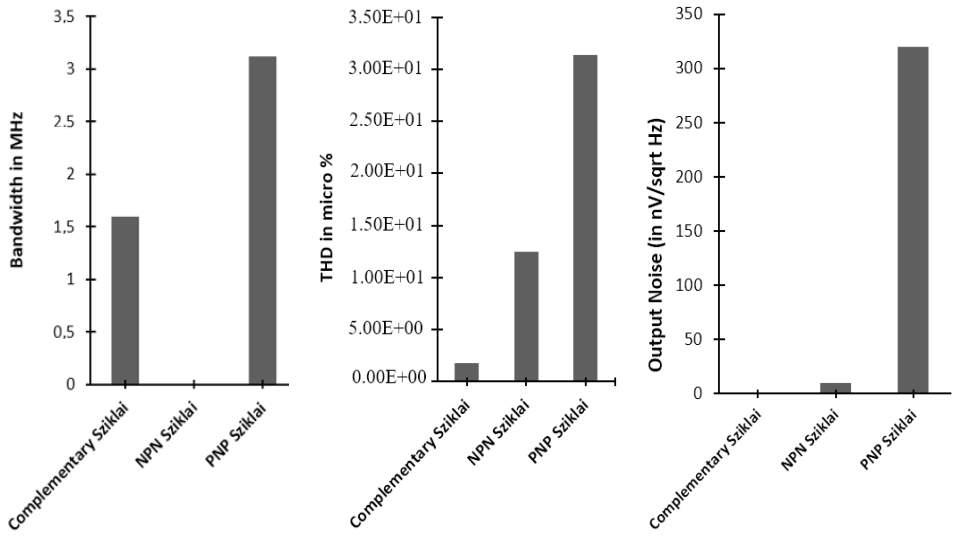


Figure 9. Comparison plots of CE amplifier in complementary Sziklai pair, NPN Sziklai, and PNP Sziklai pair with respect to (a) voltage gain, (b) total power consumption, and (c) THD



(a) (b) (c)

Figure 10. Comparison plots of CC amplifier in complementary Sziklai pair, NPN Sziklai, and PNP Sziklai pair with respect to (a) bandwidth, (b) THD, and (c) output referred noise

3.5. Performance summary and comparison

Table 5 shows the performance comparison of the proposed complementary Sziklai pair-based amplifiers with other recently reported amplifiers in past five years having high gain and wide bandwidth. The selected reference in give performance criteria is majorly based on CMOS technology and show that there is a major void of BJT based amplifier design considering its excellent noise performance in high frequency range. This paper is an effort to investigate a novel BJT based structure and compare it with the latest reported CMOS based amplifiers. The proposed device-based amplifiers show very competitive performance in terms of high gain, low noise, low power consumption and low THD than the other amplifiers [21]–[25].

Table 5. Performance summary and comparison

References	[1]	[2]	[3]	[4]	[5]	[6]	[7]	[8]	[9]	[10]	This work		Unit
Design strategy	Digital CM-OS	Analog CM-OS	Analog CM-OS	Digital CM-OS	Analog CM-OS	Digital CM-OS	Analog CM-OS	Analog CM-OS	Analog CM-OS	Analog CM-OS	CE Amplifier	CC Amplifier	----
Year	2022	2021	2020	2019	2018	2021	2019	2020	2021	2022	---	----	----
Technology	180	28	180	180	65	180	180	180	180	65	180	180	nm
Supply voltage	0.4	1.0	±0.45	1.8	1.2	0.8	1.8	0.3	0.6	1.2	-15	-15	Volts
Area	0.02	0.04	---	0.05	0.05	1.42	0.21	0.72	1.02	1.17	0.000158	0.000140	mm^2
Voltage gain	35	39.5	30	98	44	30	---	51	73	22.8	46.02	-17.14	dB
Band-width	0.000001	0.001	9.53	---	1000	---	10000	0.00074	---	10600	1.64	1.90	MHz
Unity gain band-width	---	---	---	21	---	0.000518	---	---	0.015	---	459.66	---	MHz
Current gain	---	---	---	---	---	---	---	---	---	---	21.30	-0.00869	dB
Power gain	---	---	---	---	---	---	---	---	---	---	33.66	-8.57	dB-Watt
Slew rate	---	---	---	---	---	0.26	---	---	---	---	9.2	---	V/ms
Input referred noise	395	2150	341	250	---	---	0.0307	809	362	---	2.15	7.26	nV/√Hz
Output referred noise	----	----	----	----	----	----	----	----	----	----	13.6	10.6	nV/√Hz
Total power consumption	0.000095	0.00071	0.81	3	6	0.59	10.7	0.0000005	0.0000408	15.5	1.29E-6	1.76E-6	mW
THD	1.8	---	---		---	2.82	---	---	1	---	---	----	%

4. CONCLUSION

Unlike Darlington pair and Sziklai pair, a new paired unit of opposite polarity BJT is introduced and its feasibility is examined on small-signal CE and CC amplifier circuit. Complementary Sziklai pair small-signal amplifier under CE configuration produces high voltage gain, low THD, and consumes very low power. Similarly, this amplifier under CC configuration produces very low output noise along with low THD and low total power consumption. However, NPN Sziklai pair small-signal amplifier under CE and CC configuration produces very high current gain with low output noises.

In the same manner, PNP Sziklai pair small-signal amplifier under CE and CC configurations produces high voltage gain with wider bandwidth. However, this amplifier under CE configuration produces low output noises. Under cadence virtuoso tool, the proposed device pair-based CE amplifier holds class-A amplification property with high voltage and current gains and behaves as voltage cum power amplifier having better frequency response than small-signal Sziklai and Darlington pair amplifiers of this class. These amplifiers can be suitably utilized in high gain wide band applications. Under Spice simulation tool, the CC amplifier with proposed pair (having matched BJTs) acts as perfect current amplifier and voltage buffer amplifier with high current gain and voltage gains approximately equal to unity. However, under Cadence simulation, the CC amplifier with proposed BJT pair acts as a current buffer amplifier with unity current gain. Frequency response of CC amplifier suggests that this amplifier behaves like low pass filter circuit with lower cut-off frequency f_L=1.59685 MHz. Layout of CE and CC amplifier occupies a small area of 158.309 square unit (10.23×15.475 µm) and 141.168 square unit (10.2×13.84 µm) respectively. In addition, post-layout simulation of CE and CC amplifier also verifies the proposed designs in 180 nm technology.

When the DC biasing source is replaced by +15 V and position of BJTs in both the amplifier configurations are swapped under Spice simulation tool, the resultant amplifiers produce the similar result. This unique feature is not received for small-signal Darlington and Sziklai pair amplifiers. This phenomenon is also not seen when the proposed pair with CE and CC amplifiers are implemented in cadence virtuoso simulation tool. Moreover, proposed BJT pair with CE and CC amplifiers consume very low amount of power (in mW), however total power consumption can further be reduced by reducing DC supply voltage. The proposed BJT pair with CE and CC amplifier resolves the problem of narrow bandwidth restriction of PNP small-signal Sziklai pair amplifier and small-signal Darlington pair amplifier at higher frequency.

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REFERENCES

[1] M. Ali, H. F. A. Hamed, and G. A. Fahmy, "Small Group Delay Variation and High Efficiency 3.1–10.6 GHz CMOS Power Amplifier for UWB Systems," *Electronics*, vol. 11, no. 3, p. 328, Jan. 2022, doi: 10.3390/electronics11030328.

[2] L. H. Rodovalho, C. Ramos Rodrigues, and O. Aiello, "Self-Biased and Supply-Voltage Scalable Inverter-Based Operational Transconductance Amplifier with Improved Composite Transistors," *Electronics*, vol. 10, no. 8, p. 935, Apr. 2021, doi: 10.3390/electronics10080935.

[3] L. H. Rodovalho, O. Aiello, and C. R. Rodrigues, "Ultra-Low-Voltage Inverter-Based Operational Transconductance Amplifiers with Voltage Gain Enhancement by Improved Composite Transistors," *Electronics*, vol. 9, no. 9, p. 1410, Sep. 2020, doi: 10.3390/electronics9091410.

[4] X. Chen and Y. Takahashi, "Floating Active Inductor Based Trans-Impedance Amplifier in 0.18 µm CMOS Technology for Optical Applications," *Electronics*, vol. 8, no. 12, p. 1547, Dec. 2019, doi: 10.3390/electronics8121547.

[5] A. Vasjanov and V. Barzdenas, "A Review of Advanced CMOS RF Power Amplifier Architecture Trends for Low Power 5G Wireless Networks," *Electronics*, vol. 7, no. 11, p. 271, Oct. 2018, doi: 10.3390/electronics7110271.

[6] P. Toledo, P. S. Crovetti, H. D. Klimach, F. Musolino, and S. Bampi, "Low-Voltage, Low-Area, nW-Power CMOS Digital-Based Biosignal Amplifier," *IEEE Access*, vol. 10, pp. 44106–44115, 2022, doi: 10.1109/ACCESS.2022.3168603.

[7] X. T. Pham, N. T. Nguyen, V.-N. Nguyen, and J.-W. Lee, "Area and Power-Efficient Capacitively-Coupled Chopper Instrumentation Amplifiers in 28 nm CMOS for Multi-Channel Biosensing Applications," *IEEE Access*, vol. 9, pp. 86773–86785, 2021, doi: 10.1109/ACCESS.2021.3087737.

[8] H. D. Rico-Aniles, J. Ramirez-Angulo, J. M. Rocha-Perez, A. J. Lopez-Martin, and R. G. Carvajal, "Low-Voltage 0.81mW, 1–32 CMOS VGA With 5% Bandwidth Variations and −38dB DC Rejection," *IEEE Access*, vol. 8, pp. 106310–106321, 2020, doi: 10.1109/ACCESS.2020.2999315.

[9] S. M. Anisheh, H. Abbasizadeh, H. Shamsi, C. Dadkhah, and K.-Y. Lee, "98-dB Gain Class-AB OTA With 100 pF Load Capacitor in 180-nm Digital CMOS Process," *IEEE Access*, vol. 7, pp. 17772–17779, 2019, doi: 10.1109/ACCESS.2019.2896089.

[10] L. He, L. Li, X. Wu, and Z. Wang, "A Low-Power Wideband dB-Linear Variable Gain Amplifier With DC-Offset Cancellation for 60-GHz Receiver," *IEEE Access*, vol. 6, pp. 61826–61832, 2018, doi: 10.1109/ACCESS.2018.2875764.

[11] S. N. Shukla, S. S. Arshad, and G. Srivastava, "NPN Sziklai pair small-signal amplifier for high gain low noise submicron voltage recorder," *International Journal of Power Electronics and Drive Systems (IJPEDS)*, vol. 13, no. 1, p. 11, Mar. 2022, doi: 10.11591/ijpeds.v13.i1.pp11-22.

[12] S. Shukla, "New Circuit models of small-signal amplifiers with Darlington pair in Sziklai pair topology," *Journal of Rajasthan Academy of Physical Sciences*, vol. 20, pp. 119–138, 2021.

[13] S. N. Shukla, G. Srivastava, and S. S. Arshad, "Study of Low-Noise Wide-Band Tuned Sziklai Pair Small-Signal Amplifier," in *Research Trends and Challenges in Physical Science Vol. 1*, pp. 1-16, Agus. 2021, doi: 10.9734/bpi/rtcps/v1/4064F.

[14] S. Shukla, P. Soni, N. K. Chaudhary, and G. Srivastava, "Development of Low Frequency Small Signal Amplifier using BJT JFET in Sziklai Pair Topology," *International Journal of Recent Technology and Engineering (IJRTE)*, vol. 9, no. 3, pp. 217–223, Sep. 2020, doi: 10.35940/ijrte.C4365.099320.
[15] S. Shukla, "New small-signal amplifying system with Sziklai pairs in triple-transistor topology," in *2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES)*, Nov. 2016, pp. 463–468, doi: 10.1109/ICAEES.2016.7888089.
[16] P. Saad and R. Hou, "Symmetrical Load Modulated Balanced Power Amplifier With Asymmetrical Output Coupling for Load Modulation Continuum," *IEEE Transactions on Microwave Theory and Techniques*, vol. 70, no. 4, pp. 2315–2327, Apr. 2022, doi: 10.1109/TMTT.2022.3147843.
[17] G. Giustolisi and G. Palumbo, "Design of Three-Stage OTA Based on Settling-Time Requirements Including Large and Small Signal Behavior," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 3, pp. 998–1011, Mar. 2021, doi: 10.1109/TCSI.2020.3044454.
[18] Z. Li, B. Liu, Y. Duan, Z. Wang, Z. Li, and Y. Zhuang, "Flat-High-Gain Design and Noise Optimization in SiGe Low-Noise Amplifier for S–K Band Applications," *Circuits, Systems, and Signal Processing*, vol. 40, no. 6, pp. 2720–2740, Jun. 2021, doi: 10.1007/s00034-020-01616-2.
[19] J. Hu and K. Ma, "Analysis and Design of a Broadband Receiver Front End for 0.1-to-40-GHz Application," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 68, no. 6, pp. 2393–2403, Jun. 2021, doi: 10.1109/TCSI.2021.3064262.
[20] P. Toledo, P. Crovetti, H. Klimach, S. Bampi, O. Aiello, and M. Alioto, "A 300mV-Supply, Sub-nW-Power Digital-Based Operational Transconductance Amplifier," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 9, pp. 3073–3077, Sep. 2021, doi: 10.1109/TCSII.2021.3084243.
[21] N. Lupo, M. Bartolini, P. Pulici, S. Colli, M. Nessi, and E. Bonizzoni, "On the Linearity of BJT-Based Current-Mode DAC Drivers," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 9, pp. 3138–3142, Sep. 2021, doi: 10.1109/TCSII.2021.3093657.
[22] M. Kim and S. Cho, "A Single BJT Bandgap Reference With Frequency Compensation Exploiting Mirror Pole," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 10, pp. 2902–2912, Oct. 2021, doi: 10.1109/JSSC.2021.3093583.
[23] C. Sawigun and S. Thanapitak, "A Compact Sub-μW CMOS ECG Amplifier With 57.5-MΩ Zin, 2.02 NEF, 8.16 PEF, and 83.24-dB CMRR," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 15, no. 3, pp. 549–558, Jun. 2021, doi: 10.1109/TBCAS.2021.3086182.
[24] D. Shukla, S. K. Gupta, V. Bhadauria, and R. Tripathi, "High Gain, Low Noise, Low Voltage, and Low Power Current Mode Up-Conversion Mixer for 5G Application," *IETE Journal of Research*, pp. 1–13, Aug. 2022, doi: 10.1080/03772063.2022.2103039.
[25] M. Saritha *et al.*, "A VLSI design of clock gated technique based ADC lock-in amplifier," *International Journal of System Assurance Engineering and Management*, vol. 13, no. 5, pp. 2743–2750, Oct. 2022, doi: 10.1007/s13198-022-01747-6.

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