Sliding-mode control for boost converters under voltage and load variations

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ABSTRACT

Boost converters are employed in DC motors, switch-mode power supplies, and other applications. Practical implementation difficulties, reliance on variable-frequency units, and delayed dynamic responses to changes in load and voltage are the main drawbacks of different control methods for the boost converter. In this paper, two techniques were proposed with the target of controlling the boost converter to improve the efficiency of the converter's performance. The two techniques used in this paper depended on fixedfrequency mode instead of variable-frequency mode because of the demerits of the latter factor. The first technique is the sliding-mode control for the AC-DC converter to achieve power factor correction and reduce the harmonic ratio significantly while regulating the output voltage. This technique was used for the DC-DC converter to obtain a rapid dynamic response to control sudden or considerable changes in loads or input voltages with a regulated output voltage. Moreover, the two-loop cascade control is the second proposed technique for the DC-DC converter to achieve an excellent dynamic response under step loads or input voltage variations with an excellently regulated output voltage. Re-simulation results validated the proposed design approach and illustrated the proposed controller's robustness and faster response time.

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1. INTRODUCTION

Power converters are used in hybrid electric vehicles, uninterruptible power supplies, and other applications to save energy. Power factor correction (PFC) is needed to make the input current have the same phase as the source voltage. PFC can be done in numerous techniques, such as peak current control and average current control by pulse width modulation. Engineers are interested in the single-stage converter, which has high efficiency for improved PFC in such applications and is simple to construct. PFC boost converters, consisting of a full-bridge diode and a boost converter, are commonly used structures in single-phase stage applications [1]–[3].

Sliding mode control (SMC) is a non-linear control method used in power converters to control variablestructure systems. SMC offers numerous advantages, such as durability under load and source voltage variations, stability, and design flexibility, which could improve power converter performance. Modulation methods used for SMC are either hysteresis modulation or pulse width modulation, which have some critical defects such as variable switching frequency, high noise sensitivity, and difficulty in filter design. Hence, artificial intelligence-based algorithms or fuzzy logic control with SMC were proposed to overcome the demerits of the variable switching frequency. The control guarantees that the output voltage is regulated, and the fast dynamic response of the input and output currents is maintained by a genetic algorithm [4]–[8]. Power converters have many control methods, such as inductor voltage loss integration, inductor current prediction, and state observation. Insensitive control of boost converters solves size, weight, and cost challenges. Another technique is the sliding-mode observer, which feeds the non-linear output estimation error to the observer. Additional methods, such as PI and PID control, can be applied to a system if it is non-linear and time-varying. However, there are some limitations under the significant load variations, but SMC can effectively solve such a non-linearity. SMC is less sensitive to parameter changes and simplifies design procedures [1], [6], [9]–[12]. Due to the variable switching frequency issue, a fixed-frequency operation mode is needed for passive energy storage components such as inductors and capacitors. The integrated sliding-mode control system is based on pulse width modulation, but its steady-state error increases with the decrease in the converter switching frequency. Adaptive, indirect, and integral strategies were proposed to address this shortage. However, the adaptive hysteresis system needs additional sensors, and the PI control system's stability is not guaranteed due to the slow dynamic response of the frequency control compared to the voltage and current. The frequency regulation controller monitors and compares the time of each switching period to a reference switching period to compensate for the difference in the switching period [1]–[3], [13]–[18].

The implementation of the SMC scheme was directed toward numerical control, a new trend in timevarying reference applications. Because the dynamic response is slow when controlling the output voltage of the right-half plane-zero characteristic boost converter, so a non-linear sliding-mode current control (SMCC) is applied to improve it [19]–[21]. SMC and two-loop cascade control with a fixed-frequency operating mode are presented here to reduce the adverse impacts of wide variations in load and voltage values while preserving output voltage stability. The points mentioned above are expected to enhance the dynamic response of the system's output. Furthermore, the power factor correcting and raising the harmonics issues were overcome by controlling the current using SMC. As a result, it is known as the SMCC technique with a fixed output voltage value.

In this paper, section 2 introduces the design and analysis of the proposed SMCC, and the PI-two loop cascade control (TLCC) of the boost topology. Section 3 shows and discusses the simulation results of MATLAB/Simulink for the two proposed methods for the DC-DC and AC-DC boost converters. Finally, the conclusions for this paper are given in section 4.

2. RESEARCH METHOD

The proposed SMCC and PI-TLCC for the boost converter are presented in this section. For the SMCC method, a comprehensive mathematical analysis is introduced. The ideal sliding dynamics, the equilibrium-point analysis, and the ideal sliding dynamics linearization are presented in detail with related equations in this section.

2.1. The proposed SMCC-PFC boost converter

Figure 1 shows the proposed SMCC Simulink model through reference current (I_{ref}) generation in this work to achieve PFC for the AC-DC boost converter. The values of beta (β) and reference voltage (V_{ref}) are substantial factors in achieving the proposed control system. Figure 2 shows the SMC technique for the DC-DC boost converter, Figure 2(a) shows the sliding-mode voltage control (SMVC) circuit and Figure 2(b) shows SMCC circuit for regulating the voltage and the current. The Simulink model for the DC-DC boost converter is the same as Figure 1 except for the bridge part. The amplified output-voltage error is used in the proposed controller to generate the instantaneous reference-inductor-current (I_{ref}) as (1):

$$I_{ref} = K[V_{ref} - \beta_{\nu_o}] \tag{1}$$

where V_{ref} , v_o , β , and K refer to the reference voltage, the instantaneous output voltage, the feedback-network ratio, and the amplified gain of the voltage error, respectively. A great value of K is chosen to enhance the dynamic response and minimize the steady-state voltage error in the system.

In the proposed controller, the amplified output-voltage error generates the instantaneous reference inductor current I_{ref} . The proposed controller's sliding surface is made up of a linear combination of three state variables, with the switching function given by u = 1/2(1 + sign(S)), where u is the power switch logic state:

$$S = \alpha_1 X_1 + \alpha_2 X_2 + \alpha_3 X_3 \tag{2}$$

where α_1, α_2 , and α_3 denote the sliding coefficients. The adopted controlled state variables are the current error X_1 , the voltage error vX_2 , and the integral of both current and the voltage errors X_3 , which are expressed as:

$$\begin{cases} X_{1} = I_{ref} - I_{l} \\ X_{2} = V_{ref} - \beta_{vo} \\ X_{3} = \int (X_{1} + X_{2}) dt \\ \therefore X_{3} = \int (I_{ref} - I_{l}) dt + \int (V_{ref} - \beta_{vo}) dt \end{cases}$$
(3)

where I_l denotes the instantaneous inductor current. The dynamical model of the suggested system is as follows when the behavioral models of the boost converter under CCM are substituted into the time differentiation of (3):

$$\begin{cases} \dot{x}_{1} = \frac{d(I_{ref} - I_{l})}{dt} = -\frac{\beta K}{c} I_{c} - \frac{v_{in} - \bar{u} v_{o}}{L} \\ \dot{x}_{2} = \frac{d(V_{ref} - \beta_{v_{o}})}{dt} = -\frac{\beta}{c} I_{c} \\ \dot{x}_{3} = (X_{1} + X_{2}) = (I_{ref} - I_{l}) + (V_{ref} - \beta_{v_{o}}) \\ \therefore \dot{x}_{3} = (K + 1)(V_{ref} - \beta_{v_{o}}) - I_{l} \end{cases}$$
(4)

where u = 1 - u is the inverse logic of u. v_{in} , I_c , C, and L denote the instantaneous input voltage, instantaneous capacitor current, and converter's capacitance and inductance, respectively. The SMCC equivalent-control signal:

$$u_{eq} = 1 + \frac{\kappa_1}{v_o} (V_{ref} - \beta_{v_o}) - \frac{\kappa_2}{v_o} I_c - \frac{v_{in}}{v_o} - \frac{\kappa_3}{v_o} I_l$$
(5)

$$\begin{cases}
K_1 = \frac{\alpha_3}{\alpha_1} L(K+1) \\
K_2 = \frac{\beta L}{c} (K + \frac{\alpha_2}{\alpha_1}) \\
K_3 = \frac{\alpha_3}{\alpha_1} L
\end{cases}$$
(6)

This process provides the pulse width modulation (PWM) control architecture, and it reproduces the static and dynamic characteristics of the original SM controller while functioning as a PWM controller. The control signal V_c and the ramp signal V_{ramp} from the equations of the control law inherit the following form in the proposed controller:

$$\begin{cases} V_c \\ V_{ramp} = G_s K_1 (V_{ref} - \beta_{v_o}) - G_s K_2 I_c - G_s K_3 I_l + G_s (v_o - v_{in}) (7) \end{cases}$$

where $0 < G_s < 1$, $G_s = \beta$, the three SMCC requirements, namely the hitting, existence, and stability conditions, must be satisfied for SMCC operation in this controller. The existing condition may be determined by evaluating the local reachability condition $\lim_{S\to 0} S \cdot (dS/dt) < 0$, with the substitutions of (2) and its time derivative, which gives:

$$\begin{cases} \alpha_1 \left(-\frac{\beta K}{c} I_c - \frac{v_{in}}{L} \right) - \alpha_2 \frac{\beta}{c} I_c + \alpha_3 ((K+1)(V_{ref} - \beta_{v_o}) - I_l) < 0 \\ \alpha_1 \left(-\frac{\beta K}{c} I_c - \frac{v_{in}}{L} \right) - \alpha_2 \frac{\beta}{c} I_c + \alpha_3 ((K+1)(V_{ref} - \beta_{v_o}) - I_l) > 0 \end{cases}$$
(8)

The controller must be built with a static sliding surface to ensure steady-state operations (equilibrium point):

$$\begin{cases} 0 < V_{in(min)} - K_1(V_{ref} - \beta_{vo(SS)}) + K_2 I_{c(min)} + K_3 I_{l(max)} V_{in(max)} \\ - K_1(V_{ref} - \beta_{vo(SS)} + K_2 I_{c(max)} + K_3 I_{l(min)} < V_{o(SS)} \end{cases}$$
(9)

where $V_{in(max)}$, $V_{in(min)}$, and $V_{o(SS)}$ denote the maximum input voltage, minimum input voltage, and expected steady-state output voltage, respectively. $V_{o(SS)}$ is the essential dc parameter of the small error from the desired V_{ref} . $I_{l(max)}$, $I_{l(min)}$, $I_{c(max)}$, and $I_{c(min)}$ are the maximum inductor current, minimum inductor current, maximum capacitor current, and minimum capacitor current, respectively. The gain parameters selection of the controller K_1 , K_2 , and K_3 must comply with (9). This selection ensures that the SMCC operation will continue at least in the tiny region of origin for all operating conditions up to a full load.

For the ideal sliding dynamics, the discontinuous system is transformed into an ideal SM continuous system by replacing \bar{u} with \bar{u}_{eq} (the so-called equivalent control approach) in the original boost converter's description under the CCM operation, representing the ideal sliding dynamics of the SMCC boost converter.

$$\begin{cases} \frac{dI_L}{dt} = \frac{v_{in}}{L} - \frac{v_o}{L} \quad \bar{u}_{eq} \\ \frac{dv_o}{dt} = \frac{I_L}{C} \quad \bar{u}_{eq} - \frac{v_o}{r_l C} \end{cases}$$
(10)





Figure 1. Proposed SMCC Simulink model for PFC boost converter



Figure 2. SMC for the DC-DC boost converter (a) SMVC circuit and (b) SMCC circuit

If the sliding surface has a stable equilibrium point, and accordingly, the ideal sliding dynamics will be determined. If there are no input or loading disturbances at this equilibrium (stationary state), the system's dynamics will not change. i.e., $\frac{dI_L}{dt} = \frac{dv_o}{dt} = 0$. Then, the two formulas in (11) can be equated to zero to obtain the (12).

$$I_l = \frac{V_o^2}{V_{in}R_l} \tag{12}$$

 I_l , V_o , V_{in} , and R_l denote the inductor current, output voltage, input voltage, and load at steady-state equilibrium. The ideal sliding dynamics around the equilibrium point are then linearized, yielding from (11), as follows:

$$\begin{cases} \frac{d \tilde{V}_{l}}{dt} = a_{11} \tilde{I}_{l} + a_{12} \tilde{V}_{o} \\ \frac{d \tilde{V}_{o}}{dt} = a_{21} \tilde{I}_{l} + a_{22} \tilde{V}_{o} \end{cases}$$
(13)
$$\begin{cases} a_{11} = \frac{K_{3} V_{in} R_{l}}{K_{2} L V_{o} - L V_{in} R_{l}} \\ a_{12} = \frac{K_{1} \beta V_{in} R_{l} - 2 K_{2} V_{in} + \frac{V_{in}^{2} R_{l}}{V_{o}}}{K_{2} L V_{o} - L V_{in} R_{l}} \\ a_{21} = \frac{K_{2} V_{in} - \frac{V_{in}^{2} R_{l}}{K_{2} V_{o} - C V_{in} R_{l}}}{K_{2} V_{o} - C V_{in} R_{l}} \\ a_{22} = \frac{\frac{K_{2} V_{o}}{R_{l}} - K_{1} \beta V_{o}}{K_{2} V_{o} - C V_{in} R_{l}} - \frac{1}{C R_{l}} \end{cases}$$
(14)

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The derivation is performed by adopting static equilibrium conditions: $V_{in} = v_{in}$, $R_l = r_l$, $V_{ref} - \beta_{v_o} = 0$, and $I_{ref} - I_l = 0$, as well the assumptions $I_l \gg \tilde{I}_l$ and $V_o \gg \tilde{V}_o$; the linearized system characteristic equation will be given by:

$$S^{2} - (a_{11} + a_{22})S + a_{11}a_{22} - a_{12} + a_{21} = 0$$
(15)

$$(a_{11} + a_{22}) < 0, a_{11}a_{22} - a_{12} + a_{21} > 0$$
⁽¹⁶⁾

for the case of $(a_{11} + a_{22}) < 0$, the condition for stability is:

$$\frac{K_3 C V_{in} R_l - K_1 L \beta V_o + L V_{in}}{K_2 V_o - V_{in} R_l} < 0 \tag{17}$$

$$\begin{cases} K_3 \frac{CR_l V_{in}}{L\beta V_o} + \frac{V_{in}}{\beta V_o} < K_1, K_2 > \frac{V_{in} R_l}{V_o} \\ K_3 \frac{CR_l V_{in}}{L\beta V_o} + \frac{V_{in}}{\beta V_o} > K_1, K_2 < \frac{V_{in} R_l}{V_o} \end{cases}$$
(18)

for the case of $a_{11}a_{22} - a_{12} + a_{21} > 0$, the condition for stability is (19).

$$2K_3V_o^3(K_2 - K_1\beta R_l) + K_2V_o^2V_{in}(K_1\beta R_l - 2K_2) + V_o^2V_{in}R_l(3K_2 - K_1\beta R_l) - V_{in}^3R_l^2 > 0$$
(19)

The control gains and design for the proposed SMCC depend on the existing condition of (9) and the stability conditions of (18) and (19). If met, the system's closed-loop stability is guaranteed.

2.2. The proposed PI-TLCC for the boost converter

The proposed cascade PI controller has current inner and voltage outer loops. The output voltage is compared to a voltage reference to generate an inductor reference current. The inner loop provides the duty cycle for the pulse width modulation. Figure 3 depicts the proposed PI-TLCC Simulink model for the DC-DC boost converter. The control system aims to track the reference signal as a desired external signal supplied to the outer control loop. The outer loop controller produces the reference signal for the inner loop. Here, the PI-TLCC is a DC-DC boost converter. The outer-loop controller is of the PI type and is considered to control the converter output voltage. The inner loop is a PI controller designed to control the inductor current [22], [23]. Values for the controller gains are determined by Ziegler–Nichol's method to ensure that the PI controller parameters are tuned [24]. The main equations of reference current and controller output (U) for the PI-TLCC method are given in (20) and (21), where K_p and K_i are the PI control gain parameters.

$$I_{ref} = (V_{ref} - V_{out})(K_p + \frac{K_i}{s})$$
(20)

$$U = (I_{ref} - I_l)(K_p + \frac{\kappa_i}{s})$$
⁽²¹⁾



Figure 3. Proposed PI-TLCC Simulink model for DC-DC boost converter

3. RESULTS AND DISCUSSION

The SMC design in [19] was re-simulated to validate the simulation methodology. Both the re-simulation and published results of V_{in} , V_o , I_{in} , and I_o signals of control, ramp, and gate pulse were identical. This study applied SMC and TLCC methods to the boost converter. Tables 1 and 2 show the coefficients of the boost

converter in the case of DC and AC, respectively. The SMCC steady-state simulation results at 1 s for the DC-DC boost converter are shown in Figure 4. Figures 4(a)-(d) shows $I_{in} = 3.6 \text{ A} \& I_o = 1.52$, $V_{in} = 24 \text{ V}$ and $V_o = 47 \text{ V}$, control and ramp input signals of 9.4 V and 8 V, and control and gate pulse signals of 9.4 V and 10 V. Such results confirmed excellent performance under the full-load condition of 30 Ω and the rated input voltage of 24 V. When SMCC is applied to the DC-DC boost converter, the importance of both β and V_{ref} values can affect both the output waveform and the system's dynamic response. The SMCC results of the dynamic response at 2 s for DC-DC boost converters are shown in Figure 5. Figures 5(a)-(d) shows V_{in} and V_o at $\beta = 1/8$, I_{in} and I_o at $\beta = 1/6$, and I_{in} and I_o at $\beta = 1/6$. The dynamic responses of step load variation from 30 Ω to 60 Ω and step voltage variation from 18 V to 24 V are shown in Figures 5(e)-(h). Such results are promising since the output voltage is regulated at the desired value of 47 V, as is the positive dynamic response of the system.



Figure 4. Zoomed-in SMCC steady-state response (a) I_{in} and I_o, (b) V_{in} and V_o, (c) control and ramp input signals, and (d) control and gate pulse signals



Figure 5. SMCC dynamic response (a) V_{in} and V_o at $\beta = 1/8$, (b) I_{in} and I_o at $\beta = 1/8$, (c) V_{in} and V_o at $\beta = 1/6$ (d) I_{in} and I_o at $\beta = 1/6$, (e) V_{in} and V_o step load variation, (f) I_{in} and I_o step load variation, (g) V_{in} and V_o step voltage variation, and (h) I_{in} and I_o step voltage variation

Table 1. Specification and components used in the simulation of a DC-DC boost converter

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	24	V
Reference voltage	V_{ref}	8,6	V
Output Voltage	V_o	48	V
Load	R	30	Ω
Capacitor	C_o	220	μF
Inductor	L	470	μH
Beta	β	1/6, 1/8	
Switching frequency	F_S	150	kHz

Table 2. Specification and components used in the simulation of an AC-DC boost converter

Parameter	Symbol	Value	Unit
Input voltage	V_{in}	40	V(RMS)
Supply frequency	F	50	Hz
Output Voltage	V_O	100	V
Load	R	100	Ω
Capacitor	C_o	1000	μF
Inductor	L	3	mH
Reference voltage	V_{ref}	20	V
Switching frequency	F_{S}	20	kHz
Beta	β	1/5	

Figure 6 shows the SMCC steady-state results for the AC–DC PFC boost converter. Figures 6(a)-(e) shows $I_{in} = 16$ A and $I_o = 1.04$ A, $V_{in} = 56.56$ V and $V_o = 100$ V, control from -13 V to 24 V and ramp signals of 20 V, gate signal of 10 V, and THD of 2.21%. The challenge is to minimize the harmonics and have a sinusoidal waveform for the input current to improve the system efficiency and reach the unity power factor of the boost converter, which was addressed by the proposed SMCC-PFC boost converter. The obtained power factor value was 0.99, and the harmonic value was reduced to 2.21%, using the proposed method compared to literature results [24], [25], since they achieved a power factor of 0.98 and total harmonic distortions of 2.4% and 2.38%, respectively, under 100% full load.



Figure 6. SMCC results for the boost converter (a) I_{in} and I_{out}, (b) V_{in} and V_{out}, (c) control and ramp input signals, (d) gate signal, and (e) total harmonic distortion

Figure 7 depicts the steady-state and dynamic responses of the PI-TLCC for the DC-DC boost converter under step load and step voltage variations of 200% and 75%, respectively. Figures 7(a)-(b) shows $V_{in} = 24 \text{ V}$ and $V_o = 48 \text{ V}$ and $I_{in} = 3.5 \text{ A}$ and $I_o = 1.6 \text{ A}$. The results were obtained under load variations of 30 Ω to 60 Ω and input voltage variations of 18 V to 24 V for the TLCC control method used with the boost converter as in Figures 7(c)-(f). Finally, the boost converter has a stable dynamic response to load and voltage variations.

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Figure 7. TLCC steady-state and dynamic (a) V_{in} and V_{out} , (b) I_{in} and I_{out} , (c) V_{in} and V_{out} load variation, (d) I_{in} and I_{out} load variation, (e) V_{in} and V_{out} step voltage variation, and (f) I_{in} and I_{out} step voltage variation

4. CONCLUSION

The SMCC simulation results for AC-DC and DC-DC converters are presented in this study. A fixedfrequency fast-response SMCC is proposed for the DC-DC boost converter, which provides a faster reaction with minor voltage overshoot across a wide range of operating conditions. According to simulation findings, the proposed SMCC and two-loop cascade control strategies for the boost converter are valid and resilient against changes in load from 30 Ω to 60 Ω or input voltage from 18 V to 24 V. The proposed approaches have many advantages: stability, robustness, and good dynamic performance. The SMCC converter has low input current harmonics to comply with IEC 61000-3-2 harmonic regulations and a high-power factor of 0.99 using the proposed control for the power factor correction (PFC) boost converter. SMCC can be used for buck and buck-boost PFC converters in the continuous conduction mode. The proposed converter provides a low total harmonic distortion of 2.21% at full load.

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