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A low power and high speed 45 nm CMOS dynamic comparator with low offset

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ABSTRACT

The development of efficient data converters necessitates the design of low-power and high-speed comparators with low offset. Data converters, such as analog to digital converters (ADCs) and digital to analog converters (DACs), are critical components in applications like wireless communication, multimedia, and sensor interfaces. To enhance the performance of these data converters, improving the speed and power efficiency of comparators becomes crucial. Designing dynamic comparators with low power consumption and high-speed capabilities greatly enhances the sampling rate and accuracy of data converters. Moreover, addressing the offset voltage of comparators becomes crucial for achieving accurate signal conversion. To fulfill this need, a novel dynamic comparator has been designed, featuring high-speed operation, low-power consumption, and minimal offset. The circuit comprises a pre-amplifier with a charge pump, followed by a decision circuit and an output stage. Through simulations, the comparator has demonstrated low power consumption of 15.04 µW, a delay of 80.51 ps, and an extremely low offset voltage of 8 µV. These characteristics make it highly suitable for data converters. The comparator operates at a clock frequency of 1 GHz and a supply voltage of 1 V, and the simulation was conducted using the Cadence Virtuoso tool in a 45 nm CMOS technology.

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1. INTRODUCTION

CMOS comparators are versatile components with wide-ranging applications in various electronic systems. Their ability to compare voltages accurately, provide precise outputs, and consume low power makes them essential for achieving high-performance, low-power designs in ADCs [1]–[5], DACs [6], [7], voltage references [8], overvoltage and undervoltage protection [9], motor control systems [10], [11], photovoltaic systems [12], [13], pulse-width modulation circuits, voltage level detection and window detection circuits. Comparators transform analog input signal differences into digital outputs. Figure 1 depicts the internal components, including a pre-amplifier for enhanced sensitivity. The decision stage identifies the larger input, generating the digital output. The post-amplifier (output buffer) amplifies this information to obtain the digital output.

Static comparators utilizing CMOS amplifiers exhibit restricted speed and elevated power dissipation [14]. Dynamic comparators were introduced as a viable alternative to mitigate these challenges. Incorporating positive feedback and low static power consumption, dynamic comparators demonstrate rapid operation and power efficiency, rendering them indispensable in mixed-signal circuitry. Single-stage dynamic comparators,

which consist of a latching circuit and current-mode logic preamplifier, confer speed and power benefits; however, they are susceptible to kickback noise caused by capacitive interconnections [15].

Despite attempts to mitigate kickback noise, one-stage dynamic comparators compromise offset voltage and power consumption [16]. The strong-arm latch and its variations are favoured for low static power, high speed, and full output swing but require substantial voltage headroom [17], [18]. Consequently, two-stage dynamic comparators are preferred. A double-tail latch-type voltage sensing amplifier in a two-stage comparator delivers superior offset per power ratio at high common mode voltages and low supply voltage [19]. However, the second stage's gain reduction escalates input referred noise [20]. Alternative approaches like time domain bulk tuned offset cancellation reduce offset voltage but operate at slower speeds [21]. Positive feedback in the pre-amplifier improves regeneration but increases kickback noise [22]. Directly connecting the output nodes of the first and second stages enhances speed and area but results in significant offset, high power consumption, and severe kickback noise [23]. Techniques such as delayed clocks [24], dynamic bias preamplifiers [25], and nMOS transistor pre-amplifier stages [26] address offset, power, and speed trade-offs. Figure 2 depicts Miyahara's comparator, featuring a pMOS input pair which minimizes input-referred noise [27].

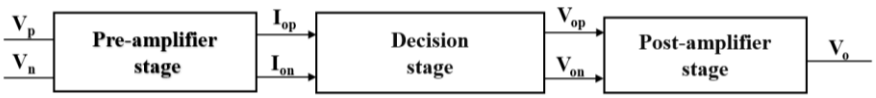

Figure 1. Block diagram of comparator

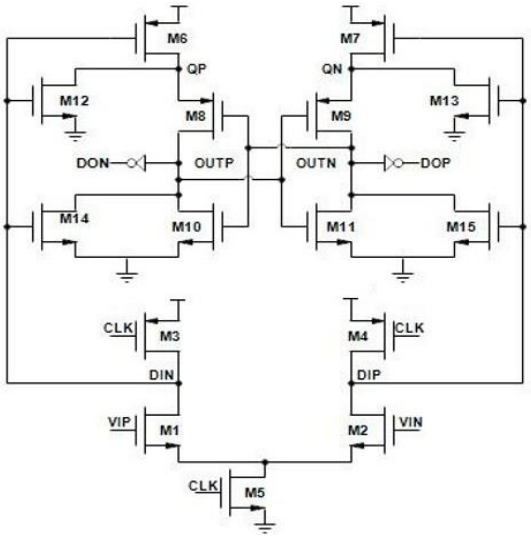

Figure 2. The Miyahara's comparator [27]

The comparator in [28] employs multiple clock signals to extend the saturation time of input transistors, resulting in improved speed and noise response. However, this approach leads to increased power consumption and offset voltage. In the pre-amplifier of a two-stage comparator [29], a pMOS latch and cross-coupled circuit are used to enhance speed, but at the expense of offset and power consumption. Recent advancements in dynamic comparators [30]–[35] include techniques such as cross-coupled transistors in the latching stage [30], which enhance transconductance but introduce significant offset voltage, affecting accuracy. Additionally at high operating frequencies the comparator operates at low speed and consumes high power and causes high offset. The comparator described in [31] utilizes a bulk driven approach to optimize offset and kickback noise, albeit at the expense of speed and increased power consumption.

Building upon the investigations conducted on dynamic comparators, this research paper introduces a two-stage dynamic comparator that incorporates a double-tail latch. To enhance comparator gain while reducing noise, the pre-amplifier stage employs a cascode differential amplifier. Within the preamplifier stage, a charge pump is employed to improve speed and achieve minimal offset and power consumption. The design of the proposed dual-stage dynamic comparator is detailed in section 2, followed by the analysis of simulation

results in section 3. Section 4 presents the key findings, emphasizing the significance of the proposed two-stage dynamic comparator, and highlighting its potential impact in mixed-signal circuitry.

2. DESIGN OF PROPOSED DUAL STAGE LATCH TYPE DYNAMIC COMPARATOR

Figure 3 illustrates a latch type dynamic comparator consisting of two stages. The initial stage functions as a pre-amplifier and utilizes a cascode differential amplifier, comprising transistors M1, M2, Mg1, and Mg2. This configuration ensures high gain, low noise, and a high output impedance. Transistors M1 and M2 interact with the input voltages VIP and VIN. The current sources M3 and M4, regulated by the CLK signal, employ pMOS transistors. To enhance switching activity and generate VTOP, a charge pump employing transistors M16 and M17, as well as capacitors C1, C2, and C3, is incorporated. Following the pre-amplifier stage is the decision circuit, which consists of back-to-back inverters (M8, M10, M9, M11). The outputs of the first stage, DIN and DIP, serve as inputs for the decision stage. Finally, the comparator output is directed to the buffer stage, with transistors M6 to M7 serving as the post-amplifier.

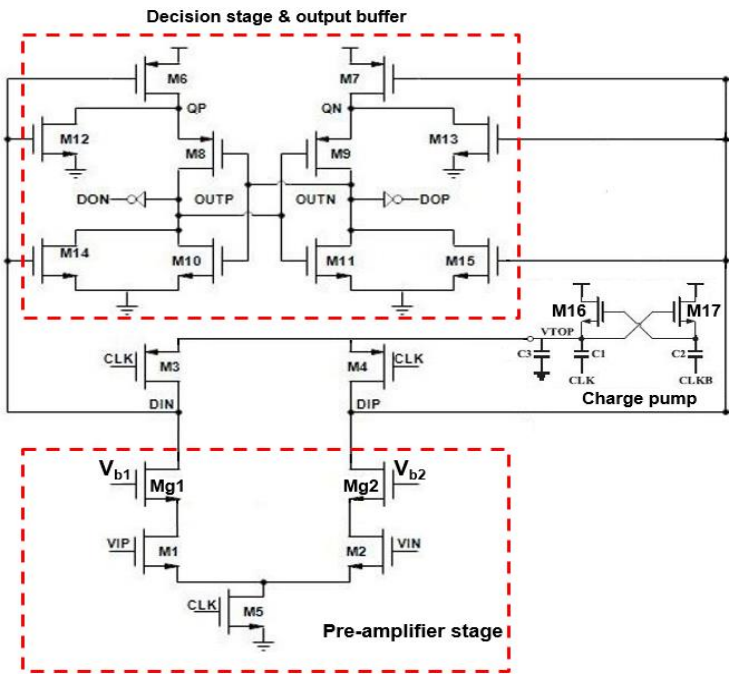

Figure 3. Schematic of proposed dual stage dynamic comparator

2.1. Working strategy of proposed dual stage dynamic comparator

The comparator operates in three phases: reset, evaluation, and comparison. In the reset phase, M3 and M4 charge the parasitic capacitance of DIP and DIN nodes, while M14 and M15 discharge the output nodes. During evaluation, M5 turns on, gradually reducing the voltages at DIP and DIN, and VTOP rises rapidly to activate the first stage input pair, increasing current flow and amplification. The second stage latch timing is optimized to reduce delay. M6 and M7 act as pre-charge switches and inputs to the second latch stage, boosting gain, sensitivity, and speed. During regeneration, M10 and M11 provide positive feedback for the result, while M12 and M13 reset QP and QN to prevent mismatch-induced offset.
The output current of pre-amplifier stage is obtained as:

$$I_{op} = -I_{on} \tag{1}$$

$$I_{op} = \frac{g_m}{2(V_{ip}-V_{in})} + \frac{I_{ss}}{2} \tag{2}$$

where g_m is the transconductance, V_{ip} and V_{in} are the input voltages. Assuming that I_{op} is much larger than I_{on} and the output voltage V_{op} is (3).

$$V_{op} = \frac{\sqrt{2I_{op}}}{\beta_A} + V_{THN} \tag{3}$$

The current flowing through decision stage transistors M11 and M14 is obtained as (4) and (5).

$$I_{on} = \frac{\beta_B}{2(V_{op} - V_{THN})^2} \tag{4}$$

$$I_{op} = \frac{\beta_A}{2(V_{op} - V_{THN})^2} \tag{5}$$

3. RESULTS AND DISCUSSION

The double tail latch type dynamic latch comparator circuit underwent validation using the SPECTRE simulator within CADENCE Virtuoso. The validation was conducted under the conditions of a 1 V supply voltage, a temperature of 27 ^{0}C, and utilizing a 45nm CMOS process. Figure 4 illustrates the comparator output at node OUTP as obtained from the simulation. The adjustment of VTOP to 1.65 V effectively decreases the falling edge delay of DIP and DIN, leading to an accelerated latch time for the second stage. The propagation delay, which quantifies the duration between the clock edge and the output, measures 80.51 ps and is presented in Figure 5. Furthermore, the comparator design demonstrates a commendably low offset voltage of 8 µV, visually represented in Figure 6.

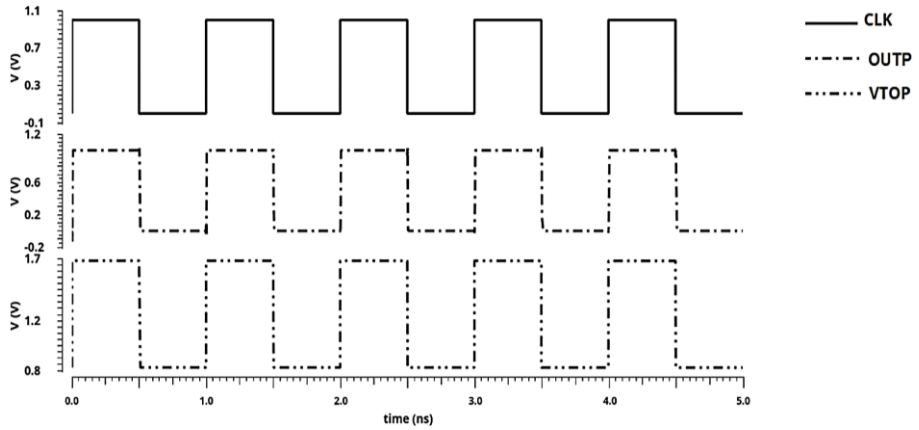

Figure 4. Simulated output of the proposed comparator

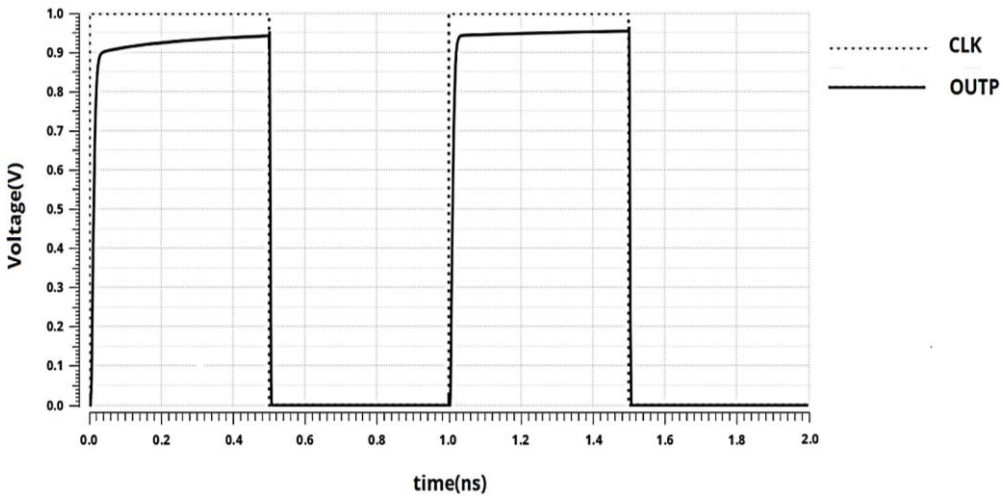

Figure 5. Propagation delay

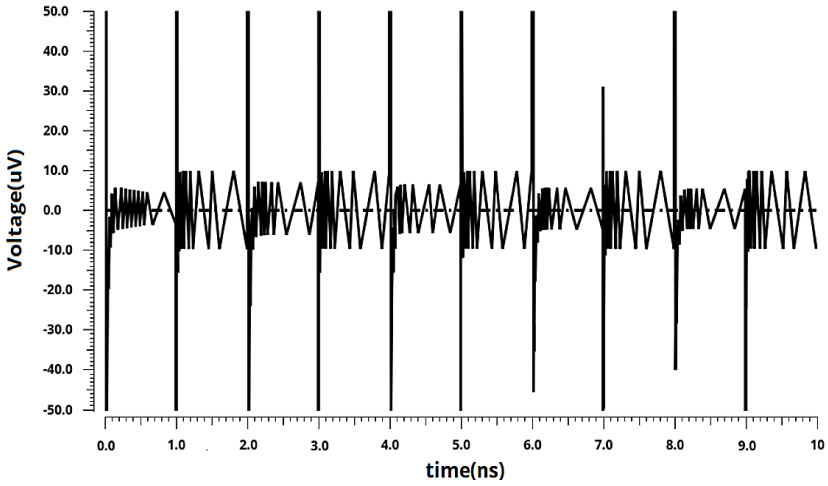

Figure 6. Comparator offset voltage

3.1. Monte Carlo analysis for power

The proposed comparator has achieved an average power of 15.04 µW at 1 GHz clock frequency. Monte Carlo study on average power is performed through 200 random statistical runs of simulation. The mean value of the average power is found to be very much close to the value obtained at the (ss) corner. Using Monte Carlo simulations, a histogram plot of average power is shown in Figure 7.

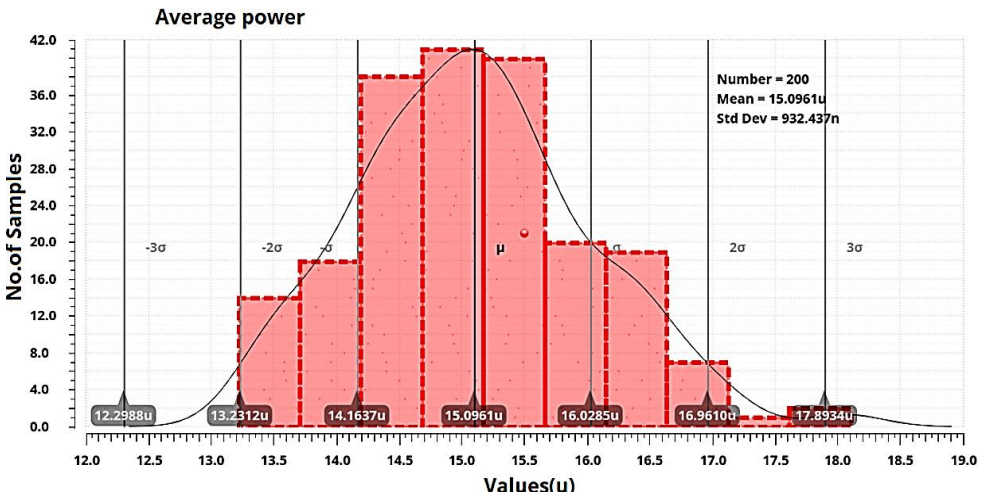

Figure 7. Histogram plot of average power for the proposed comparator

3.2. Corner simulations

To validate the benefit of low power consumption, the proposed comparator was examined under various process corners (ss-slow-slow, tt-typical-typical, ff-fast-fast), voltage (0.6, 0.8, and 1 V) and temperature (0°, 27°, and 70 °C). The power consumption varies based on VDD variation. Table1 presents the results of average power obtained for 1 GHz at 27 corners.

3.3. Layout

A proposed comparator has been realized in 45nm CMOS technology and the layout in Figure 8 is obtained using Cadence Virtuoso layout tool. Table 2 presents a comparative analysis of the newly suggested and previously reported circuits. The critical aspects of the comparators are high power consumption and offset voltage. Mainly higher offset voltage directly affects the accuracy of the comparator. From Table 2, the reported works in [22], [29], and [30] exhibit higher offset and power consumption. Compared to [27], the proposed comparator consumes less power at a 1 GHz frequency. The proposed circuit achieves a minimal

offset of 8 µV. Compared to [31], the proposed comparator operates at low power of 15.04 µW and has a delay of 80.5 1 ps, making it a better design in terms of lower PDP.

Table 1. Power of the comparator obtained at different corners

VDD	Power @ 1G Hz (µW)								
		T = 0 °C			T = 27 °C			T = 70 °C	
	ss	tt	ff	ss	tt	ff	ss	tt	ff
0.6 V	7.70	11.49	16.26	7.33	12.68	20.54	15.9	44.53	62.82
		T = 0 °C			T = 27 °C			T = 70 °C	
	ss	tt	ff	ss	tt	ff	ss	tt	ff
0.8 V	12.22	19.08	30.62	11.65	19.15	32.58	15.32	39.77	65.82
		T = 0 °C			T = 27 °C			T = 70 °C	
	ss	tt	ff	ss	tt	ff	ss	tt	ff
1 V	16.24	35.42	58.22	15.04	35.04	56.59	21.04	46.9	78.86

Table 2. Performance comparison

References	Technology	Operating Frequency (Hz)	Supply Voltage (V)	Power (µ W)	Delay (ps)	Offset voltage (mV)	PDP
[22]	180 nm	500M	1.2	329	550	7.8	22.7fJ
[29]	180 nm	0.5G	1.8	230	263	2	60.5fJ
[30]	180 nm	2G	1.2	72.2	268.6	7.3	19.39fJ
[27]	90 nm	1G	1	40	122	1.69	4.90fJ
[31]	45 nm	250M	1.2	24.92	127	--	3.16fJ
Proposed	45 nm	1G	1	15.04	80.51	8 µ	1.21fJ

--Not reported

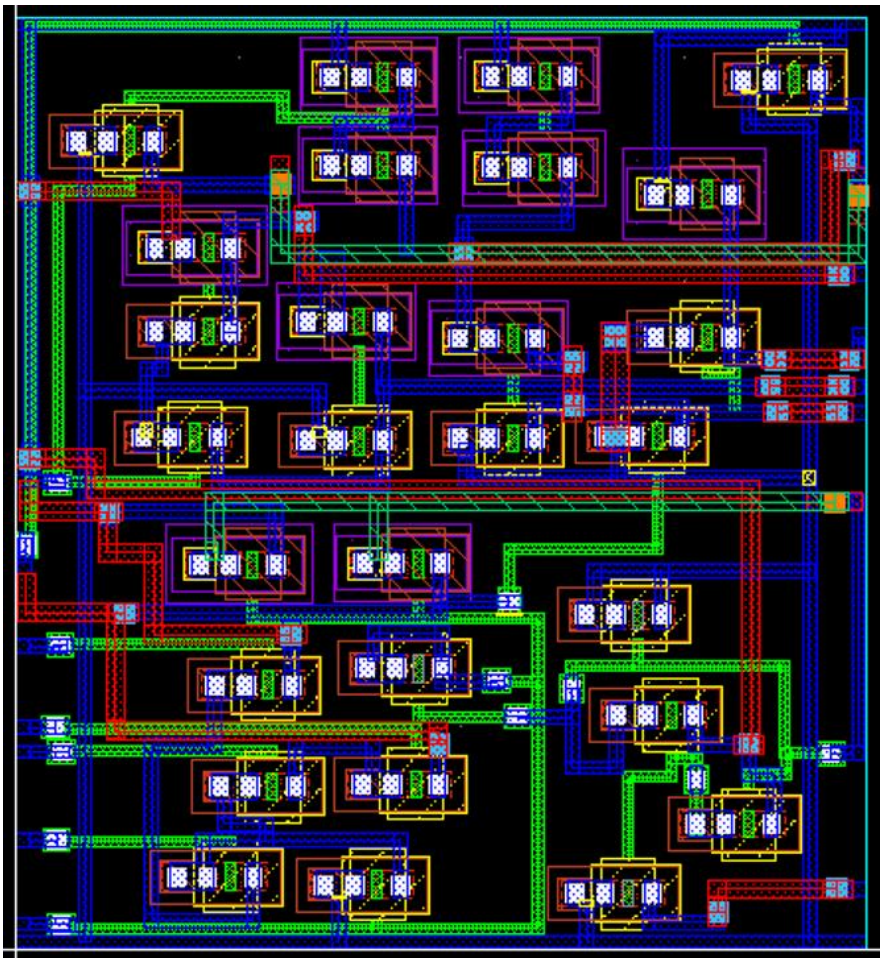

Figure 8. Layout of the proposed comparator

4. CONCLUSION

A unique high-speed dual stage latch type dynamic comparator is introduced. By incorporating a cascode differential amplifier and a charge pump into the pre-amplifier stage, the comparator's speed is significantly enhanced. Simulation results indicate that the comparator operates with reduced power consumption and minimal offset. Consequently, this design is better suited for developing data converters for applications that require high-speed performance and low power consumption.

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REFERENCES

[1] H. Zhuang, C. Tong, X. Peng, and H. Tang, "Low-Power, Low-Noise Edge-Race Comparator for SAR ADCs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 12, pp. 2699–2707, 2020, doi: 10.1109/TVLSI.2020.3021680.

[2] M. Asgari, K. S. Lee, and H. Chung, "Highly Area Efficient Component Sharing Extended Counting ADC for Multi-Channel Sensing," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 3, pp. 889–893, 2023, doi: 10.1109/TCSII.2022.3219768.

[3] M. Hosseinnejad and H. Shamsi, "Fully differential charge-pump comparator-based pipelined ADC in 90 nm CMOS," *Microelectronics Journal*, vol. 53, pp. 8–15, 2016, doi: 10.1016/j.mejo.2016.04.003.

[4] Y. Shu, F. Mei, Y. Yu, and J. Wu, "A 5-Bit 500-MS/s Asynchronous Digital Slope ADC with Two Comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 65, no. 4, pp. 426–430, 2018, doi: 10.1109/TCSII.2017.2695720.

[5] S.-H. Wang and C.-C. Hung, "A 0.3V 10b 3MS/s SAR ADC with Comparator Calibration and Kickback Noise Reduction for Biomedical Applications," *IEEE Transactions on Biomedical Circuits and Systems*, pp. 1–1, 2020, doi: 10.1109/TBCAS.2020.2982912.

[6] K. Bunsen, E. Martens, D. Dermit, and J. Craninckx, "A Redundancy-Based Background Calibration for Comparator Offset/Threshold and DAC Gain in a Ping-Pong SAR ADC," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 68, no. 2, pp. 592–596, 2021, doi: 10.1109/TCSII.2020.3046091.

[7] Y. S. Shu, L. T. Kuo, and T. Y. Lo, "An Oversampling SAR ADC with DAC Mismatch Error Shaping Achieving 105 dB SFDR and 101 dB SNDR over 1 kHz BW in 55 nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 51, no. 12, pp. 2928–2940, 2016, doi: 10.1109/JSSC.2016.2592623.

[8] B. Do Yang, "250-mV Supply subthreshold CMOS voltage reference using a low-voltage comparator and a charge-pump circuit," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 61, no. 11, pp. 850–854, 2014, doi: 10.1109/TCSII.2014.2350354.

[9] A. Rahman *et al.*, "High-Temperature SiC CMOS Comparator and op-amp for Protection Circuits in Voltage Regulators and Switch-Mode Converters," *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 4, no. 3, pp. 935–945, 2016, doi: 10.1109/JESTPE.2016.2584599.

[10] K. Vanchinathan, K. R. Valluvan, C. Gnanavel, C. Gokul, and J. R. Albert, "An improved incipient whale optimization algorithm based robust fault detection and diagnosis for sensorless brushless <scp>DC</scp> motor drive under external disturbances," *International Transactions on Electrical Energy Systems*, vol. 31, no. 12, pp. 1–23, Dec. 2021, doi: 10.1002/2050-7038.13251.

[11] J. R. Albert, A. A. Stonier, and K. Vanchinathan, "Testing and performance evaluation of water pump irrigation system using voltage-lift multilevel inverter," *International Journal of Ambient Energy*, vol. 43, no. 1, pp. 8162–8175, 2022, doi: 10.1080/01430750.2022.2092773.

[12] J. R. Albert, K. Ramasamy, V. Joseph Michael Jerard, R. Boddepalli, G. Singaram, and A. Loganathan, *A Symmetric Solar Photovoltaic Inverter to Improve Power Quality Using Digital Pulsewidth Modulation Approach*, no. 0123456789. 2023.

[13] T. Yuvaraj, "Deep Learning–Based Predictive Maintenance of Photovoltaic Panels," *Photovoltaic Systems*, pp. 123–137, 2022, doi: 10.1201/9781003202288-7.

[14] B. Razavi and B. A. Wooley, "Design Techniques for High-Speed, High-Resolution Comparators," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 12, pp. 1916–1926, 1992, doi: 10.1109/4.173122.

[15] T. B. Cho and P. R. Gray, "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, vol. 30, no. 3, pp. 166–172, 1995, doi: 10.1109/4.364429.

[16] P. M. Figueiredo and J. C. Vital, "Kickback Noise Reduction Techniques for CMOS Latched Comparators," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 53, no. 7, pp. 541–545, 2006, doi: 10.1109/TCSII.2006.875308.

[17] B. Razavi, "The StrongARM latch [A Circuit for All Seasons]," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015, doi: 10.1109/MSSC.2015.2418155.

[18] Yun-Ti Wang and B. Razavi, "An 8-bit 150-MHz CMOS A/D converter," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 3, pp. 308–317, Mar. 2000, doi: 10.1109/4.826812.

[19] D. Schinkel, E. Mensink, E. Klumperink, E. Van Tuijl, and B. Nauta, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," *Digest of Technical Papers - IEEE International Solid-State Circuits Conference*, 2007, doi: 10.1109/ISSCC.2007.373420.

[20] H. Zhuang, H. Tang, and X. Liu, "Voltage Comparator with 60% Faster Speed by Using Charge Pump," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 12, pp. 2923–2927, 2020, doi: 10.1109/TCSII.2020.2983928.

[21] J. Lu and J. Holleman, "A low-power high-precision comparator with time-domain bulk-tuned offset cancellation," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 60, no. 5, pp. 1158–1167, 2013, doi: 10.1109/TCSI.2013.2239175.

[22] S. Babayan-Mashhadi and R. Lotfi, "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 22, no. 2, pp. 343–352, Feb. 2014, doi: 10.1109/TVLSI.2013.2241799.

[23] M. Abbas, Y. Furukawa, S. Komatsu, T. J. Yamaguchi, and K. Asada, "Clocked comparator for high-speed applications in 65nm technology," *2010 IEEE Asian Solid-State Circuits Conference, A-SSCC 2010*, pp. 277–280, 2010, doi: 10.1109/ASSCC.2010.5716609.

[24] M. Hassanpourghadi, M. Zamani, and M. Sharifkhani, "A low-power low-offset dynamic comparator for analog to digital converters," *Microelectronics Journal*, vol. 45, no. 2, pp. 256–262, Feb. 2014, doi: 10.1016/j.mejo.2013.11.012.
[25] H. S. Bindra, C. E. Lokin, A. J. Annema, and B. Nauta, "A 30fJ/comparison dynamic bias comparator," *ESSCIRC 2017 - 43rd IEEE European Solid State Circuits Conference*, pp. 71–74, 2017, doi: 10.1109/ESSCIRC.2017.8094528.
[26] S. D'Amico, G. Cocciolo, A. Spagnolo, M. De Matteis, and A. Baschirotto, "A 7.65-mW 5-bit 90-nm 1-Gs/s folded interpolated ADC without calibration," *IEEE Transactions on Instrumentation and Measurement*, vol. 63, no. 2, pp. 295–303, 2014, doi: 10.1109/TIM.2013.2278998.
[27] M. Miyahara, Y. Asada, D. Paik, and A. Matsuzawa, "A low-noise self-calibrating dynamic comparator for high-speed ADCs," *Proceedings of 2008 IEEE Asian Solid-State Circuits Conference, A-SSCC 2008*, pp. 269–272, 2008, doi: 10.1109/ASSCC.2008.4708780.
[28] C. H. Chan, Y. Zhu, U. F. Chio, S. W. Sin, U. Seng-Pan, and R. P. Martins, "A reconfigurable low-noise dynamic comparator with offset calibration in 90nm CMOS," *2011 Proceedings of Technical Papers: IEEE Asian Solid-State Circuits Conference 2011, A-SSCC 2011*, pp. 233–236, 2011, doi: 10.1109/ASSCC.2011.6123645.
[29] A. Khorami and M. Sharifkhani, "A low-power high-speed comparator for precise applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 26, no. 10, pp. 2038–2049, 2018, doi: 10.1109/TVLSI.2018.2833037.
[30] Y. Wang, M. Yao, B. Guo, Z. Wu, W. Fan, and J. J. Liou, "A Low-Power High-Speed Dynamic Comparator With a Transconductance-Enhanced Latching Stage," *IEEE Access*, vol. 7, pp. 93396–93403, 2019, doi: 10.1109/ACCESS.2019.2927514.
[31] A. K. Dubey and R. K. Nagaria, "Optimization for offset and kickback-noise in novel CMOS double-tail dynamic comparator: A low-power, high-speed design approach using bulk-driven load," *Microelectronics Journal*, vol. 78, pp. 1–10, 2018, doi: 10.1016/j.mejo.2018.05.006.
[32] J. Zhang, X. Ren, S. Liu, C. H. Chan, and Z. Zhu, "An 11-bit 100-MS/s Pipelined-SAR ADC Reusing PVT-Stabilized Dynamic Comparator in 65-nm CMOS," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 67, no. 7, pp. 1174–1178, 2020, doi: 10.1109/TCSII.2019.2935171.
[33] H. Xu and A. A. Abidi, "Analysis and Design of Regenerative Comparators for Low Offset and Noise," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 66, no. 8, pp. 2817–2830, 2019, doi: 10.1109/TCSI.2019.2909032.
[34] L. Qiu, T. Meng, B. Yao, Z. Du, and X. Yuan, "A High-Speed Low-Noise Comparator With Auxiliary-Inverter-Based Common Mode-Self-Regulation for Low-Supply-Voltage SAR ADCs," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 31, no. 1, pp. 152–156, 2023, doi: 10.1109/TVLSI.2022.3224237.
[35] J. R. Rusli, S. Shafie, R. M. Sidek, H. A. Majid, W. Z. Wan Hassan, and M. A. Mustafa, "Optimized low voltage low power dynamic comparator robust to process, voltage and temperature variation," *Indonesian Journal of Electrical Engineering and Computer Science*, vol. 17, no. 2, pp. 783–792, 2019, doi: 10.11591/ijeecs.v17.i2.pp783-792.

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