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The 1.5 bit-per-stage 10-bit pipelined CMOS A/D converter for CMOS image sensor

Aicha Menssouri, Karim El Khadiri, Ahmed Tahiri
Laboratory of Computer Science and Interdisciplinary Physics (L.I.P.I), Normal Superior School Fez (ENSF),
Sidi Mohamed Ben Abdellah University, Fez, Morocco

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ABSTRACT

This paper presents a 1.5-bit/stage pipeline analog-to-digital converters (ADC) with a 100 MHz operating frequency for CMOS image sensors built using TSMC 90nm CMOS technology. The design features a novel architecture including a comparator, CMOS transmission gates, a sub-ADC logic circuit, bootstrap switches, and a gain-boosted fully differential telescopic op-amp based switched-capacitor MDAC. The ADC operates on a 1.8 V power supply, with a typical power dissipation of 1.632 mW, and a full-scale input signal voltage of 0.8 V. At 100 MHz sampling frequency, it achieves a maximum ENOB of 12.42 bits, an SNR of 76.53 dB, and a FOM of 0.297 pJ/conversion step. This 1.5-bit/stage pipeline ADC is well-suited for CMOS image sensors.

Corresponding Author:

Aicha Menssouri
Laboratory of Computer Science and Interdisciplinary Physics (L.I.P.I)
Normal Superior School Fez (E.N.S.F), Sidi Mohamed BenAbdellah University
Fez, Morocco
Email: aicha.menssouri@usmba.ac.ma

1. INTRODUCTION

In recent years, there has been increased interest in using images to interpret the world. CMOS image sensors (CIS) play a crucial role in this process by converting optical signals into electrical signals, serving as an interface between external objects and internal digital signal processor (DSP) systems [1]–[3]. A typical CIS device consists of a vertical shift register, a pipeline analog-to-digital converter array, a pixel array, a bias circuit, and a clock generator. In order to effectively digitize large pixel arrays, CIS devices need to have a high-precision, small-area ADC with low power consumption [4]–[6].

Pipeline analog-to-digital converters (ADCs) are commonly used in a variety of digital imaging systems, such as medical imaging, digital receivers, base stations, and digital video. They provide a good balance of resolution, speed, and power efficiency [7]. By using a limited number of comparators, pipeline ADCs reduce power dissipation for high-resolution (N-bit) systems. Additionally, they are more suitable for high sample rates as they process multiple bits at the same time [8].

The paper is structured as follows: in section 2, we discuss the 1.5-bit/stage pipeline ADC design. Section 3 describes all the blocks that contain our ADC, whereas this latter is divided into subsections: i) Shows the sub-ADC block, which includes comparators and a sub-ADC logic circuit; ii) Explains the operational amplifier design for the MDAC block; and iii) Presents the switches used in the system. Section 4 mainly focuses on circuit analyses, including simulation and FFT analyses. Section 5 concludes the work of this paper.

2. DESIGN OF THE 1.5-BIT/STAGE PIPELINE ADC

The design of a 10-bit pipeline ADC is depicted in Figure 1. It consists of 9 comparator stages, all of which are 1.5-bits except for the last stage which is a normal 2-bit flash ADC [9]. Each 1.5-bit stage is composed of two main components: a sub-ADC and a MDAC. The Sub-ADC, which includes two comparators and sub-ADC logic, produces two digital bits by comparing the input signal during the first clock phase (Φ1). The MDAC is comprised of a sample and hold (S/H) block and an operational amplifier that amplifies the input signal by a factor of two. During the second clock phase, Φ2, the input signal is multiplied by two using the MDAC. The result is then modified by adding either -VFS, +VFS, or 0, based on the decision made by the sub-ADC, before being passed to the next stage as shown in Figure 2 [10].

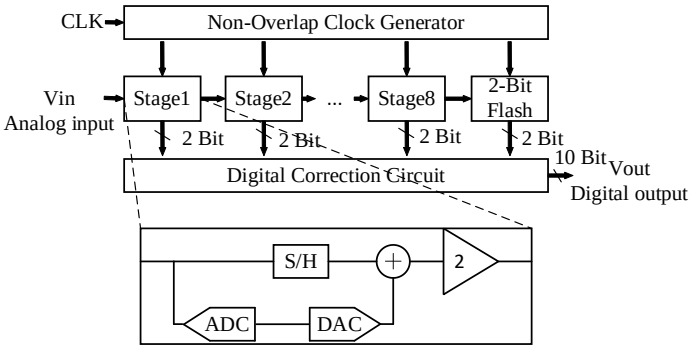

Figure 1. Pipelined ADC architecture

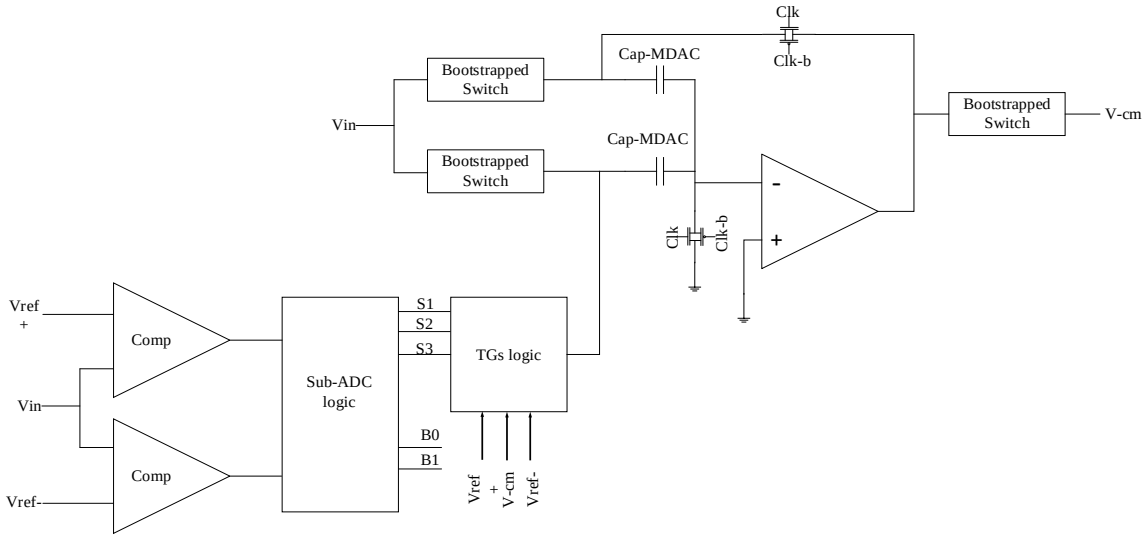

Figure 2. The 1.5-bit pipelined stage

3. DESCRIPTION OF THE 1.5/BIT ADC BLOCKS

3.1. Sub-ADC block

The sub-ADC block utilizes two differential clocked comparators. Both comparators receive the input signal, references, and common-mode voltage. To cancel the offset at the input, TG-CMOS switches and two capacitors (cap-in) are used [11]. Thus, those comparators offer amplification of the differential input voltage thanks to the preamplifier, which forms the first stage of each comparator. A regenerate latch works on the regeneration depending on the voltage difference between the two inputs [12], [13]. The last stage of our comparator design is the output buffer or post-amplifier, which has the purpose of converting the output of the decision circuit into a logic signal [14]. The proposed comparator scheme is represented in Figure 3. It is composed of three stages of a different nature, as indicated above, to be more insensitive to noise and process variations [15], [16].

Figure 4 shows the block diagram of each component in the comparator. The preamp (Figure 4(a)) amplifies the difference between the differential input signals and reduces kickback effects. A regenerative latch circuit is employed after the preamp to amplify this difference and should be capable of discriminating mV-level signals (Figure 4(b)). The last component is an RS-latch circuit (Figure 4(c)), which converts the output of the regenerative latch into a digital signal and keeps the comparator's output values fixed during the sampling phase. Only two comparators are used per stage, allowing for lower power consumption [17].

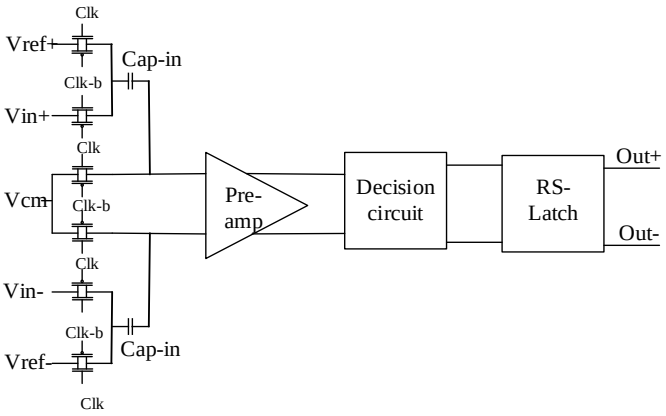

Figure 3. Schematic diagram of clocked comparator

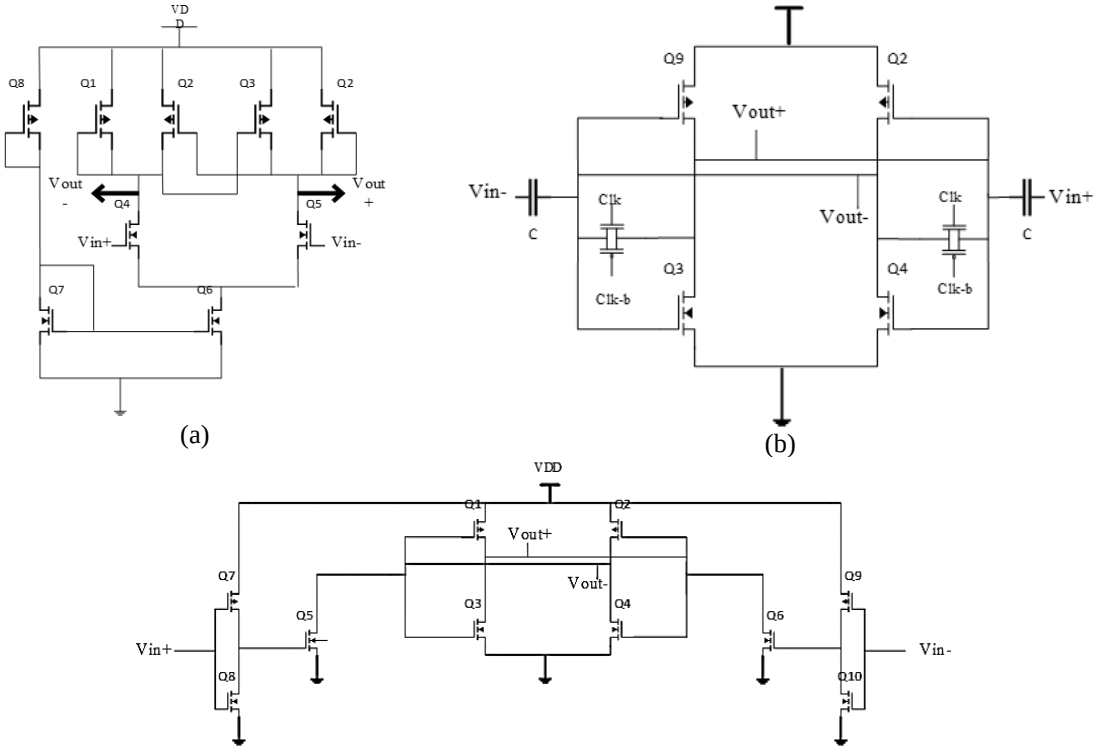

Figure 4. Blocks of the comparator: (a) preamp, (b) regenerative latch, and (c) RS-latch

Figure 5 displays the results of a transient analysis with a stop time of 700 ns, yielding a waveform. The output behavior under two conditions is shown:

- When Vinp > Vinn, output p discharges faster than output n
- When Vinp < Vinn, output n discharges faster than output p

The sub-ADC logic circuit receives the comparators' outputs for generating two types of outputs. S1, S2, and S3 are the control signals applied to various switches to supply the –VFS, + VFS, or 0 to the MDAC

circuit, while B1 and B0 are the digital bits delivered to the digital correction circuit. The truth table shown in Table 1 is used to constructing the logic circuit in Figure 6.

Two comparators are required to divide the input range into three sections. The comparator outputs will be latched by the sub-ADC logic. The input voltage range for the comparators varies between 0.4 V and 1.4 V, while the output voltage range is between 0 V and 1.8 V. The comparator decides when Φ2 is high, and both comparator latch outputs (outp, outm) are reset to VDD during Φ1. This results in the expected output sequence of 10101. The minimum input voltage required to decide, as determined from the overdrive test, is 2 mV. The proposed clocked comparator is estimated to consume 275.997 nW of power.

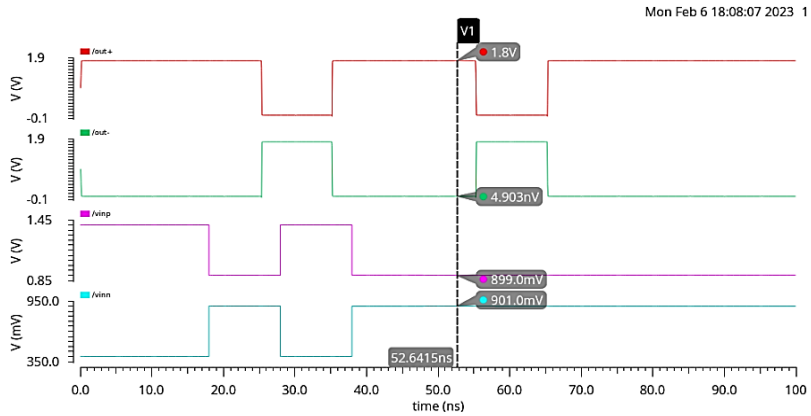

Figure 5. Transient response of comparator

Table 1. Sub-ADC logic circuit truth table

Inputs		Outputs			Output of stage
A1	A2	B1	B0	Control	
0	0	0	0	S3	Vout = 2Vin+Vfs
0	1	0	1	S2	Vout = 2Vin
1	1	1	0	S1	Vout = 2Vin-Vfs

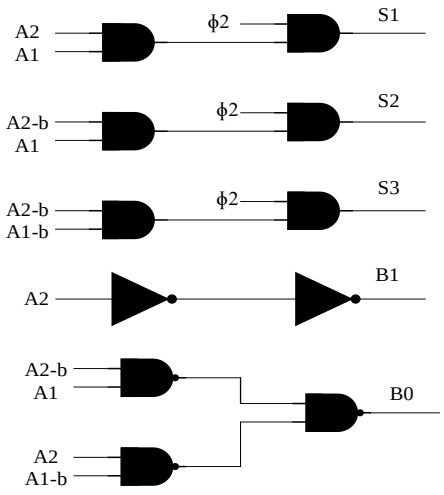

Figure 6. Sub-ADC logic circuit

3.2. MDAC block

Pipeline analog-to-digital converters demand operational amplifiers with high DC gain and a high unity gain frequency to attain accuracy and rapid settling times [18], [19]. A two-stage system is optimal for achieving this. Figure 7 demonstrates the complete implementation of a gain-boosted folded-cascode op-amp

in a fully differential configuration [20], [21]. The open-loop gain and unity gain frequency of the main op-amp are designed based on the gain error (GE) and settling error (SE) requirements specified by (1) and (2), respectively:

$$GE = \frac{1}{A\beta} < \frac{1}{4}LSB \quad (1)$$

$$SE = e^{-t/\tau} < \frac{1}{2}LSB \quad (2)$$

with β is called the feedback factor and $\tau = \frac{1}{2\pi f_{un}\beta}$ time constant.

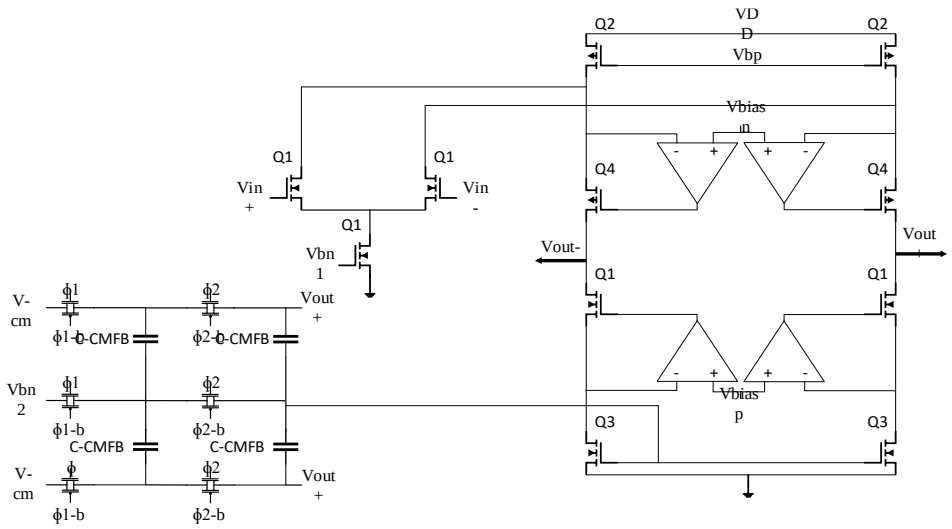

Figure 7. Schematic of gain-boosted amplifier

A gain-boosted operational amplifier (op-amp) will be used in a closed-loop configuration, so an NMOS differential pair is selected for the main input stage to minimize virtual ground parasitic effects. Figure 8 illustrates the gain-boosted auxiliary amplifiers which use in the two-stage fully differential OTA design. These op-amps are connected to the transistor gates at the cascode stage of the main op-amp in a negative feedback configuration. The auxiliary op-amp increases the main op-amp's output impedance and enhances its total gain. The unity-gain frequency of the gain-boosting op-amps must be higher than the -3dB frequency of the original op-amp and lower than the first non-dominant pole of the original op-amp. The type of input stage used depends on the input level: for high-level inputs, the NMOS input stage is used, and for low-level inputs, the PMOS input stage is used. Figures 8(a) and 8(b) show the auxiliary op-amps with PMOS and NMOS input stages, respectively [22], [23].

The gain-boosted folded-cascode op-amp circuit utilizes a dynamic CMFB circuit, to reduce static power usage and maintain the common-mode level of the output near the desired level during the amplification stage of the MDAC. However, caution must be taken in the choice of capacitors for the SC-CMFB, to ensure that they do not strain the main op-amp or experience charge injection from the switches [24]. The frequency response of gain-boosted auxiliary amplifiers is shown in Figure 9(a), which represents the NMOS-input stage, and Figure 9(b), which represents the PMOS-input stage. The gain-boosted op-amp's frequency response is presented in Figure 10. Table 2 summarizes the design specifications and achieved results.

Table 2. Op-amps AC response parameters

Parameter	Auxiliary amplifier NMOS	Auxiliary amplifier PMOS	Gain-boosted op-amp
DC-Gain (dB)	30.1	43.86	98.41
Unity-Gain Frequency (MHz)	197.54	124.47	191.98
Phase margin	59.37°	84.57°	55.067°

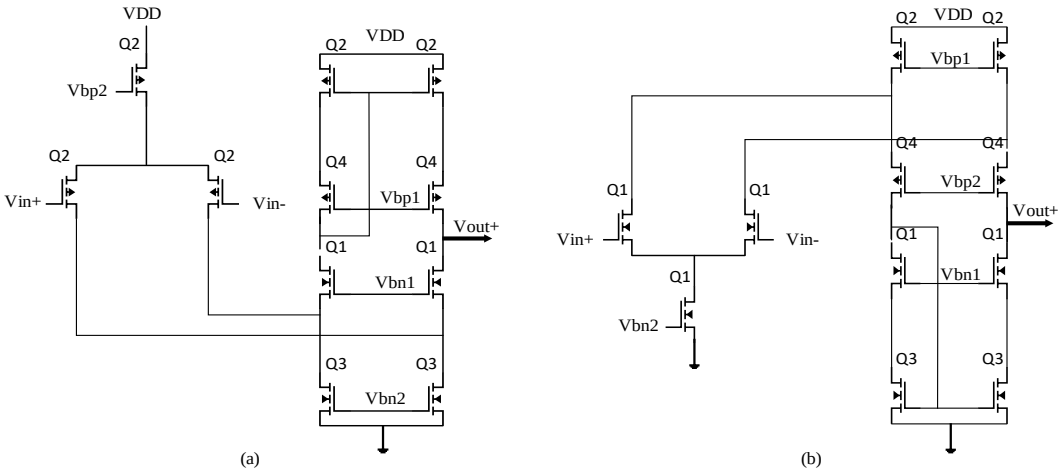

Figure 8. Gain-boosted auxiliary amplifiers (a) PMOS-input stage (b) NMOS-input stage

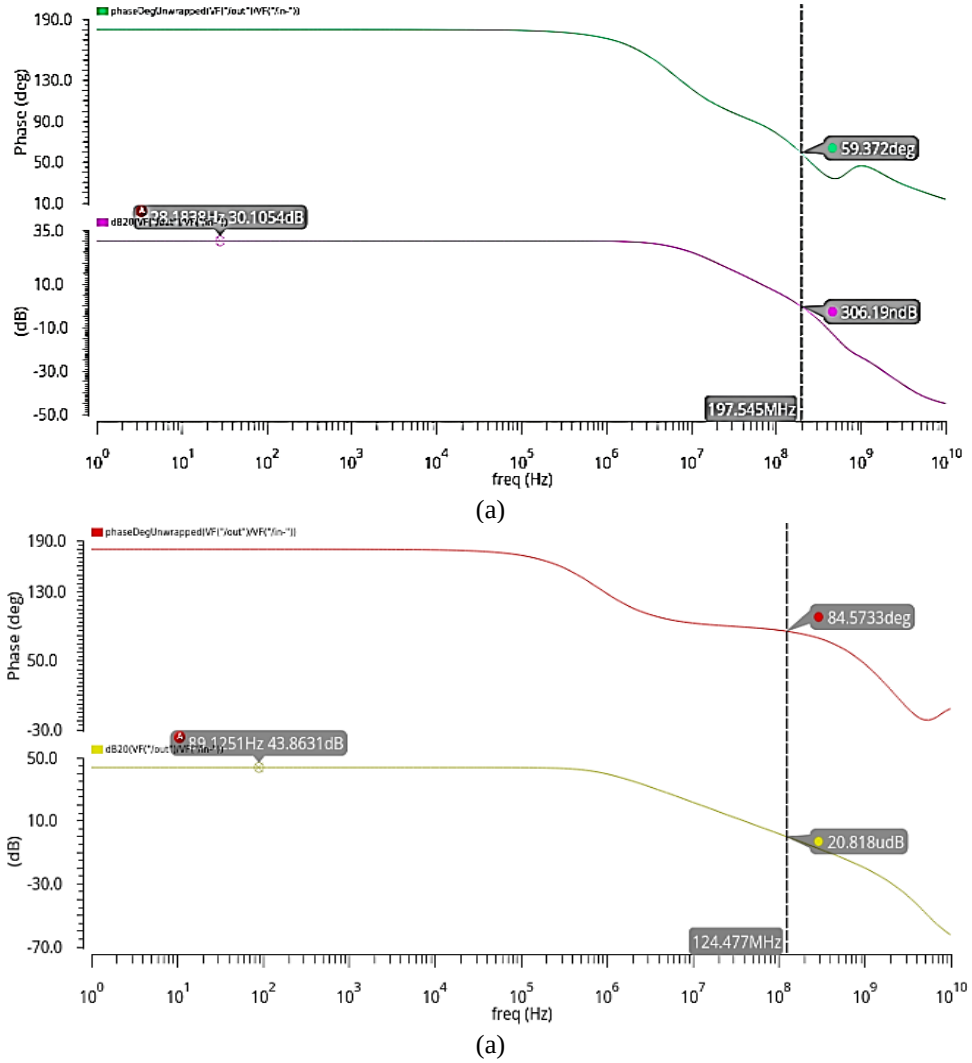

Figure 9. AC responses for gain-boosted auxiliary amplifiers: (a) NMOS-input op-amp and (b) PMOS-input op-amp

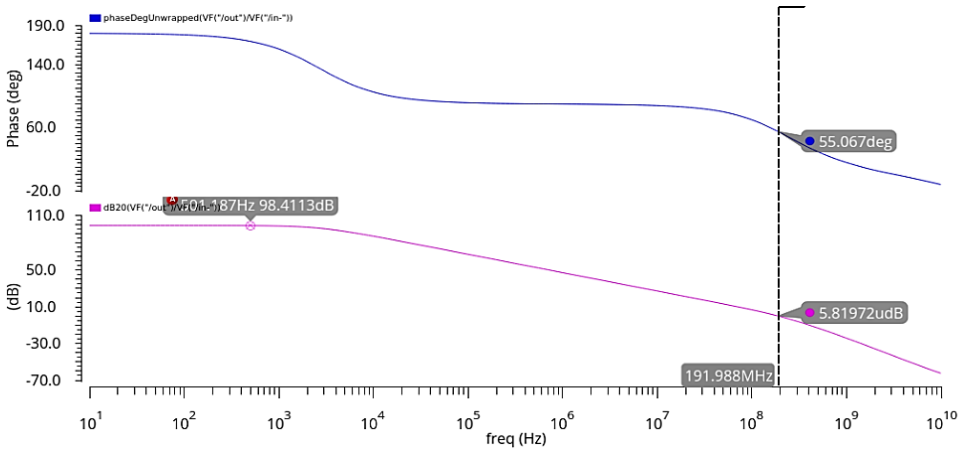

Figure 10. AC Responses for the gain-boosted op-amp

3.3. Switches

Figure 11(a) illustrates CMOS transmission gates (TGs). The advantage of using CMOS TGs is that they can transmit both high and low input values, unlike PMOS-only or NMOS-only switches. The TGs use reference voltages controlled by S1, S2, and S3 to transmit common-mode voltages for Op-amps. However, the TGs are not suitable for high-swing signals because the RON of the transistors depends on the input signal. This issue can be resolved using the "bootstrapping" circuit approach, which reduces the fluctuation of the switch RON in the presence of substantial input and output voltage variations [25]. The bootstrapped switch connects the feedback capacitor to the MDAC output and transfers the input signal to the MDAC block. As shown in Figure 11(b), the bootstrapped switch uses a capacitor to stabilize the VGS of the primary switch transistor (Q7) [26], [27].

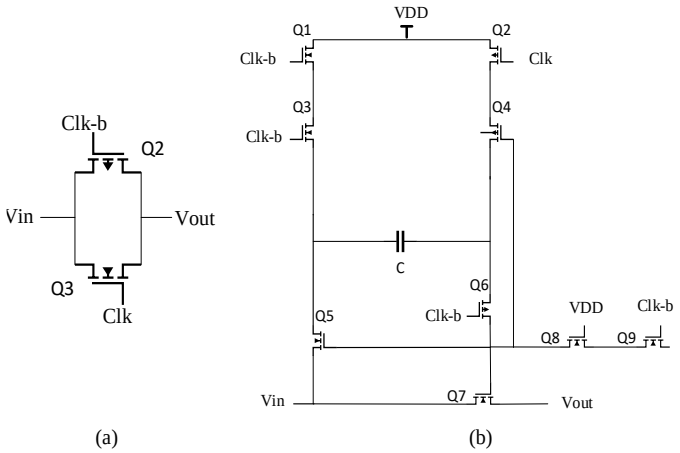

Figure 11. Switches (a) CMOS TG and (b) Bootstrapped switch

4. RESULTS AND DISCUSSION

A 1.5-bit/stage pipeline ADC has been designed in 90 nm technology using the Cadence tool, operating at a 100 MHz sampling frequency and a 1.8 V supply voltage. The 1.5-bit/stage design of the 10-bit pipeline ADC was optimized by considering W/L ratios, which were determined through analysis of the drain current equation in both the saturation and linear regions. The acquired data was utilized in the pipeline ADC, and a schematic diagram was generated using the Cadence tool.

The functioning of a 1.5-bit stage system with a sampling frequency of 100 MHz and an input signal of frequency f = (7/64)*fS, as depicted in Figure 12. The input signal is a pulse that varies from 0 V to 0.4 V. In the 2x gain mode, it is required that the amplifier output changes from 0 V to 0.8 V in one cycle.

According to the 64-point FFT spectrum of the output signal in 2x gain mode shown in Figure 13, under typical conditions (TT, VDD=1.8V, 27o), the effective number of bits (ENOB) is 9.756 bits and the Signal-to-Noise Ratio (SNR) is 60.495 dB. Table 3 displays the different amplitude values of the input signal. As the amplitude decreases, the SNR and ENOB decrease as the signal becomes weaker relative to the noise level.

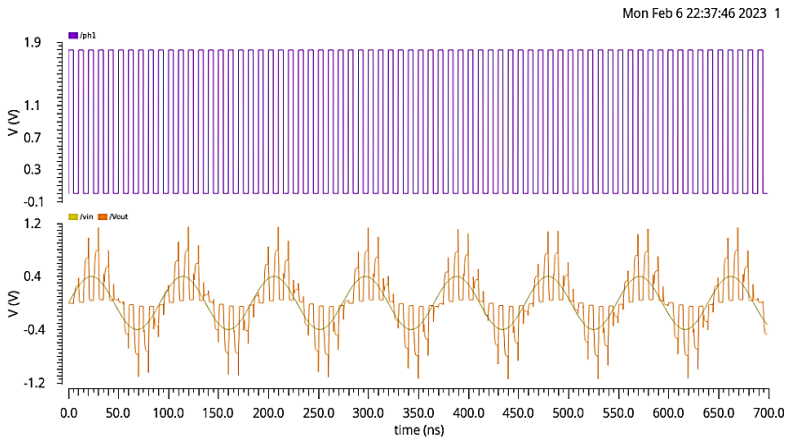

Figure 12. Transient simulation waveforms in 2x-gain mode

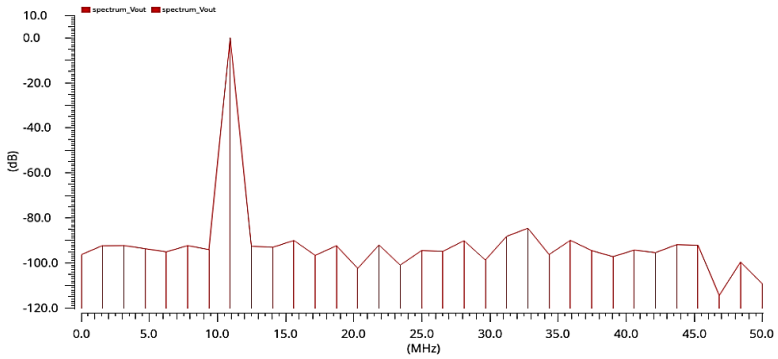

Figure 13. The output of the 2x-gain mode analyzed through a 64-point fast Fourier transform (FFT) to produce its spectrum

Table 3. Input signal vs ENOB and SNR

Input Amplitude (V)	ENOB (bits)	SNR (dB)
0.5	12.58	77.5
0.4	12.42	76.53
0.3	12.38	76.32
0.1	11.8	72.82

The simulation results for variations in PVT conditions have been tabulated in Table 4. It was found that the best results occurred in the typical case (TT, VDD = 1.8 V, 27o), while the worst cases were found in one case: FF, VDD = 1.8 V, 27o. The reason for this is that the biasing circuits were designed to keep the VDS of the cascode transistors low, resulting in many transistors having a VGS close to Vth. However, in the SS corner, an increase in Vth causes some of the cascode transistors to leave saturation, while in the FF corner, the opposite occurs.

The power consumption of a 1.5-bit stage is 1.632 mW. If we estimate the total energy usage of a 10-bit pipelined ADC to be 10 times that of a single stage, and its effective number of bits (ENOB) to be one bit less than the single stage, then the figure-of-merit (FOM) to be 0.297 pJ/conversion. Table 5 compares the proposed ADC with previous work.

Table 4. ENOB and SNR by means of PVT

	Typical Case	NN 1.8V		TT 27°		1.8V 27°	
		0	70°	1.7 V	1.9 V	FF	SS
ENOB (Bits)	12.42	12.68	12.23	12.49	12.68	11.68	12.78
SNR (dB)	76.53	78.12	75.41	76.97	78.15	72.11	79.25

Table 5. Comparison of the proposed ADC with previous work

References	Process (nm)	Bit	ENOB (bits)	Power (mW)	Speed (MHz)
[12]	28	12	9.97	-	1000
[9]	180	10	8.74	19.7	100
[11]	180	10	9.54	74.3	400
[16]	180	16	12.49	374	120
This work	90	10	12.68	16.32	100

5. CONCLUSION

The paper describes the design and analysis of a 1.5-bit/stage pipeline ADC with a 100 MHz sampling frequency for a CMOS image sensor. The ADC was built using 90 nm CMOS technology and operates at 1.8 V. The comparators were clocked at 2 mV, leading to a higher resolution. CMOS transmission gates and bootstrapped switches were used for improved signal transmission. The gain-boosted op-amp used in the ADC has a DC gain of 98.41 dB and a unity-gain frequency of 191.98 MHz. The ADC was found to have an ENOB of 12.42 bits, a power consumption of 1.632 mW, and a FOM of 0.297 pJ/conv. The ADC was found to be well suited for use with the CMOS image sensor.

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BIOGRAPHIES OF AUTHORS

Aicha Menssouri received the M.S degree in Micro-Electronics Signals and Systems, and pursuing her study in Ph.D. in electrical engineering from the University of Sidi Mohamed Ben Abdellah, Fez, Morocco, in 2019 and 2023, respectively. Her research study is a CMOS image sensor. She can be contacted at email: aicha.menssourii@usmba.ac.ma.

Karim El Khadiri is a Professor in Superior Normal School, ENS-FEZ, Morocco. He received his Master degree since 2011 in Micro-Electronics and Ph.D. degrees since 2017 in FSDM, USMBA, Fez, Morocco. His research interests include Li-Ion battery charger interface (BCI) and BMS, RFID passive and active tags, CMOS mixed mode integrated circuit design, integrated class-D power output stage and renewable energy. He can be contacted at email: karim.elkhadiri@usmba.ac.ma.

Ahmed Tahiri received the graduate degree DES in Department of Physics, Sidi Mohammed Ben Abdellah University, Morocco in 1997, received the Ph.D. degree in physics from the University Sidi Mohamed Ben Abdellah, Faculty of Science, Morocco in 2005. He completed his doctoral studies in didactics of science in the University of Sherbrooke in Canada in 2010. He is now a professor in Superior Normal School, ENS-FEZ, Morocco. His research interests include Li-Ion battery charger interface (BCI) and BMS, RFID passive and active tags, CMOS mixed mode integrated circuit design. He can be contacted at email: ahmed.tahiri@usmba.ac.ma.