Experimental validation of quadratic-boost-zeta converter based on coat circuit

Ahmed Mahmood Ali, Turki Kahawish Hassan
Department of Electrical Engineering, College of Engineering, Mustansiriyah University, Baghdad, Iraq

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ABSTRACT

This work proposed a high step-up DC-DC converter with a voltage gain of 12 at a duty cycle of 48.25% with a single active switch. The new design combines the quadratic-boost converter and an isolated zeta converter with a single-stage coat circuit by a transformer with a trans ratio of 2.3. This can result in low voltage stress on switch and diodes with low conduction losses without using an additional clamp circuit, which in turn causes an increase in total efficiency. It has continuous and low ripples in the input and output currents. The voltage conversion ratio and the component voltage stresses are calculated in continuous conduction mode (CCM). The prototype was constructed and tested practically while considering an input voltage of 30 V, an input power of 240 W, an output voltage of 360 V, and a switching frequency of 100 kHz to validate the theoretical evaluations. The maximum efficiency at maximum output power is 94.5%.

Corresponding Author:

Ahmed Mahmood Ali
Department of Electrical Engineering, College of Engineering, Mustansiriyah University
Falastin St, Baghdad, Iraq
Email: ahmedmahmood19862022@uomustansiriyah.edu.iq

1. INTRODUCTION

Because of worries about the environment and a lack of fossil fuels, photovoltaics (PV) and other forms of renewable energy are becoming more popular worldwide [1]–[4]. However, the performance of a PV panel depends on several variables, such as temperature, the amount of sunlight, and the amount of shade. As a result, the voltage of a PV panel is typically around 12-60 volts; thus, a high step-up voltage is required to supply energy to the AC grid or DC microgrid [5]–[9]. A conventional boost converter with a very high-duty cycle operation can produce a high step-up voltage. However, the voltage of the main switch will increase, it must have a large on-resistance, and an increased cost is required. Additionally, issues with the diode's reverse recovery, electromagnetic interference, and conduction losses will accompany the used high-duty cycle and cause more loss, decreasing efficiency.

Many ideas have been put forward to get a high step-up voltage, such as using switched capacitors, voltage multipliers (VMs) or coat circuits, cascade structures or stack structures, transformers, and coupled inductors. Some converters use switched capacitors to boost voltage, but these converters have three significant drawbacks: i) The output voltage ratio is dependent on the number of stages of switched capacitors; ii) The input current is large and pulsating, and the current is significant overshoot through the capacitors; and iii) The converters needed two or more switches, which make the circuit and drive are complex [10]–[12]. The converters used by voltage multiplier techniques, providing high-voltage gain, have been presented while simultaneously lowering the voltage on the switches; however, when utilizing multi-stage converters, the high charging currents cause a significant conduction loss when passing through the converter switch [13]–[16]. To create powerful step-up converters, magnetic coupling is often used. A higher turn ratio will result in a higher voltage gain. But the leakage inductance of the connected inductor or the transformer can cause high voltage spikes in the switches, which can cause high voltage stress, increase size, and decrease efficiency [17]–[22]. The other approach suggested in [23], [24] uses cascading or stacking. The converters can be connected in series or parallel to increase voltage gain. The cascade or stack converter uses three or more converters to improve the voltage gain. Due to its many converters, the cascade or stack converter also requires numerous components and has low efficiency.

Furthermore, in [25]–[27] A new approach has been proposed in the DC-DC converter by combining two or more conventional transformers, in [25] has successfully combined flyback and SEPIC topologies, but the profit is still small and requires an increase in the duty cycle, as the result increase loss. The work of [26] shows that the boost converter has been improved and the profit is fairly good, but it requires two keys, which makes controlling it complex and increases costs and losses. Also, in [27] has successfully combined quadratic boost and SEPIC topologies but to increase voltage gain should be increased duty cycle and used to switch.

High step-up converters based on zeta converters are suggested in [28]. In the circumstances described above, it would be good to combine the advantages methods, i.e., the stacking, cascading layers, and voltage multipliers, together while maintaining high voltage gain without reducing the converter's efficiency [29]. This research draws from the abovementioned works and presents a high step-up converter by combining stacking and cascading configurations of two well-known quadratic boost and isolated zeta converters with a single stage based on a coat circuit. This converter gets the benefits of both quadratic-boost and isolated zeta converters, which is low input and output current ripples. Additionally, the proposed converter only needs one active switch, and the voltage stress on the switch and the diodes are much lower than the output voltage. Therefore, switches with low on-resistance and low voltage drop diodes can be used.

2. THE STRUCTURE AND OPERATION PRINCIPLE OF THE PROPOSED CONVERTER

The proposed converter is shown in Figure 1. It combines quadratic boost and isolated zeta converters with a single-stage of coat circuit, making it a relatively simple structure. The quadratic-boost converter is composed of an input source $\mathrm{V_{in}}$, one inductor ($\mathrm{L_1}$), one transformer with magnetizing inductance($\mathrm{L_M}$), three diodes ($\mathrm{D_1}$, $\mathrm{D_2}$, and $\mathrm{D_3}$), two capacitors ($\mathrm{C_1}$ and $\mathrm{C_5}$), and one switch (SW). The zeta converter with a single-stage of coat circuit is composed of two diodes ($\mathrm{D_4}$ and $\mathrm{D_5}$), four capacitors ($\mathrm{C_2}, \mathrm{C_3}, \mathrm{C_4}$, and $\mathrm{C_6}$), and two inductors ($\mathrm{L_2}$ and $\mathrm{L_3}$). One of the characteristics of the converter that distinguishes it is that the input and output ports are connected to an inductor($\mathrm{L_1}$ and $\mathrm{L_3}$); this may help explain why the proposed converter can have a low ripple current from both the input and output ports.

Before the analysis, the following assumptions are made: i) All of the parts in the circuit are assumed to be ideal; ii) Since the inductors and capacitors are sufficiently large, their current and voltage ripples can be ignored; and iii) The transformer ratio(n) is equal to $\frac{N_S}{N_P}$ .Assuming the symbol N_p represents the number of turns of the primary transformer, and the symbol N_s Represents the number of turns of a secondary transformer.

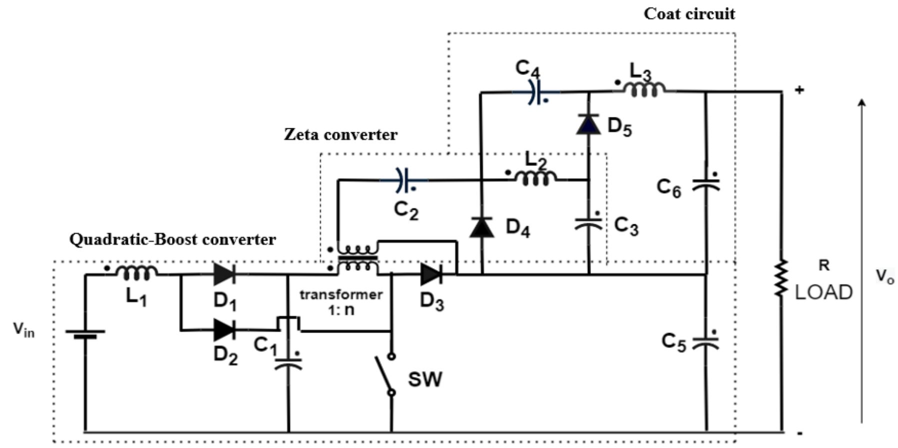


Figure 1. The proposed converter circuits

There are two operating stages for the continuous conduction mode (CCM). The following gives a detailed examination of the converter at (CCM).

- Stage 1: Figure 2(a) shows that the switch SW and the diode D_2 are turned ON, the Diodes D_1, D_3, D_4, and D_5 are turned OFF. The voltage source V_{in} charges the inductor L_1 through the diode D_2 and the switch SW, the energy stored in the capacitor $C_1$is transferred to the inductor L_M, and the energy stored in the capacitors(C_1, C_2) are transferred to the inductor L_2. Also, the energy stored in the capacitors ($C_1$and, $C_{2,}$ and C_4) is transferred to the inductor L_3 and the capacitor C_6. The capacitors $C_1.C_2.C_4$ and C_5 are delivering power to the load. Consequently, the currents through the inductances i_{L1}, i_{L2}, and i_{L3} increase linearly. During this stage, the capacitors C_3 and C_6 are charged, and the capacitors C_1, C_2, C_4, and C_5 are discharged. The inductances L_1, L_M, L_2, and L_3 are charged. The following equation is used to obtain inductors voltages:

$$V_{L1} = V_{in} \tag{1}$$

$$V_{LM} = V_{C1} \tag{2}$$

$$V_{L2} = nV_{C1} + V_{C2} - V_{C3} \tag{3}$$

$$V_{L3} = nV_{C1} + V_{C2} + V_{C4} - V_{C6} \tag{4}$$

- Stage 2: Figure 2(b) shows that the diodes D_1, D_3, D_4, and D_5 are turned ON, the diode D_2 and the switch SW is turned OFF. The voltage source V_{in} and the inductor L_1 charge the capacitor C_1, the capacitor C_5 charged by the voltage source V_{in}, the inductors L_1 and L_M through the diode D_3, also through the diode D_4, the inductor L_M charge the capacitor C_2, and also the inductor charges the capacitor C_4 through diode D_5 and the capacitor C_3. The inductor L_2 charges the capacitor C_4 through the diode D_5. Finally, the inductor L_3 and the capacitor C_3 are delivering power to the load with the capacitor C_6. Hence, the currents through these inductances i_{L1}, i_{L2}, and i_{L3} are decreasing linearly. Also, during this stage, the capacitors C_1, C_2, C_4, and C_5 are charged, and the capacitors C_3 and C_6 are discharged. The inductances L_1, L_M, L_2, and L_3 are discharging.

$$V_{L_1} = V_{in} - V_{C_1} \tag{5}$$

$$V_{LM} = V_{C_1} - V_{C_5} \tag{6}$$

$$V_{L2} = -V_{c3} = -V_{C_4} \tag{7}$$

$$V_{L3} = V_{c3} - V_{c6} \tag{8}$$

$$V_{sec} = -V_{c2} = n(V_{c1} - V_{c5}) \tag{9}$$

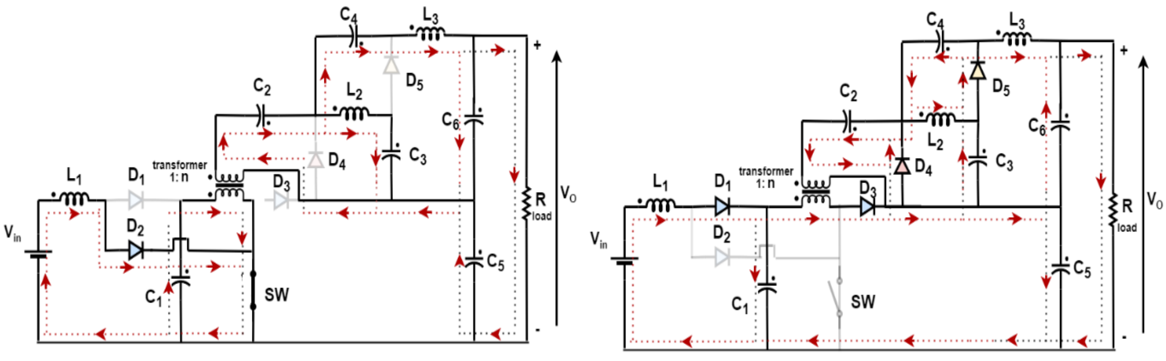


Figure 2. Operation stages and the current direction for the proposed converter (a) stage 1 and (b) stage 2

3. STEADY STATE ANALYSIS DURING CCM

3.1. Voltage gain calculation

By applying the voltage-sec balance principle on L_1, L_M, L_2, and L_3, and using (1), (2), (3), (4), (5), (6), (7), and (8). The (10)-(14) can be obtained:

$$V_{C1} = \frac{V_{in}}{(1-D)} \tag{10}$$

$$V_{C5} = \frac{V_{in}}{(1-D)^2} \tag{11}$$

$$V_{C4} = V_{C3} = \frac{nDV_{in}}{(1-D)^2} \tag{12}$$

$$V_{C6} = \frac{2nDV_{in}}{(1-D)^2} \tag{13}$$

$$V_o = V_{c5} + V_{c6} \tag{14}$$

The (10), (11), (12), and (13) are derived as follows.

$$\int_0^{DT} V_{L1}\,dt + \int_{DT}^{T} V_{L1} dt = 0$$
$$V_{in} * D + (V_{in} - V_{C1}) * (1-D) = 0$$
$$V_{C1} = \frac{V_{in}}{(1-D)}$$
$$\int_0^{DT} V_{LM}\,dt + \int_{DT}^{T} V_{LM} dt = 0$$
$$V_{C1} * D + (V_{C1} - V_{C5}) * (1-D) = 0$$
$$\frac{V_{C5}}{V_{C1}} = \frac{1}{(1-D)} \rightarrow V_{C5} = \frac{V_{in}}{(1-D)^2}$$

$$\int_0^{DT} V_{L2} dt + \int_{DT}^{T} V_{L2} dt = 0$$
$$(nV_{c1} + V_{C2} - V_{C3}) * D + (-V_{C3}) * (1-D) = 0$$
$$(nV_{c1} * D + V_{C2} * D - V_{C3} = 0$$
$$(nV_{c1} * D - n(V_{c1} - V_{c5}) * D - V_{C3}) = 0$$
$$\frac{V_{C4}}{V_{C1}} = \frac{V_{C3}}{V_{C1}} \frac{nD}{(1-D)} \rightarrow V_{C4} = V_{C3} = \frac{nDV_{in}}{(1-D)^2}$$

$$\int_0^{DT} V_{L3}\,dt + \int_{DT}^{T} V_{L3} dt = 0$$
$$(nV_{C1} + V_{C2} + V_{C4} - V_{C6}) * D + (V_{c3} - V_{c6}) * (1-D) = 0$$
$$(nV_{c1} * D + V_{C2} * D + V_{C3} - V_{C6}) = 0$$
$$(nV_{c1} * D + -n(V_{c1} - V_{c5}) * D + V_{C3} - V_{C6}) = 0$$
$$\frac{V_{C6}}{V_{C1}} = \frac{2nD}{(1-D)} \rightarrow V_{C6} = \frac{2nDV_{in}}{(1-D)^2}$$

So, the final equation of the converter's gain is (15).

$$M = \frac{V_0}{V_{in}} = \frac{1+2nD}{(1-D)^2} \tag{15}$$

In (15) is the voltage gain M of the proposed converter.

3.2. Voltage and current stress calculation on switch SW and diodes

The voltage stress imposed on the switch SW, the diodes D_1, D_2, D_3, $D_{4.}$ and D_5 can be represented by the symbols V_{SW}, V_{D1}, V_{D2}, V_{D3}, V_{D4}, and V_{D5}; $respectively$, according to Figure 2, the (16)-(21) can be obtained:

$$\left.\begin{aligned} V_{SW} &= V_{c5} \\ V_{SW} &= \frac{1}{(1-D)^2} V_{in} \end{aligned}\right\} \tag{16}$$

$$\left.\begin{aligned} V_{D1} &= V_{c1} \\ V_{D1} &= \frac{1}{(1-D)} V_{in} \end{aligned}\right\} \tag{17}$$

$$\left.\begin{aligned} V_{D2} &= V_{c5} - V_{c1} \\ V_{D2} &= \frac{D}{(1-D)^2} V_{in} \end{aligned}\right\} \tag{18}$$

$$\left.\begin{aligned} V_{D3} &= V_{c5} \\ V_{D3} &= \frac{1}{(1-D)^2} V_{in} \end{aligned}\right\} \tag{19}$$

$$\left.\begin{aligned} V_{D4} &= nV_{c1} + V_{c2} \\ V_{D4} &= nV_{c1} - n(V_{c1} - V_{c5}) \\ V_{D4} &= nV_{c5} \\ V_{D4} &= \frac{\boldsymbol{n}}{(\boldsymbol{1-D})^{\boldsymbol{2}}} V_{in} \end{aligned}\right\} \tag{20}$$

$$\left.\begin{aligned} V_{D5} &= -V_{c3} + nV_{c1} + V_{c2} + V_{c4} \\ V_{D5} &= nV_{c1} - n(V_{c1} - V_{c5}) \\ V_{D5} &= nV_{c5} \\ \mathrm{V_{D5}} &= \frac{n}{(1-D)^2} V_{in} \end{aligned}\right\} \tag{21}$$

Assuming that the converter is efficient at 100% makes the analysis easier. The average current I_{L1} at the input is, thus.

$$\left.\begin{aligned} P_{in} &= P_{out} \\ V_{in} * I_{L1} &= V_O * I_0 \\ I_{L1} &= \frac{1+2nD}{(1-D)^2} I_o \end{aligned}\right\} \tag{22}$$

To simplify the diodes' average current calculation, the ripple was neglected. They can be obtained as (23)-(27).

$$I_{Tp} = (1 - D) I_{L1} \tag{23}$$

$$I_{D2} = D \frac{1+2nD}{(1-D)^2} I_o \tag{24}$$

$$I_{D1} = \frac{1+2nD}{(1-D)} I_o \tag{25}$$

$$I_{D3} = I_{D4} = I_{D5} = I_{L2} = I_{L3} = I_O \tag{26}$$

$$I_{SW} = I_{D2} + I_{Tp} - I_O \tag{27}$$

4. PARAMETERS DESIGN

4.1. Design of inductors

In practical uses, the current ripple is always predetermined. As a result, the inductance of the inductors L_1, L_M, L_2, and L_3 may be found by using the (28)-(31). Consequently, the inductances must be suitable for continuous inductor current mode operation.

$$\left.\begin{aligned} V_{in} &= \mathrm{L}_1 \frac{\Delta i_{L1}}{DT} \\ \mathrm{L}_1 &\geq \frac{V_{in} * D}{\Delta i_{L1} * f} \end{aligned}\text{from on state}\right\} \tag{28}$$

$$\left.\begin{aligned} V_{C1} &= L_M \frac{\Delta i_{LM}}{DT} \\ \mathrm{L}_1 &\geq \frac{V_{in} * D}{\Delta i_{L1} * f} \end{aligned}\text{ from on state}\right\} \tag{29}$$

$$\left.\begin{aligned} V_{C3} &= \mathrm{L}_2 \frac{\Delta i_{L2}}{(1-D)T} \\ \mathrm{L}_2 &\geq \frac{n * V_{in} * D}{\Delta i_{L2} * f * (1-D)} \end{aligned}\text{from on state}\right\} \tag{30}$$

$$\left.\begin{aligned} V_{C6} - V_{C4} &= \mathrm{L}_3\ \frac{\Delta i_{L3}}{(1-D)T} \\ \mathrm{L}_3 &\geq \frac{n*V_{in}*D}{\Delta i_{L3}*f*(1-D)} \end{aligned}\right\} \text{from on state} \tag{31}$$

4.2. Design of capacitances

In practical uses, the voltage ripple is always predetermined. As a result, the capacitance of the capacitors C_1, C_2, C_3, C_4 C_5 and C_6 can be obtained as (32)-(36).

$$\left.\begin{aligned} I_{c1-on} &= I_{TP} = (1-D)I_{L1} = \mathrm{C}_1\ \frac{\Delta \mathrm{V}_{\mathrm{C}1}}{\mathrm{DT}} \\ \mathrm{C}_1 &\geq \frac{\mathrm{I}_{\mathrm{L}1}*D(1-D)}{\Delta \mathrm{V}_{\mathrm{C}1}*\mathrm{f}} = \frac{D}{\Delta \mathrm{V}_{\mathrm{C}1}*\mathrm{f}}\frac{1+2nD}{(1-D)}\ I_o \end{aligned}\right\} \tag{32}$$

$$\left.\begin{aligned} I_{c5-on} &= I_O = \mathrm{C}_5\ \frac{\Delta \mathrm{V}_{\mathrm{C}5}}{\mathrm{DT}} \\ \mathrm{C}_5 &\geq \frac{I_O*D}{\Delta \mathrm{V}_{\mathrm{C}5}*\mathrm{f}} \end{aligned}\right\} \tag{33}$$

$$\left.\begin{aligned} I_{c2-on} &= I_{L2} + I_{L3} = 2I_0 = \mathrm{C}_2\ \frac{\Delta \mathrm{V}_{\mathrm{C}2}}{\mathrm{DT}} \\ \mathrm{C}_2 &\geq \frac{2*I_O*\mathrm{D}}{\Delta \mathrm{V}_{\mathrm{C}2}*\mathrm{f}} \end{aligned}\right\} \tag{34}$$

$$\left.\begin{aligned} I_{c3-on} &= I_{L2} = I_O = \mathrm{C}_3\ \frac{\Delta V_{\mathrm{C}3}}{\mathrm{DT}} \\ \mathrm{C}_4 &= \mathrm{C}_3 \geq \frac{I_O*\mathrm{D}}{\Delta V_{\mathrm{C}3}*\mathrm{f}} \end{aligned}\right\} \tag{35}$$

$$\left.\begin{aligned} \mathrm{C}_6 * \Delta \mathrm{V}_{c6} &= 0.5 * \frac{\mathrm{T}}{2} * \frac{\Delta I_{\mathrm{L}3}}{2} \\ \mathrm{C}_6 &\geq \frac{\Delta \mathrm{I}_{\mathrm{L}3}}{8*\mathrm{f}*\Delta V c6} \end{aligned}\right\} \tag{36}$$

5. COMPARISON OF THE DESIGNED CONVERTER WITH OTHER CONVERTERS

The suggested converter is compared to current topologies in [19], [20], [22] and [29], which also produce significant voltage gains. Table 1 details the voltage gains and the normalized equations that characterize the voltage stresses. In addition, the number of diodes and switches used in each equivalent circuit is also provided. To ensure that comparisons are valid, the turns ratio (n) is consistently defined as 2. In [19], [20], and [22], the need for two active switches leads to low efficiency because of conduction losses and complex controlling methods. Even though the displayed topology consists of a single switch and a simple method for controlling it, it still needs a lot of diodes. Also, in [29], the voltage stress on the output diode and the switch is higher than in the proposed structure. A low current ripple can extend the service life of renewable energy sources; thus, it is essential to consider that at the input [30]. The topology in [19] has a large ripple in the input and output currents. Also, the input ripple current on the input side of the boost converter is less because it has an input inductor. Also, the output inductor of the zeta converter is one of the components that help reduce the ripple current on the output side. So, the proposed converter is different compared with the other converter structure.

Table 1. Comparison between the proposed converter and other converters

Topologies	[19]	[22]	[20]	[29]	Proposed converter
Number of diodes	3	6	4	5	5
Number of switches	2	2	2	1	1
Gain	$\frac{2+(n(2-D))}{1-D}$	$\frac{1+2n(1-D)}{(1-D)^2}$	$\frac{1+D+2n}{1-D}$	$\frac{1+nD}{(1-D)^2}$	$\frac{1+2nD}{(1-D)^2}$
Switch voltage	$\frac{V_o}{2+(n(2-D))}$	$\frac{V_o}{1+(2n(2-D))}$	$\frac{V_o}{1+D+2n}$	$\frac{V_o}{1+nD}$	$\frac{V_o}{1+2nD}$
Voltage stress on outer diode	$\frac{(1+n)V_o}{2+n*(2-D)}$	$\frac{2n(1-D)V_o}{1+(2n(2-D))}$	$\frac{(1+n)V_o}{1+D+2n}$	$\frac{n}{1+nD}\ V_o$	$\frac{n}{1+2nD}\ V_o$
Input current ripple	High	Low	low	low	low
Output current ripple	High	Low	low	low	very low

6. EXPERIMENTAL RESULTS

A 240 W experimental prototype has been constructed to test the aforementioned theoretical study's validity, as shown in Figure 3. Table 2 illustrates the values and device type of the used components by considering the current ripple of each inductor as $\Delta i_{L1,2,3} = 30\%$ of $i_{\mathrm{L1,2,3}}$, and the voltage ripple of each capacitor as $\Delta V_{c1,6} = 1\%$ of $\mathrm{V_{C1,6}}$, $\Delta V_{c2,3,4,5} = 0.84$ % of $\mathrm{V_{C2,3,4,5}}$.

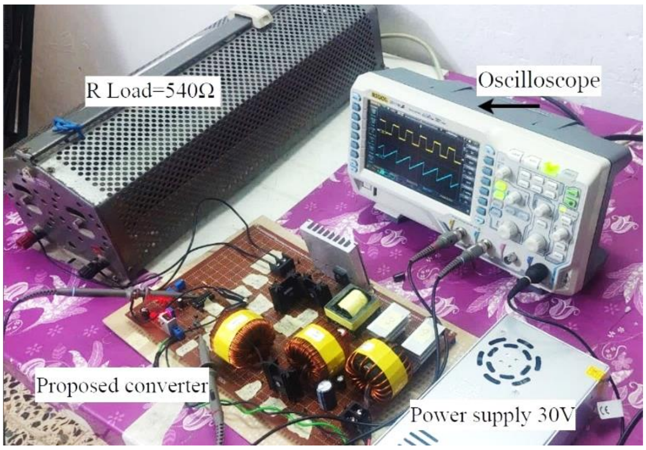


Figure 3. Shows the proposed converter, power supply, R load, and oscilloscope in the laboratory

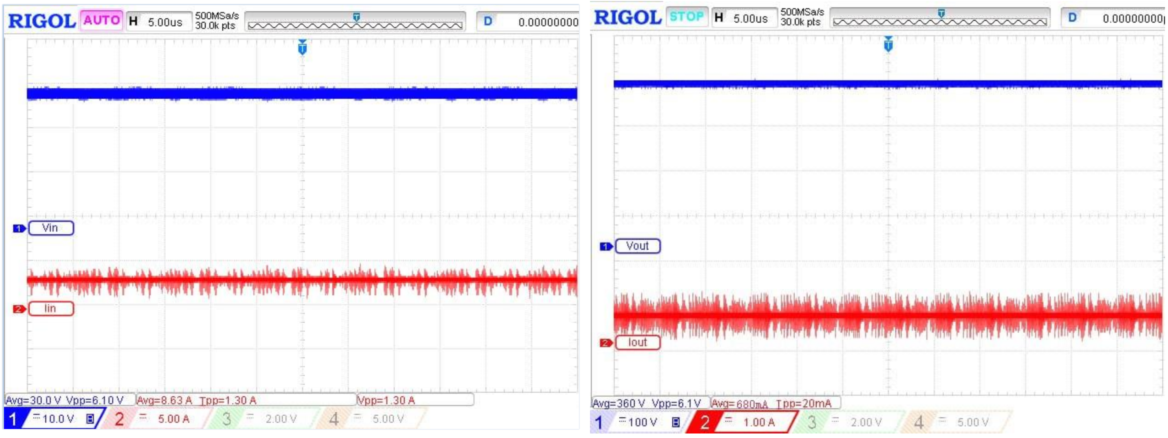
Table 2. The parameters and device types of the proposed converter

Parameter	Value	Device	Type
L_1	$63*10^{-6}$ H	Diodes (D_1, D_2, D_3)	STPS30150CT
$L_{2.3}$	$3*10^{-3}$ H	Diodes (D_3)	MBR30200
C_1	$33.3*10^{-6}$ F/100V	Diodes (D_4, D_5)	MBR30600
C_5	$3.3*10^{-6}$ F/240V	Switch (SW)	IRFP460
C_2	$6.6*10^{-6}$ F/240V		
$C_{3.4}$	$3.3*10^{-6}$ F/480V		
C_6	$0.1*10^{-6}$ F/480V		
Transformer magnetizing inductance (L_m)	$87*10^{-6}$ H		
Load resistance(R)	540 ohms		
Frequency (f)	100 kHz		
Input voltage(V)	30 V		
Output voltage(V)	360V		
Trans. Ratio(n)	2.3		

The experimental voltage and current waveforms of the suggested converter for the input voltage of 30 V are shown in Figures 4–9. The gate pulses of the MOSFETs and closed-loop control are produced by the IC TL494, and the switch operates at a duty cycle of 48.25% to achieve the output voltage of 360 V. Besides that, the experimental waveforms were measured using a Rigol DS1104Z oscilloscope.

The experimental waveforms of input voltage $\mathrm{V_{in}}$ and input current i_{in} are shown in Figure 4(a), and the average input voltage and current are around 30V and 8.63 A, respectively. Also, the experimental waveforms of output voltage $\mathrm{V_o}$ and output current i_{o} are shown in Figure 4(b), and the average output voltage and output current are around 360 V and 0.68 A, respectively.

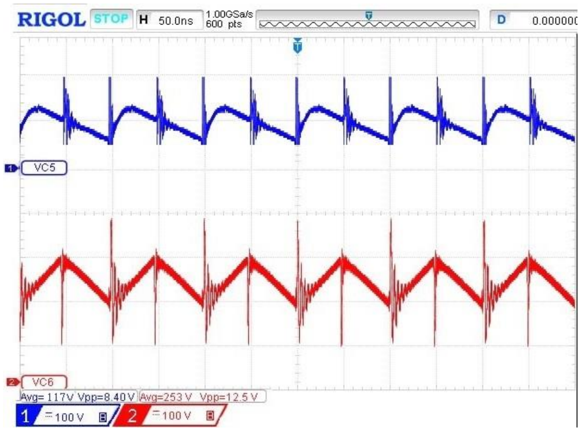
Figure 5 illustrates the voltage for the capacitors C_1, C_2, C_3, C_4, C_5, and C_6. The experimental results of $\mathrm{V_{c1}} = 56.6$ V, $\mathrm{V_{c2}} = 132$ V, $\mathrm{V_{c3}} = 133$ V, $\mathrm{V_{c4}} = 132$ V, $\mathrm{V_{c5}} = 117$ V, and $\mathrm{V_{c6}} = 253$ V are sufficiently near to the theoretical results that are as: $\mathrm{V_{c1}} = 57.97$ V, $\mathrm{V_{c2}} = 124.3$ V, $\mathrm{V_{c3}} = 124.3$ V, $\mathrm{V_{c4}} = 124.3$ V, $\mathrm{V_{c5}} = 112$ V, and $\mathrm{V_{c6}} = 248.6$ V. Figure 6 illustrates the voltage stress and current through the diodes D_1, D_2, D_3, and D_4. The experimental results of $\mathrm{V_{D1}} = 58.4$ V, $\mathrm{V_{D2}} = 67.2$ V, $\mathrm{V_{D3}} = 145$ V , $\mathrm{V_{D4}} = 286$ V and $\mathrm{V_{D5}} = 285$ V, and the average current of $\mathrm{I_{D1}} = 4.6$ A, $\mathrm{I_{D2}} = 4.6$ A, $\mathrm{I_{D3}} = 0.9$ A , $\mathrm{I_{D4}} = 0.85$ A and $\mathrm{I_{D5}} = 0.68$ A. The measurements and waveforms for the current and voltage are shown in the figure, showing that the effect of the leakage inductance of the transformer on the diodes was observed to be minor, and the results are close to their equations. Consequently, all of the voltages agreed with the theoretical assessments.



(a) (b)

Figure 4. The waveforms of input and output voltage and input and output current: (a) input voltage and current and (b) output voltage and current

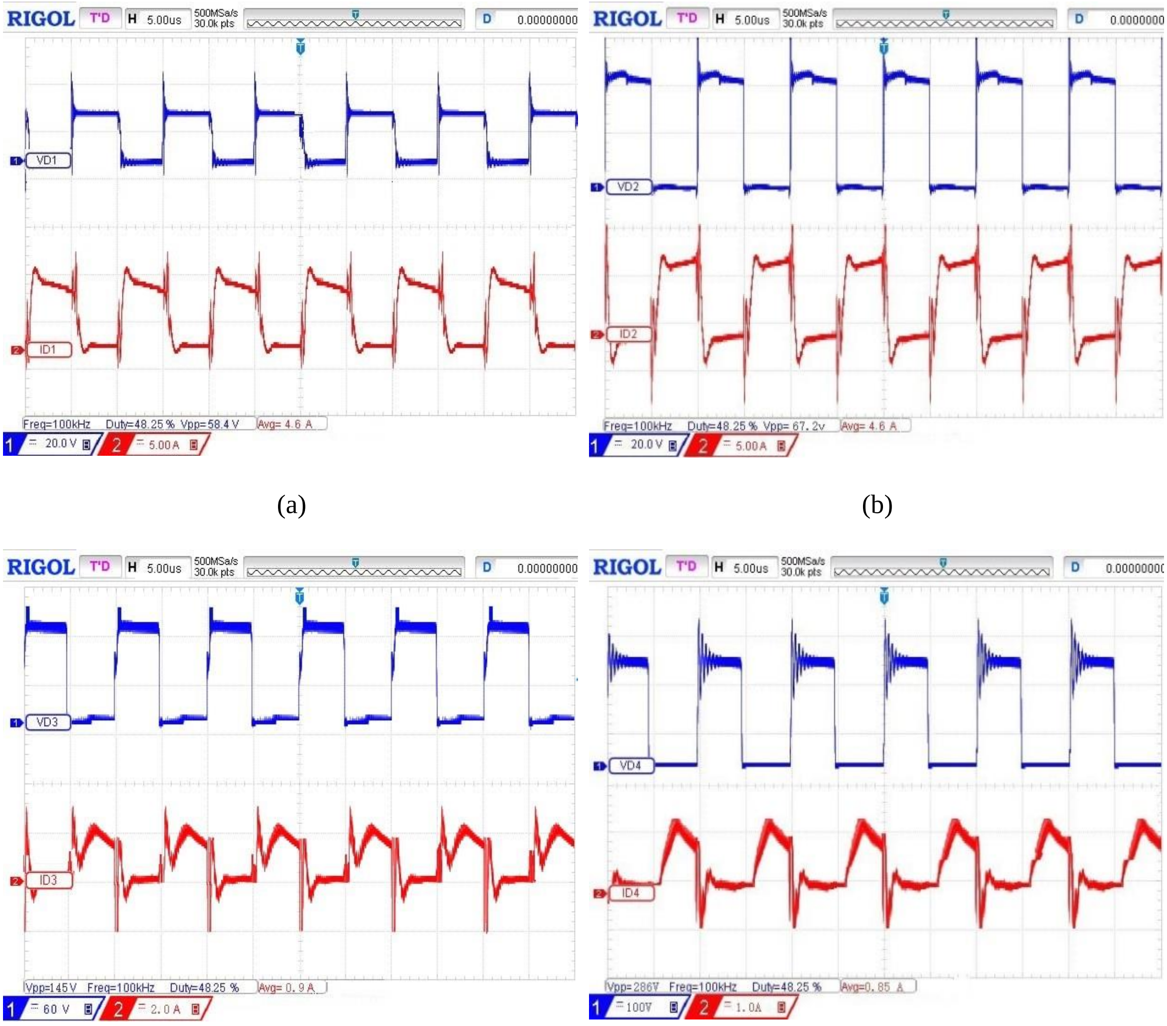
(a) (b)



(c)

Figure 5. The waveforms of voltage for the capacitors: (a) for the capacitors C_1 and C_2, (b) for the capacitors C_3 and C_4, and (c) for the capacitors C_5 and C_6

The voltage stress and average current of the switch SW are 125 V and 8.33 A, respectively, which are illustrated in Figure 7. Also, the voltage spikes it very small in the switch voltage, and its value is much lower than the output voltage. This means that low-voltage MOSFETs with low ON-state resistance can increase the converter's efficiency. Also, the results agreed with the theoretical assessments.



(a) (b)

(c) (d)

Figure 6. The waveforms of voltage and current for the diodes: (a) for the diode D_1, (b) for the diode D_2, (c) for the diode $D_{3,}$ and (d) for the diode D_4

Figure 8 illustrates the peak-to-peak voltage and current passing through the primary and secondary of the transformer. The voltage is about $v_{ti} = 120$ V and $v_{to} = 285$ V . The measurements and waveforms for the current and voltage are shown in the figure, showing that the effect of the leakage inductance of the transformer was observed to be minor. The desired voltage gain was reached for all cases, thus validating the theoretical evaluation. Assuming the symbol v_{ti} the peak-to-peak voltage for the primary transformer, and the symbol v_{to} represents the peak-to-peak voltage for the secondary transformer.

Finally, the converter was tested when the input voltage changed. Figure 9 shows the input and output voltage waveforms when the input voltage changes from 30 to 25 volts using a closed-loop circuit based on the IC TL494, and the output voltage (V_o) maintains its reference value.

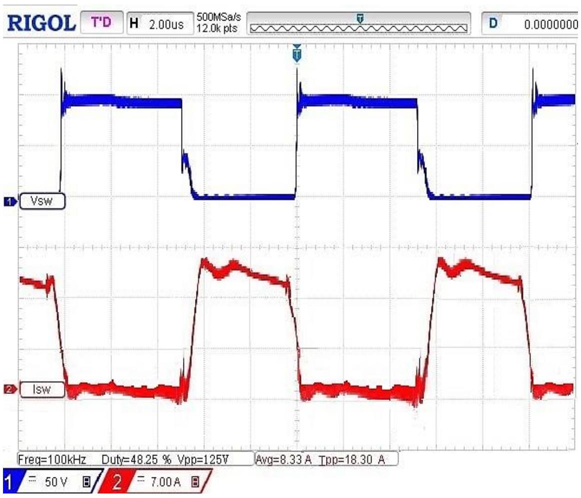
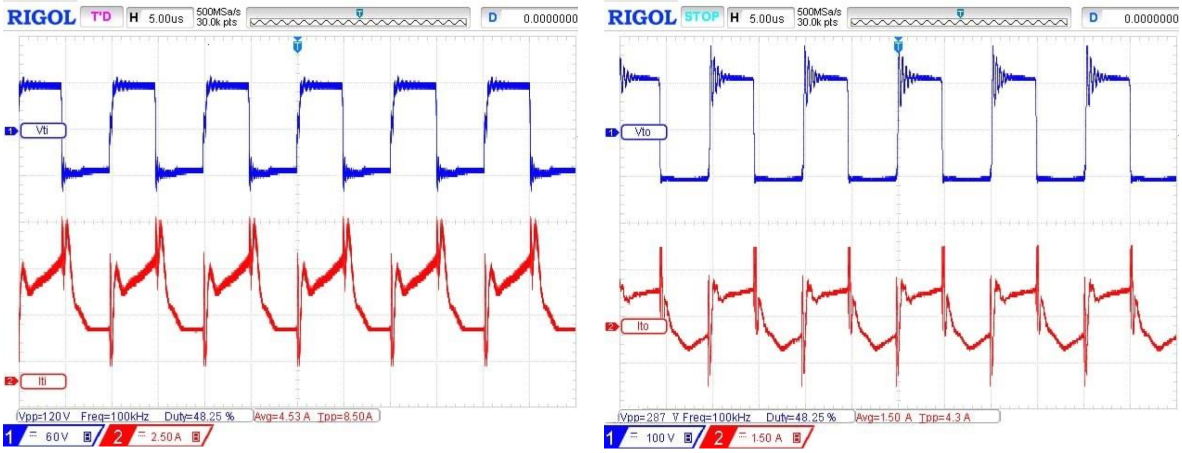


Figure 7. The waveforms of the voltage and the current for the switch (SW)



(a) (b)

Figure 8. The waveforms of the voltage and current for the transformer: (a) primary and (b) secondary

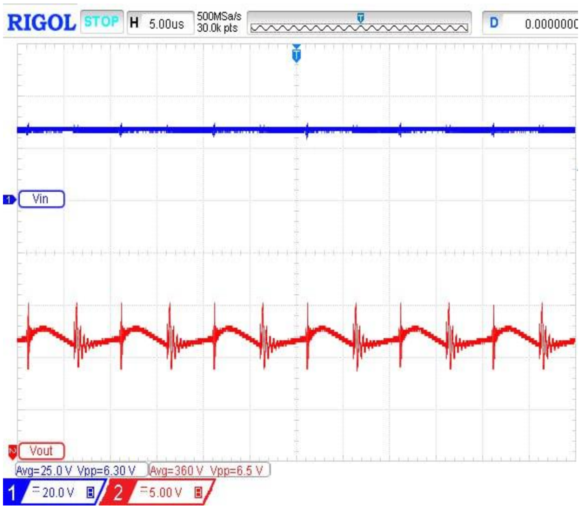


Figure 9. Converter response (output and input voltage when changing the input voltage from 30 to 25 V)

7. CONCLUSION

In this study, a transformer with a trans ratio of 2.3 successfully combines a quadratic-boost converter and an isolated zeta converter with a single stage of the coat circuit. This simplifies the circuit topology and results in a high step-up voltage gain for renewable energy applications. The voltage gain was 12 times more than the input and output voltage of roughly 360 V at 48.25% of the duty cycle. The circuit was studied, designed, and tested practically with an output power of 240 watts, an input voltage of 30 volts, and a frequency of 100 kHz. As a result, a high step-up voltage gain, one switch without a snubber circuit, low voltage across the diodes and switch, continuous input and output current, very low input and output current ripple, and the use of MOSFETs with low on-resistance lowers cost and loss, resulting high efficiency of (94.5%).

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BIOGRAPHIES OF AUTHORS

Ahmed Mahmood Ali was born in 1986. He received B.Sc. in Electrical Engineering in 2010 from the Electrical Engineering Department, College of Engineering, University of Kufa, Iraq. He is pursuing a master's study at Al-Mustansiriyah University, College of Electrical Engineering, Baghdad, Iraq. His research interests include Power Electronics & Electrical Machines. From 2014 to now, he was a chief engineer in the Ministry of Education. He can be contacted at email: ahmedmahmood19862022@uomustansiriyah.edu.iq.

Turki Kahawish Hassan was born in 1959. He received B.Sc. in Electrical Engineering in 1982, an M.Sc. in Electrical Engineering/Power Electronics Specialization in 1991, and a Ph.D. in electrical engineering power electronics in 2005 from the Electrical Engineering Department, College of Engineering, University of Baghdad, Iraq from 1983-2005 he worked in Electrical Engineering Design Centre as a designer for DC-AC Converters, and AC-DC Converters. From 2006 to now, he was a lecturer for power electronics in the Electrical Engineering Department, College of Engineering, Mustansiriyah University. He was a professor in 2020. His research interests include modular multilevel converters, high-frequency DC-DC converters, AC drive systems, and grid-connected photovoltaic systems. He has published 27 journal articles and 5 international conference articles. He can be contacted at email: turki_k.eng@uomustansiriyah.edu.iq.