CHB multilevel inverter with sliding mode controller for DSTATCOM applications

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Article Info

ABSTRACT

In this article, the robust nonlinear controller for cascaded H-bridge-based distributed static compensator (DSTATCOM) with input-output linearization and sliding mode control scheme using an improved voltage balancing scheme is presented. The feedback linearization method and sliding mode control scheme are used to cancel nonlinearities and deal with invariant stability due to mathematical modeling uncertainties due to DSTATCOM parameter and external load disturbance. The improved voltage balancing is used to balance the voltages of the DC side capacitor of DSTATCOM. The complete simulation studies are out to validate the control scheme based on the improved voltage balance integrated with sliding mode control under disturbances caused by the load changes and DSTATCOM parametric changes. The performance characteristics of the DSTATCOM with sliding mode controller are tested using the MATLAB/Simulink platform.

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1. INTRODUCTION

Currently, most of the electrical energy is processed through the power electronics-based converter system. The endless usage of power electronics converters creates reactive current and harmonics problems in the utility. The harmonics current caused by the power electronics converter creates a disturbance to the sophisticated electronics equipment [1]. Especially, the rectifier based on the diode and thyristor is used to decrease the power factor and dislocation factor of the source current. The nonlinear loads are main causes of harmonics in distribution system, these harmonics are main cause of low power factor and increases of prize electricity. In addition to this, the harmonics current leads to the overheating of the transformer, failure of the cable, torque pulsation, and derating of the adjustable speed drives. Traditionally, the harmonics current caused by the nonlinear load is eliminated with a passive filter based on the inductor and capacitor. However, the passive filter-based method is suffered from series/parallel resonance, aging problems and fixed VAR generations [2]. The harmonics current caused by the non-linear load damage the power factor correction capacitors used in an electrical line of the power system.

The harmonics current caused by the non-linear load is varying dynamically. However, the passive filter is not able to eliminate dynamically varying harmonics current [3]. In most cases, the two-level active power filters (APF) were used for reactive current demand and harmonic current elimination of the non-linear load. However, a two-level inverter-based APF is employed for low power rating and a medium power rating filter with two-level active power filters is realized with the passive filter or through a transformer [4]. Then the system of the distributed static compensator (DSTATCOM) becomes bulky and complex.

Moreover, the two-level voltage source inverter-based DSTATCOM is not appropriate for medium and high-power function, due to the limitation of device rating.

The concept of the multilevel inverter is the addition of a few switching devices and a capacitor to achieve higher power and voltage rating of the inverter [5]. The MLI-based DSTATCOM is used for better recompense characteristics in low and high-power applications. The neutral point clamped inverter seems to be a better suitable topology for the DSTATCOM because of the availability of a common DC bus. Initially, the neutral point clamped (NPC) converter based on the diode clamped inverter is most widely used, because of the requirement of two diodes and four switching devices in the leg for the three-level inverter [6]. However, the NPC based on the diode clamped converter suffers from a high number of blocking diodes, unequal ratings of the switching devices, unequal capacitor voltages and unequal distribution of switching losses. The NPC based diode clamped inverter acts as active neutral point clamped ANPC converter. It presents the increased number of freedoms as compared to the diode clamped converter. In addition to this, the three-level active NPC inverter has better loss distribution and equal voltage stress across the switching devices of the inverter [7]. The APF based on the NPC inverter is adopted in this article. The active filter is a shunt-connected device used for compensation of harmonics caused by the non-linear load. The active filter is also known as a distributed static compensator. The DSTATCOM is the family of custom power devices used for the compensation of voltage and current harmonics caused by the nonlinear load [8]. The realization of the DSTATCOM becomes easier due to the development of the semi-conductor and digital electronics controllers.

Many control schemes had in the literature for the control of DSTATCOM. Among all control schemes such as power balance, synchronous reference frame, instantaneous reactive power (IRP) theory, symmetrical component (SC) theory and synchronous reference frame (SRF) and IRP theory are most widely reported for DSTATCOM control [9]. The soft based on type-1, type-2 fuzzy logic controller and neural network-based approach are also used for DSTATCOM control [10]. The reference current computation with the SRF scheme is the most efficient control technique for DSTATCOM. In IRP theory, all the three-phase instantaneous quantities are transformed into the bi-phase quantities for the computation of the active and reactive power of the control scheme. Subsequently, these calculated active and reactive powers are used for further computation of the reference currents for the DSTATCOM [11]. The calculated reference current is fed to the pulse width modulator to generate the switching pulses for the semi-conductor devices to track the desired source currents [12], [13]. The current harmonics eliminated by using IRP theory in distribution system. However, the computation of the harmonics active power demands the low pass filter in the control unit of the DSTATCOM [14]. The low pass filter-based techniques require a rigorous tuning process for its parameter tuning and adjustment of the same. There is no systematic method is available for parameter adjustment of the PI controller used in the SRF. In this article, the SMC is integrated with a SRF for the computation of the harmonics' active power of the control unit. The reference current after computation is fed to the pulse generating system to trace the required current with the DSTATCOM. The complete simulation study of the DSTATCOM is carried out with MATLAB/Simulink simulation with Sim power system using power electronics block sets. The different control based on conventional voltage balance scheme with PI-SRF and an improved voltage balance scheme with SMC based SRF modeled using the control system of Simulink library. The simulated response shows the effectiveness of compensation characteristics of the DSTATCOM for the elimination of harmonics cause by the load.

2. CONFIGURATION OF DSTATCOM TOPOLOGY

The complete electrical power system network with DSTATCOM is shown in Figure 1. The DSTATCOM system consists of electrical sources, the power circuit of DSTATCOM and load. Three phase sources having phase displacement 120°. The power circuit of DSTATCOM is realized with eleven IGBTs in each leg, three interfacing inductors and three DC link capacitors. The non-linear load is realized with three commutation inductors, and six diode bridges with a resistive-inductive load on its DC side. Generally, the nonlinear load is made up of three phase diode rectifier bridge with R-L load or R-C load.

2.1. Control scheme

The function of the CHB-DSTATCOM is used to compensate for the harmonics and reactive requirement of the load. The compensation currents of DSTATCOMs are estimated with a synchronous reference frame. The PI controller is used for controlling DSTATCOM and compensating harmonics. The error voltage signals directly processed by the PI controller are modulated with carrier signals. Nevertheless, due to the absence of the loop of inner current control, the direct power control method results in an overshoot of current. The current overshoot mechanism activates the protection circuit of the DSTATCOM.

The high current caused by the inappropriate control can damage the power and driver circuits of DSTATCOM. Thus, control scheme based on two loops is used in this manuscript. However, the control

scheme based on SRF has two loops; the outer loop is used for the control of voltage and the inner loop for current control. The estimated reference currents errors of the control scheme are computed based on the direct and quadrature component of the current. These current references compute based on direct and quadrature components are compared with the measured actual current to obtain the errors in current. The errors obtained from the current loop are processed through the proportional and integral controller to derive the desired direct and quadrature component of currents. The multilevel inverter-based DSTATCOM is highly nonlinear with different voltages and multiple switching to achieve multiple outputs within a single cycle of the source. The tuning of the proportional and integral controller for the highly nonlinear multilevel inverter-based DSTATCOM is a complex task. The tuning of PI controllers for two sets of the inner control loops is a more complex and tedious process. Hence, to reduce the parameter tuning of the proportional and integral controller, a control scheme with DC link voltages is controlled with an improved voltage balancing scheme using proportional and integral controllers, and the inner current controller is regulated with SMC control [9] and as shown in Figure 2.
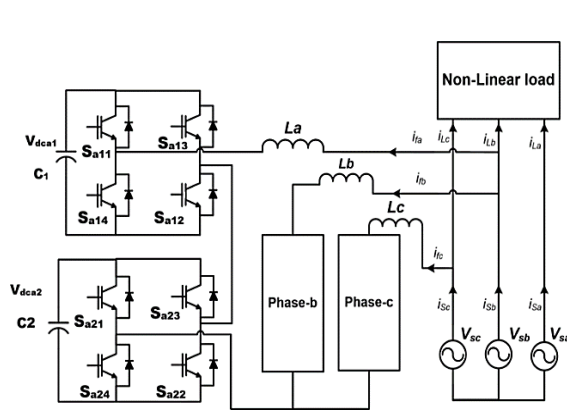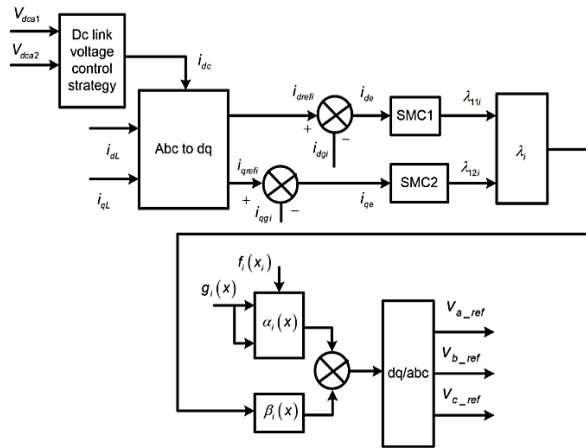

Figure 1. DSTATCOM topology

Figure 2. Real and reactive power control with SMC-based control scheme

The improved two-loop PI control-based control scheme decreases the difficulty [15]–[20]. The multilevel inverter-based DSTATCOM is highly coupled with nonlinearity and multivariable structure. Additionally, the PI controller-based control scheme is sensitive to system limitation variations and requires a complete mathematical model of the structure. Hence, the feedback linearization technique can be used to transform the coupled nonlinear structure into the decoupled linear system. The feedback linearization is as follows. The DSTATCOM power system is presented in Figure 1. The dynamic mathematical model as given (1) and (2).

$$v_{dinv_i} - R_{f_i}i_{dg_i} - L_{f_i}\frac{di_{dg_i}}{dt} + \omega_i L_{f_i}i_{qg_i} - v_{dg_i} = 0 \tag{1}$$

$$v_{qinv_i} - R_{f_i}i_{qg_i} - L_{f_i}\frac{di_{qg_i}}{dt} + \omega L_{f_i}i_{dg_i} - v_{qg_i} = 0 \tag{2}$$

Consider the dynamic state-space model representation given as (3).

$$\frac{dx_i}{dt} = f_i(x_i) + g_i(x_i)u_i \tag{3}$$

By rearranging (1) and (2) into (3) with and as state variables, the coupled and nonlinear dynamic equations can be converted into the decoupled linear system.

$$f_i(x) = \begin{bmatrix} -\frac{R_{f_i}}{L_{f_i}}i_{dg} + \frac{X_{f_i}}{L_{f_i}}i_{qg_i} - \frac{1}{L_{f_i}}v_{dg_i} \\ -\frac{R_{f_i}}{L_{f_i}}i_{qg_i} + \frac{X_{f_i}}{L_{f_i}}i_{dg_i} - \frac{1}{L_{f_i}}v_{qg_i} \end{bmatrix}$$

$$g_i(x) = \begin{bmatrix} \frac{1}{L_{f_i}} & 0 \\ 0 & \frac{1}{L_{f_i}} \end{bmatrix} x_i = \begin{bmatrix} i_{d_i} \\ i_{q_i} \end{bmatrix} u_i = \begin{bmatrix} v_{dinv_i} \\ v_{qinv_i} \end{bmatrix} \tag{4}$$

From (4), it can be concluded that there is a hypothetical decoupling existing between the currents and after linearization of the data the system as a whole can also be expressed as (5).

$$\lambda_i = A_i(x_i) + B_i(x_i)U_i \tag{5}$$

In (5)'s control input for the DSTATCOM switching operation can be expressed as (6).

$$U_i = \left(-B_i^{-1}(x_i) * A_i(x_i)\right) + \left(B_i^{-1}(x_i) * \lambda_i\right) or U_i = \alpha_i(x_i) + \beta_i(x_i)\lambda_i \tag{6}$$

Were

$$\alpha_i(x) = \left(-B_i^{-1}(x_i) * A_i(x_i)\right) and \beta_i(x_i) = B_i^{-1}(x_i)$$
$$B_i(x_i) = \begin{bmatrix} g_{i_{11}}(x_i) & 0 \\ 0 & g_{i_{22}}(x_i) \end{bmatrix} A_i(x_i) = \begin{bmatrix} f_{i11}(x_i) \\ f_{i21}(x_i) \end{bmatrix} \tag{7}$$
$$\lambda_i = \begin{bmatrix} \lambda_{i11}\lambda_{i_{12}} \end{bmatrix}^T = \begin{bmatrix} \frac{di_{dg_i}}{dt} & \frac{di_{qg_i}}{dt} \end{bmatrix}^T$$

In this work, the DSTATCOM is working in active and reactive power regulation mode, and the output states are taken as (8).

$$Y_i = \begin{bmatrix} i_{dg_i} i_{qg_i} \end{bmatrix}^T \tag{8}$$

3. ADOPTION OF SLIDING MODE CONTROL

To apply the feedback linearization technique effectively, if the precise mathematical model of the system is identified. On the other hand, the parameter variation makes the system more complex and difficult. Moreover, the DSTATCOM based on a multilevel inverter has many switching, different voltage sources and parameter variations in a single cycle [21]–[25]. The accurate mathematical model and prevailing nonlinearity make the system more complex. Further, the system parameter and operating point are subjected to variation in the given course of time. However, the developed mathematical system cannot represent an accurate model of the system. To alleviate this, a sliding mode controller is combined with a control scheme. In the sliding mode controller, the equilibrium points and sliding surface are computed in every instant and the controller is operated around the sliding surface and equilibrium operating point.

3.1. Constitution of stability criterion and sliding surface

Once SMC is integrated into the controller, the state vector is transformed into a new state vector via the linearization process, producing a new control input. The corresponding control and switching control components of the SMC are denoted in (9). Switching control is used to minimize the error brought on by operating changes and parameter variation while the linearization procedure is utilized to compute the equivalent control.

$$U_i(t) = U_{i_{eq}}(t) + U_{i_{sw}} = U_{ieq}(t) + \rho_i . tanh(\sigma_i) \tag{9}$$

Where ρ is used to representing a positive constant and σ is used to represent the sliding surface. The sliding surface is defined to obtain the satisfactory operation of the controller. The sliding surfaces, namely σ_{i1} and σ_{i2} are to be defined, since (9) has two output states i_{dg_i} and i_{qg_i}. The state variable for the second-order system and the sliding surface $\sigma_i(t)$ can be given as (10).

$$\sigma_i(t) = \frac{der_i(t)}{dt} + K_i er_i(t) \tag{10}$$

Where K_i is used to represent the positive constant and $er_i(t)$ is used to represent the error in the output. In this paper, the relative degree of i_{dg_i} and i_{qg_i} is considered as 1 and the error in the utility current is taken as

a sliding surface. Hereafter, $\sigma_{i_1} = er_{i1} = i_{dg_i} - i_{dref_i}$ and $\sigma_{i_2} = er_{i2} = i_{qgi} - i_{qrefi}$. The σ_1 and σ_2 are the elements of sliding surface matrix σ and can be given as (11).

$$\sigma_i = [\sigma_{i1} \quad \sigma_{i2}] \tag{11}$$

The Lyapunov function with the sliding surface matrix can be represented as (12).

$$G_i = \frac{1}{2}\sigma_i{}^2 \tag{12}$$

As per the Lyapunov stability criterion, "if the function G_i is a positive definite function and its derivative function, i.e., $\frac{dG_i}{dt}$ is a negative definite function, then the system is said to be asymptotically stable".

$$i.e., \frac{dG_i}{dt} = \sigma_i \dot{\sigma}_i{}^T < 0, \tag{13}$$

To fulfill the condition $\sigma_i \dot{\sigma}_i{}^T < 0$ $\dot{\sigma}_i$ can be represented as $\rho \ tanh(\sigma)$.

$$\dot{\sigma}_{i1} = -\rho_{i1} \ tanh(\sigma_{i1}) \ and \dot{\sigma}_{i2} = -\rho_{i1} \ tanh(\sigma_{i2}) \tag{14}$$

Substituting (11) into (14).

$$\dot{\sigma}_{i1} = -\rho_{i1} \ tanh(i_{dgrefi} - i_{dgi}) \ and \dot{\sigma}_{i2} = -\rho_{i1} \ tanh(i_{qgrefi} - i_{qgi}) \tag{15}$$

With the attained new dynamics using SMC, the state vector can be given as (16).

$$\lambda_{i1} = \begin{bmatrix} \lambda_{i11} \\ \lambda_{i12} \end{bmatrix} = \begin{bmatrix} \rho_{i1} \ tanh(i_{dgrefi} - i_{dgi}) \\ -\rho_{i1} \ tanh(i_{qgrefi} - i_{qgi}) \end{bmatrix} \tag{16}$$

i_{dgrefi} and i_{qgrefi} can be found from (3). If the variations of the parameter of the Satcom, then the corresponding change in the system matrix is ΔA_i, and the system can be represented as (17).

$$\dot{X}_i = (A_i + \Delta A_i)X_i + B_i(U_{ieq} + U_{isw}) \tag{17}$$

$$\dot{X}_i = A_i X_i + B_i U_{ieq} + \Delta A_i X_i + B_i \rho_i \ tanh(\sigma_i) \tag{18}$$

The system parameter dependence part $\Delta A_i X_i$ is compensated with the switching part $B_i \rho_i \ tanh(\sigma_i)$. Therefore, the boundary condition for the selection of ρ is:

$$B_i \rho_i > \Delta A_i X_i \ or p_i > [B_i^{-1} \Delta A_i X_i] \tag{19}$$

Where ρ represents a positive constant and is used to cancel out the error caused by the parameter deviations, operating point variations and disturbances caused by the load. The value of ρ should be large, which results in smooth transition action $tanh(\sigma)$ into a hard switching function. The hard switching results in chattering in the output. However, the very small value ρ is not able to cancel the variation caused by the parameter and operating point dependencies. Additionally, the small value ρ will cause slow response.

4. DC VOLTAGE BALANCING

The voltage balancing scheme of the CHB-based DSTATCOM is shown in Figure 3 and Figure 4 respectively. The conventional scheme of voltage balancing consists of individual balancing and average balancing. Individual balancing is used for regulating each capacitor voltage. The average balancing is used for balancing and regulating each leg's voltages of the CHB DSTATCOM. The proposed scheme of voltage regulation of CHB-based DSTATCOM is shown in Figure 4. The scheme consists of individual balancing and average balancing. The individual balancing is used to estimate the maximum value of the capacitor voltage and compare it with a reference voltage. Each time maximum value capacitor voltage changes and this is repeated until the voltage of the capacitor is balanced. Similarly, average balancing is used for each leg voltage balancing of CHB-based DSTATCOM.
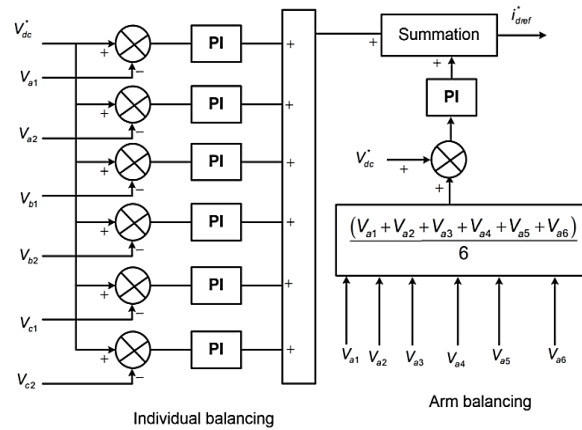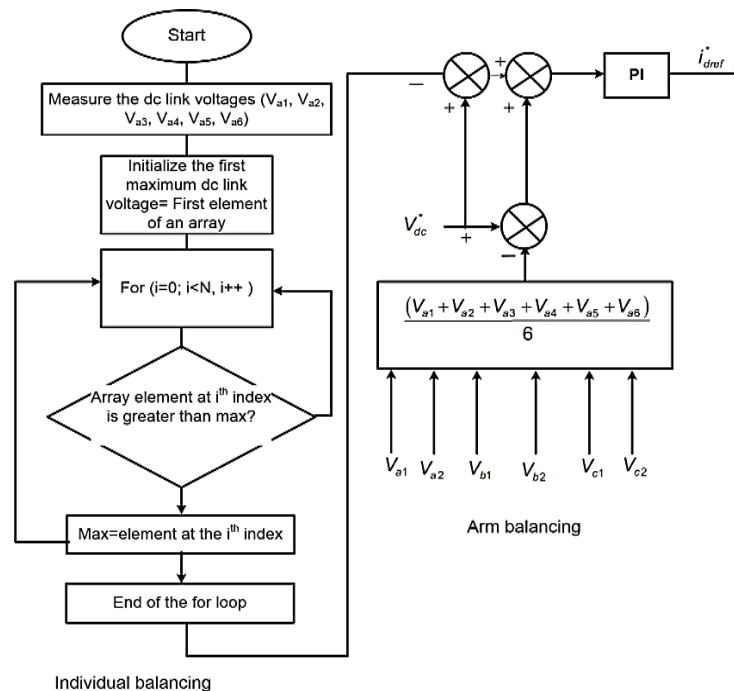
Figure 3. Conventional voltage balancing

Figure 4. Improved voltage balancing scheme

5. SIMULATION RESULTS

The complete electrical power system with DSTATCOM is shown in Figure 1. The DSTATCOM three-phase electrical sources are realized with electrical sources block set of Sim power system library. The nonlinear is realized with power electronics and elements library of the Sim power system. The DSTATCOM is also realized with the power electronics and elements of the Sim power system library of Simulink. The two different control schemes of the DSTATCOM are created with the control blocks of Simulink library. The simulated response of DSTATCOM with conventional SRF is shown in Figure 5. Initially, before t = 4 sec, the source current follows the load current. The load current wave form is stepped in shape and highly distorted. The triple harmonic components are presented in load. At t = 4 sec, DSTATCOM is switched-on, and the source current waveform tends to be nearly sinusoidal waveform and follows the source voltage waveform. The power factor of the voltage and current waveform is almost unity. The time required for the source current to reach steady is almost 3-4 cycles. The corresponding DC side voltage of the DSTATCOM capacitor is shown in Figure 5. The time required for the DC voltage of DSTATCOM to reach steady is almost 0.05 sec. the THD of the source current before harmonics elimination is shown in Figure 6. Figure 7(a) shows the value of THD of source current before harmonics elimination DSTATCOM is 26.76%. After

compensation with DSTATCOM, Figure 7(b) shows the THD of source current is reduced to 2.13% as depicted Figure 7.

The current waveforms of DSTATCOM with SMC-based SRF are shown in Figure 8. Initially, before t = 0.15 sec, the source current follows the load current. The waveform of the load current is stepped in shape and highly distorted. This characteristic is caused by the presence of triple harmonics components in the load current. At t = 0.15 sec, DSTATCOM is switched-on, and the source current waveform tends to be nearly sinusoidal waveform and follows the source voltage waveform. The power factor of the voltage waveform and current waveform is unity. The time required for the source current to reach steady is almost 2-3 cycles. The corresponding DC side voltage of the DSTATCOM capacitor is shown in Figure 9. The time required for the DC voltage of DSTATCOM to reach steady is almost 0.05 sec. The total harmonics distortion of the source current before harmonics elimination is shown in Figure 7. The value THD of source current before harmonics elimination DSTATCOM is 26.76%. After compensation with DSTATCOM, the THD of source current is reduced to 2.13% as depicted in Figure 10. From the characteristics of DSTATCOM, the simulated results obtained with the SMC-based control scheme outperform that of the conventional SRF schemes.
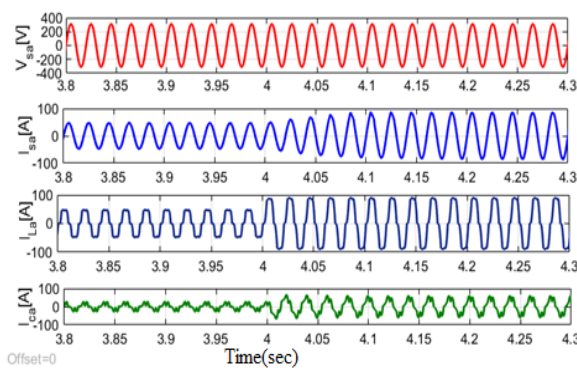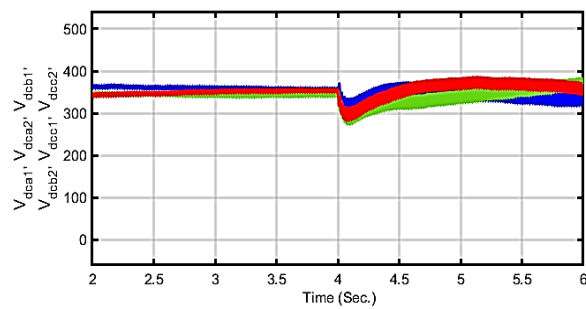

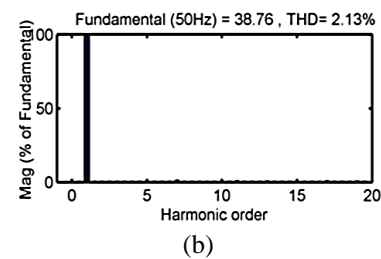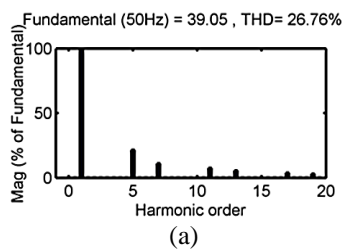Figure 5. Simulated waveform

Figure 6. DC link voltage

Figure 7. Source current THD (a) THD value without DSTATCOM and (b) THD value with DSTATCOM
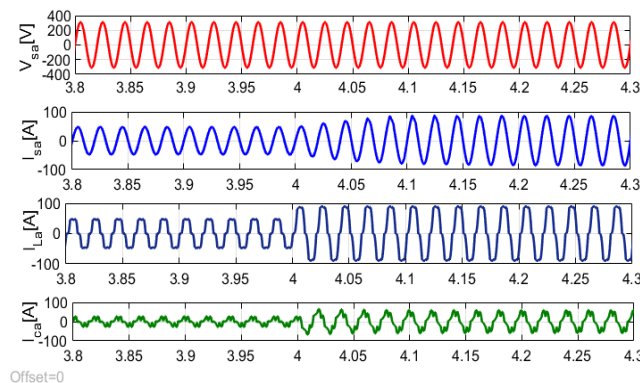

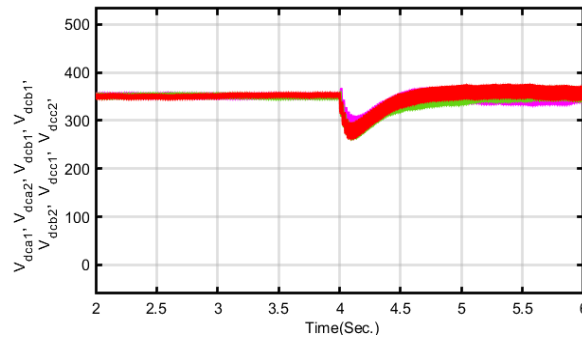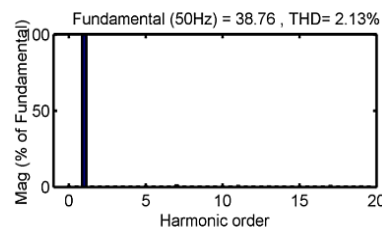Figure 8. Simulated waveform

Figure 9. DC link voltage

Figure 10. Source current with compensation

6.   CONCLUSION

In this paper, the DSTATCOM based on a reduced switch count converter based is adopted for current harmonics elimination in the source current of the electrical system. The simulation study is carried out to study the comparative show of the DSTATCOM with two different voltage balancing schemes with SMC controller-based control schemes. The comparative results show that the improved voltage balancing control with an SMC-based SRF control scheme outperforms that of conventional voltage balancing with SMC controller-based SRF in dynamic conditions. The CHB-MLI-based DSTATCOM with improved voltage balancing with the SMC-SRF control scheme has a better steady-state response than that of the conventional control scheme. The firing pulse of CHB-MLI-based DSTATCOM is generated with sinusoidal pulse width modulation.

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