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# Design of a linearized 4-H-bridge STATCOM for load balancing purposes

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**ABSTRACT**

In this paper, a 4-H-bridge STATCOM (4-HB STATCOM) is introduced. Four H-bridges are cascaded to build the proposed STATCOM. Cascading the H-bridges makes it possible to operate the devised STATCOM on high voltage levels with less voltage harmonic association. The proposed STATCOM is equipped with an adaptive current controller and a voltage balancing technique for its DC capacitor voltages. The adopted controlling strategy makes the STATCOM respond continuously and linearly to current demand in both inductive and capacitive operational modes without noticeable association of harmonics. The DC capacitor of each H-bridge is shunted by a second harmonic filter to stabilize its voltage. The proposed STATCOM does not require initial charging of its DC capacitors because it is provided with a utilized technique for charging them rapidly by disabling the STATCOM carrier for a certain period sufficient to build up the required level of DC voltages. In this work, the proposed STATCOM is designed to operate on 11 kV AC voltage as a continuously and linearly controlled compensating susceptance. It can deservingly be employed in load balancing systems for achieving big amount of energy savings in power generation and big reduction in transmission losses.



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## 1. INTRODUCTION

The controlling strategies, harmonic treatment, load compensation, and different configurations of STATCOM's layouts are studied in this work [1]–[3]. A new controlling scheme was proposed in [4] to balance the DC buses in cascaded H-bridge converters. The adopted method certifies the convergences of the DC capacitor voltages to a reference value, even though their loads are taking different amounts of power. A new controlling strategy was proposed for a STATCOM built of voltage source inverter based H-bridges in cascaded form [5]. The controlling scheme focused on independent balancing of the voltages across the capacitors in the H-bridge converters. To carry out the proposed control strategy, the voltage of the capacitor in each H-bridge is simultaneously compared with a reference voltage. In a four-wire system, a DSTATCOM built of a zigzag transformer equipped with a low power voltage source converter was proposed in [6] for the power quality improvement purposes.

The proposed STATCOM was designed for Var control, harmonics elimination, load balancing, and voltage control at the point of common coupling (PCC). Three control schemes of a 3-phase STATCOM were employed for compensating unbalanced voltages and currents [7]. These schemes were voltage control, current control, and integrated control. By selecting suitable controlling schemes, the introduced system can

accomplish voltage regulation, current balancing, and power factor correction. A multilevel converter based STATCOM was discussed in [8]. This STATCOM was equipped with a new current controller and it was introduced for fast Var compensation, treatment of harmonics, and load current balancing of a 3-phase AC source using a new algorithm for current control. A harmonic free compensating susceptance built of a TCR and certain filtering circuitries was proposed in [9] for load balancing purposes. It was controlled linearly and continuously in both inductive and capacitive operational modes. A Δ-connected STATCOM built on the basis of cascaded multilevel converters was introduced in [10]. The exchange reactors of this STATCOM were serially connected to reactors coupled mutually in order to offer easy paths for the flow of circulating currents. An approach of parameter design of a PI controller for balancing the individual DC voltages of cascaded H-bridge STATCOM was proposed in [11]. Using phase shift SPWM, two control loops (phase angle and DC voltage) were exploited to certify the balance of the DC voltages and to calculate parameters of the PI controller. A harmonic free TCR was introduced in [12] as a compensating susceptance controlled linearly and continuously in inductive operational mode, whereas in [13] a TCR equipped with a new current controller and an adaptive filtering scheme was introduced to function as a continuously and linearly controlled capacitive susceptance. Both categories were dedicated for power quality purposes like power factor correction and load balancing. An asymmetric distribution STATCOM provided with DC-link regulation and reactive power control loops for converters built in cascaded multilevel topology was presented in [14] in order to enhance the power quality in distribution systems of medium-voltages. A control scheme was investigated in [15] to enhance the capability of the DC fault ride-through of a multilevel converter station with full-bridge modular, while certifying a stable operation as a safely controlled STATCOM during DC faults without needing to fault isolation. A STATCOM built of cascaded H-bridges was proposed in [16] to operate with low DC capacitances calculated in the case of the maximum acceptable voltage ripple.

The current limit method of the voltage controlling scheme of a STATCOM built using delta-connected H-bridge and operated under an event of unbalanced voltage fault was discussed in [17]. When a certain phase to ground fault occurred, the possibility of heightening the sagging phase voltage was taken into account using symmetric transformation method. An advanced controller was used in [18] to produce the PWM pulses for the switching devices of a STATCOM built of cascaded H-bridges. The feedback control of the proposed STATCOM offered controllable reactive power and reduced THD. The effectiveness of certain controllers can make multilevel inverter based STATCOMs allow effective operation, low harmonic association in the absence of filters, low switching frequency, and high flexibility to achieve any required level of output voltage [19]. A certain control scheme for balancing the capacitor voltages of a STATCOM based on cascaded H-bridges and full-bridges was proposed to accomplish the control aims [20]. The presented balancing strategy distributed Var among the cells equally and increased the reliability in addition to balancing voltage among capacitors. Disturbances like the fluctuations of voltage resulting from the complexities of grid and conditions of unbalanced loads cause severe power quality issues like voltage unbalance and total harmonic distortion [21]. A delta-connected Multilevel STATCOM was proposed to provide both Var and real power support [22]. The purpose of this work was to accomplish short-term storage of energy to enable grid support services. The strategies of balancing active power for the satisfactory operation of the most commonly used STATCOMs under unbalanced current and/or voltage conditions were discussed in [23], whereas a new topology for a STATCOM was proposed in [24] for producing multilevel AC voltages. The four-leg distribution STATCOM is suggested to eliminate the current imbalances in low-voltage power system networks [25]. In this research, an 11 kV four H-bridge STATCOM is introduced as a linearly and continuously controlled compensating susceptance for load currents balancing issues.

## 2. THE PROPOSED FOUR H-BRIDGE STATCOM

The layout of the four H-bridge STATCOM (4-HB STATCOM) is shown in Figure 1. Each H-bridge (HB) in this figure is equipped with a second harmonic filter and a DC chopper. The second harmonic filter is used for smoothing the voltage profile of the HB DC capacitor voltage, while the DC chopper keeps it in balance with the other DC capacitor voltages in the 4-HB STATCOM. The STATCOM reactor is portioned into two equal reactors. $L_{RST1}$ and $R_{ST1}$ represent the self-inductance and self-resistance of the first reactor, respectively, whereas $L_{RST2}$ and $R_{ST2}$ represent the self-inductance and self-resistance of the second reactor, respectively. The capacitor $C_{SH}$ is inserted to treat the voltage spikes. The AC supply voltage $v_{ac}$ is stepped down to $k_3v_{AC}$, which is an analog voltage having an amplitude of 5 V. Therefore, $k_3v_{AC}$ is running at the same phase and frequency $f$ of $v_{AC}$. In the STATCOM current controller, the analog voltage $k_3v_{AC}$ is shifted by a small angle $\alpha$ depending on the demanded STATCOM susceptance $k_2B_S$ to produce the modulating signal $v_{MOD}$, which is expressed by:

$$v_{MOD} = A_{MOD}\, sin(\omega t + \alpha) \quad (1)$$

where, $A_{MOD}$ is its amplitude and $\omega$ is the angular frequency ($2\pi f$) of the AC supply voltage. Generally, sinusoidal pulse width modulation SPWM is usually exploited to trigger STATCOMs. Thus, the instantaneous voltage $v_{VSI}$ across the cascaded 4-H bridges is governed by the modulating signal $v_{MOD}$. The average values of $v_{VSI}$ constitute a sinusoidal envelope representing its fundamental components $v_1$ and running at the AC supply frequency. Since, $v_1$ follows $v_{MOD}$, then $v_1$ will be shifted from $v_{AC}$ by an angle $\alpha$, which represents the STATCOM angle. Therefore, the STATCOM rms current $I_S$ can be expressed by:

$$I_S = \frac{V_{A.C} - V_1 \angle \alpha}{R_{ST1} + j\omega L_{ST1} + R_{ST2} + j\omega L_{ST2}} \cong \frac{V_{A.C} - V_1 \angle \alpha}{j\omega L_{ST1} + j\omega L_{ST2}} \quad (2)$$

where, $V_{AC}$ and $V_1$ are the rms values of $v_{AC}$ and $v_1$, respectively. The very close approximation in (2) is due to the negligible ohmic resistances of the STATCOM reactors compared to their reactance.

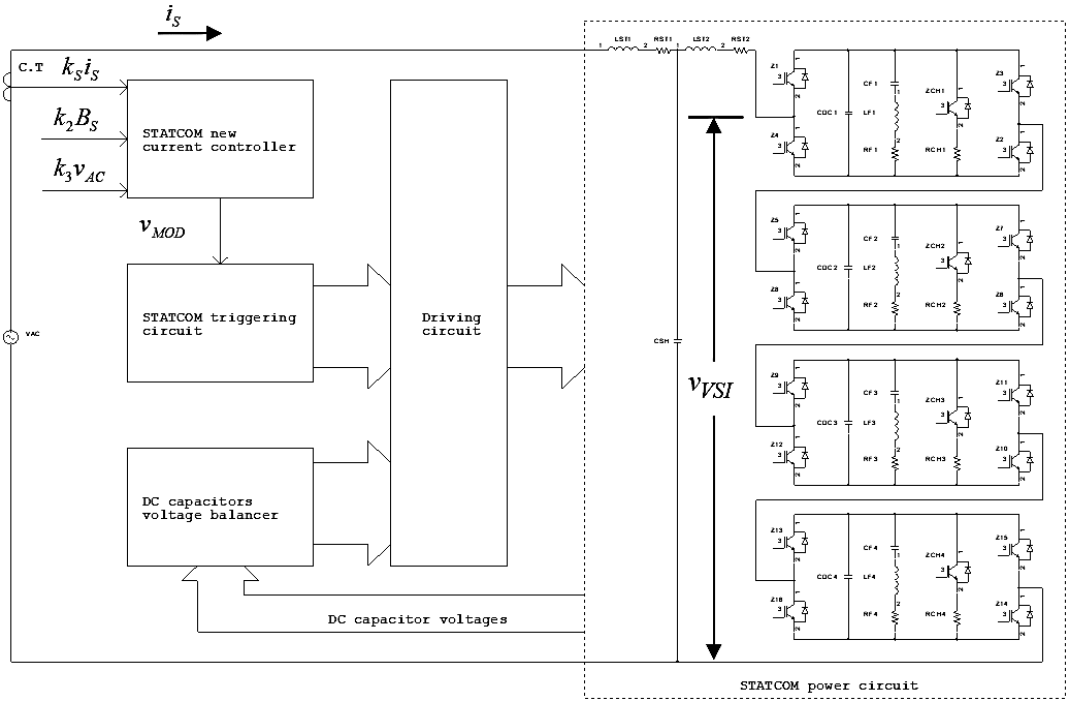



Figure 1. Layout of the proposed STATCOM

In this work, $\alpha$ is controlled in the range of ±0.1rads. Consequently, $V_{AC}$ and $V_1 \angle \alpha$ will be almost in phase and $I_S$ will be purely reactive. If $V_{AC}$ is greater than $V_1 \angle \alpha$, then $I_S$ will be purely inductive and If $V_{AC}$ is less than $V_1 \angle \alpha$, then $I_S$ will be purely capacitive. The STATCOM current controller is responsible for generating the modulating signal $v_{MOD}$. The main input signals to this controller are $k_S i_S$, $k_2 B_S$, and $k_3 v_{AC}$. The input signal $k_2 B_S$ is an analog signal less than 10 V and proportional to the STATCOM susceptance required to satisfy the reactive current demand. The input signal $k_S i_S$ is an analog signal proportional to the instantaneous STATCOM current $i_S$ and has a maximum amplitude of 10 V.

### 2.1. The STATCOM current controller

Figure 2 illustrates the modeling of the controlling scheme. When $i_S$ (the instantaneous current of STATCOM) is detected and converted to the voltage signal $k_S i_S$ by the current transformer (CT), the latter voltage signal is treated sample and hold circuits to produce $k_S I_{Sm}$, which is an analogue voltage signal proportional to $I_{Sm}$ (amplitude of $i_S$). The constant $k_S$ is dependent on the turn ratio of the current transformer and the passive components of its circuitry. The voltage $k_S I_{Sm}$ is then subtracted from another signal called $k_S I_{Dm}$, which is directly proportional to $I_{Dm}$ (amplitude of reactive demand). The analogue voltage $k_S \Delta I_{Sm}$ is the subtraction result, which represents the deviation amount of the actual current drawn by the STATCOM from the required reactive current. $I_{Sm}$ is negative when the reactive current demand is inductive and is positive during capacitive current demand. Its value. The phase and magnitude of the current flowing in the STATCOM reactor are identified by detecting $I_{Sm}$. The controlling circuitry of the STATCOM angle is an important part in

this controller. This circuitry comprises $Q_1$ and $Q_2$, which are two identical silicon transistors biased critically in their active regions. The threshold voltage $V_\gamma$ is the cut in value of the base to emitter voltage of $Q_1$ and $Q_2$. According to the biasing conditions of $Q_1$ and $Q_2$, the currents of their collector's $i_{C1}$ and $i_{C2}$ can be calculated as follows:

$$i_{C1} = h_{FE} i_{B1} = \frac{h_{FE} \Delta V(\alpha)}{R_{B1}}, \quad \Delta V(\alpha) \geq 0 \tag{3}$$

$$i_{C2} = h_{FE} i_{B2} = \frac{-h_{FE} \Delta V(\alpha)}{R_{B2}}, \quad \Delta V(\alpha) \leq 0 \tag{4}$$

Where, $h_{FE}$ is the DC current gain of $Q_1$ and $Q_2$ and $\Delta V(\alpha)$ is a voltage signal proportionally corresponding to the error associated with the STATCOM angle $\alpha$.

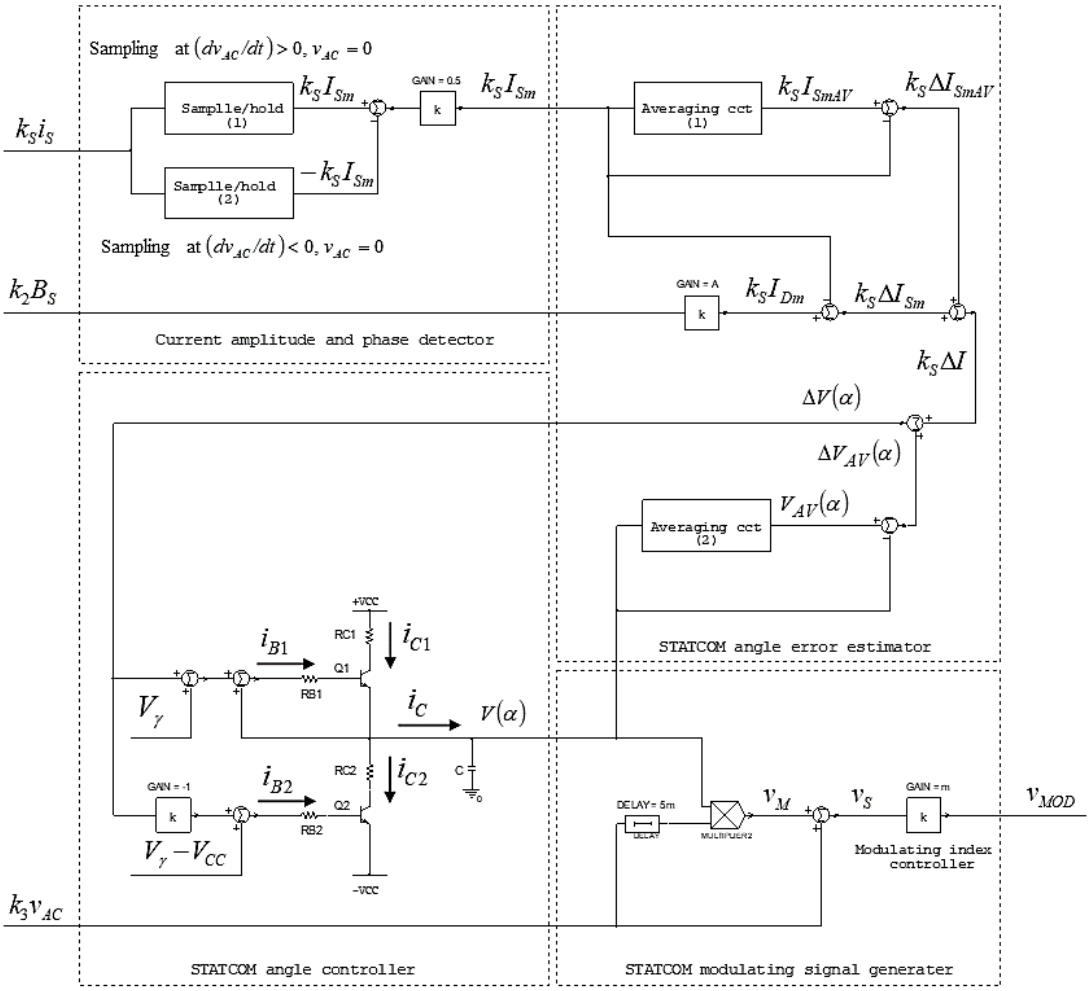



Figure 2. The schematic design of the STATCOM current controller

$V(\alpha)$ is proportional to the STATCOM angle and it is definitely the voltage appearing across $C$ capacitor. It represents a voltage signal governing an important circuitry in this controller. This controlling part is designed to generate $v_{MOD}$, which represents the modulating signal. The $C$ capacitor current $i_C$ is given by (5).

$$i_C = \begin{pmatrix} i_{C1} + i_{B1}, & \Delta V(\alpha) \geq 0 \\ -i_{C2}, & \Delta V(\alpha) \leq 0 \end{pmatrix} \tag{5}$$

The analogue signal $V(\alpha)$ can be expressed as (6).

$$V(\alpha) = \frac{1}{C}\int i_C dt \quad (6)$$

The STATCOM angle error signal $\Delta V(\alpha)$ is determined by (7),

$$\Delta V(\alpha) = \Delta V_{AV}(\alpha) + k_S \Delta I \quad (7)$$

where, $\Delta I$ and $\Delta V_{AV}(\alpha)$ are expressed by:

$$\Delta I = \Delta I_{Sm} + \Delta I_{SmAV} \quad (8)$$

$$\Delta V_{AV}(\alpha) = V_{AV}(\alpha) - V(\alpha) \quad (9)$$

where, $V_{AV}(\alpha)$ is the average value of $V(\alpha)$. $\Delta I_{Sm}$ and $\Delta I_{SmAV}$ stand for components of the current errors, which are expressed by:

$$\Delta I_{Sm} = I_{Dm} - I_{Sm} \quad (10)$$

$$\Delta I_{SmAV} = I_{SmAV} - I_{Sm} \quad (11)$$

where, $I_{SmAV}$ is an analogue signal proportional to the instantaneous value of $I_{Sm}$ average. When $i_C$ rapidly grows positive, $V(\alpha)$ rapidly builds up and it may exhibit noticeable overshoots. The error voltage signals identified by the parameters $k_S\Delta I_{SmAV}$ and $\Delta V_{AV}(\alpha)$ reduce the possible chances for $V(\alpha)$ to reveal noticeable overshoots and settle the current of the STATCOM in its desired value. When $V(\alpha)$ approaches its steady state condition, both $k_S\Delta I_{SmAV}$ and $\Delta V_{AV}(\alpha)$ vanish. $V(\alpha)$ identifies the phase angle of $v_{MOD}$ with respect to the STATCOM AC voltage. $V(\alpha)$ is varying between $-V_{CC}$ and $+V_{CC}$. Positive values of $\Delta V(\alpha)$ cause the capacitor $C$ charge towards $+V_{CC}$ through the transistor $Q_1$, whereas its negative values make $C$ discharge through $Q_2$ towards $-V_{CC}$. The generator of the modulating signal is constructed of an analogue multiplier, a 5msec time delayer, a summer, and an amplifier with a forward voltage gain $m$ corresponding to the modulation index of the STATCOM. The signal voltage $k_3v_{AC}$ is a low-level sinusoidal voltage signal in phase with the AC voltage source. For a 50 Hz AC source, the time delay of 5msec corresponds to a delay in phase of $\pi/2$. If $v_{AC}$ (the AC voltage) is defined by $V_m sin(\omega t)$, then $v_M$ (the analogue multiplier output) will be determined by:

$$v_M = k_3 V_m \sin\left(\omega t - \frac{\pi}{2}\right) V(\alpha) A_M = -V(\alpha) A_M k_3 V_m \cos(\omega t) \quad (12)$$

where, $A_M$ is the analogue multiplier gain and $V_m$ is $v_{AC}$ amplitude. The output $v_S$ of the summing amplifier is defined by (13).

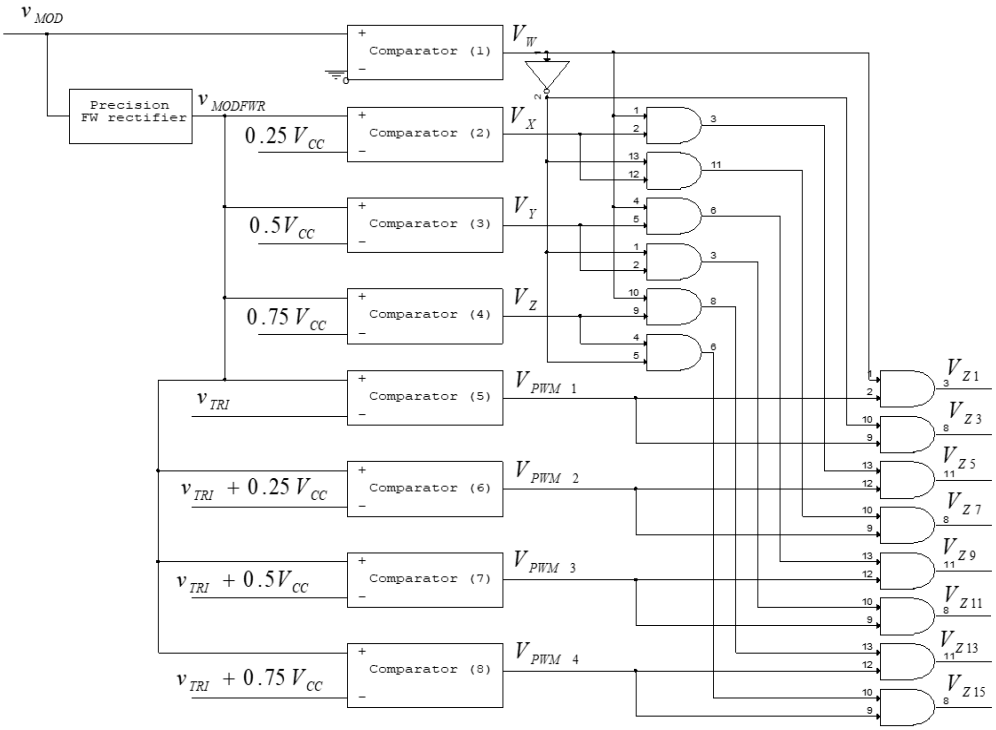
$$v_S = k_3 v_{AC} + v_M = k_3 V_m \left(\sqrt{\left(A_M V(\alpha)\right)^2 + 1}\right) sin\left(\omega t - tan^{-1}\left(A_M V(\alpha)\right)\right) \quad (13)$$

The modulating signal is obtained after the multiplication of $v_S$ by the modulation index $m$ and can be expressed as (14).

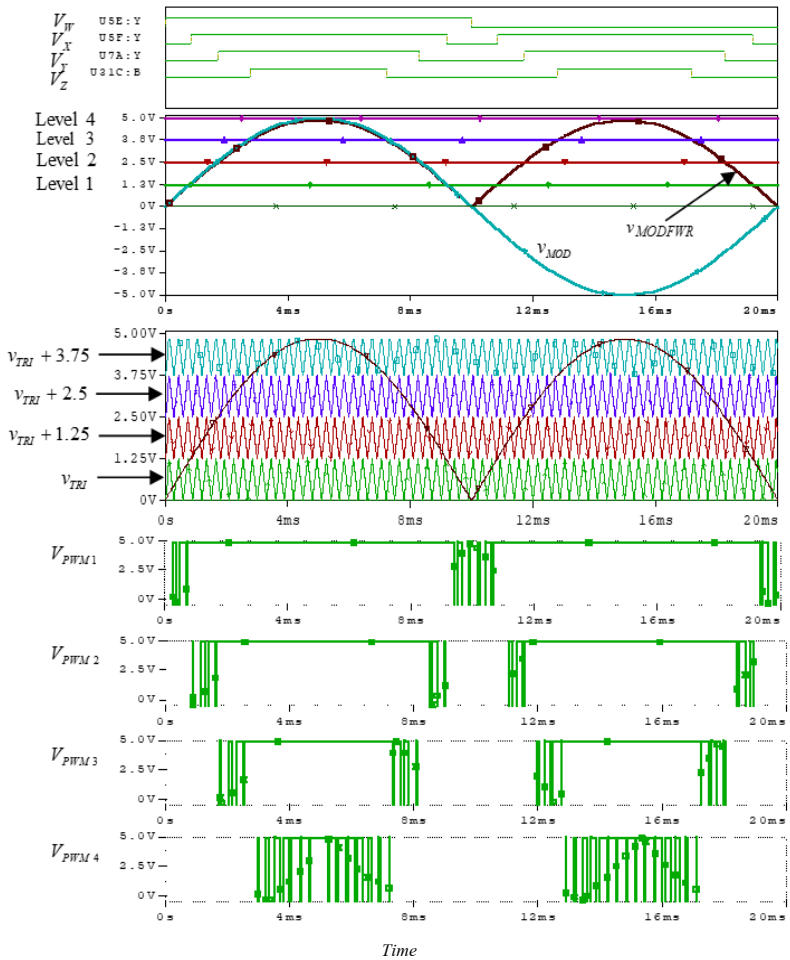
$$v_{MOD} = m v_S \quad (14)$$

### 2.2. The STATCOM triggering scheme

The triggering technique for the proposed 4-HB STATCOM and its corresponding triggering waveforms are shown in Figure 3. For unity modulation index in this technique, the modulating signal amplitude $V_{MOD}$ should be equal to the DC supply voltage $V_{CC}$. The latter voltage is divided into four equidistant levels (0.25 $V_{CC}$, 0.5 $V_{CC}$, 0.75 $V_{CC}$, and $V_{CC}$). Figure 3(a) shows the layout of the triggering scheme, whereas Figure 3(b) shows the generation of rectangular and PWM waveforms of the proposed STATCOM. In Figure 3(b), the modulating signal $v_{MOD}$ is firstly compared with a zero voltage for producing the rectangular waveform $V_W$ and then full-wave rectified by a precision rectifier to produce $v_{MODFWR}$. The latter signal is compared with the voltage levels 0.25 $V_{CC}$, 0.5 $V_{CC}$, and 0.75 $V_{CC}$ for producing the rectangular voltages $V_X$, $V_Y$, and $V_Z$ respectively. In addition, $v_{MOD}$FWR is compared with $v_{TRI}$, $v_{TRI}$ +0.25 $V_{CC}$, $v_{TRI}$ +0.5 $V_{CC}$, and $v_{TRI}$ +0.75 $V_{CC}$ for producing the pulse width modulation signals $V_{PWM1}$, $V_{PWM2}$, $V_{PWM3}$, and $V_{PWM4}$ respectively. The eight generated rectangular and PWM waveforms are processed logically for producing the triggering signals for the upper switching devices in the 4-HB STATCOM as shown in Figure 4.




(a)




(b)

Figure 3. The triggering mechanism of the proposed STATCOM (a) topology and (b) waveforms

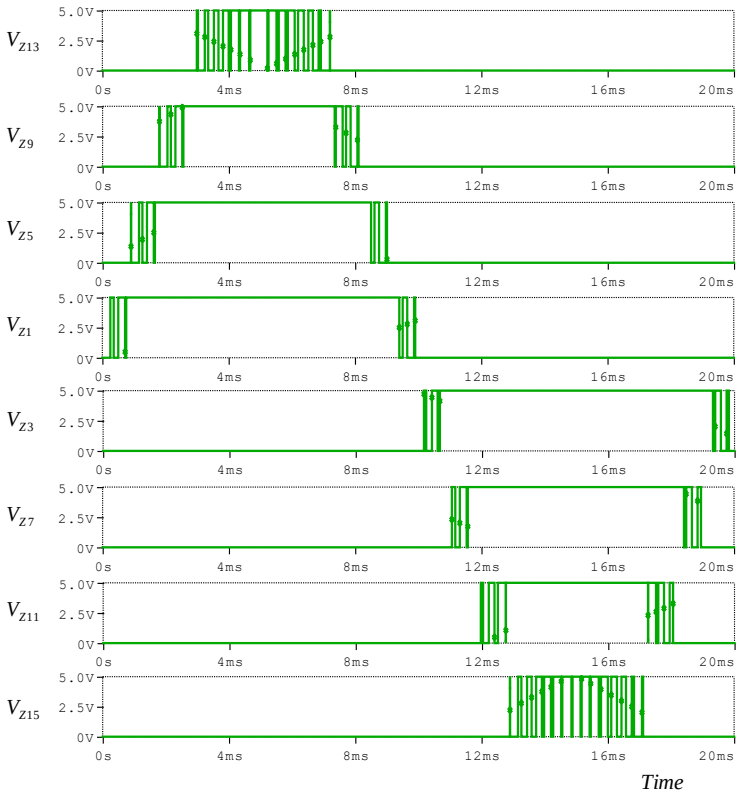



Figure 4. The triggering signals for the upper switching devices in the 4-HB STATCOM

### 2.3. The voltage balancing technique of the 4-HB STATCOM DC capacitor voltages

The layout of this technique is shown in Figure 5. The positive and negative potentials of the DC capacitors are stepped down to low levels through potential dividers and then processed by unity gain difference amplifiers to produce the low-level analogue voltages $k_4V_{DC1}$, $k_4V_{DC2}$, $k_4V_{DC3}$, and $k_4V_{DC4}$, which are proportional to the actual DC capacitor voltages $V_{DC1}$, $V_{DC2}$, $V_{DC3}$, and $V_{DC4}$ respectively. The low-level analogue voltages are summed and divided by four to obtain their average $k_4V_{DCAV}$. Each of $k_4V_{DC1}$, $k_4V_{DC2}$, $k_4V_{DC3}$, and $k_4V_{DC4}$ is compared with $k_4V_{DCAV}$.to produce the triggering signal of its corresponding DC chopper switching device. The DC chopper triggering signals are $V_{ZCH1}$, $V_{ZCH2}$, $V_{ZCH3}$, and $V_{ZCH4}$. If a certain DC capacitor voltage exceeds the average value of the capacitor voltages, then its corresponding chopper will discharge its excessive charge through a resistor. When the actual DC capacitor voltage becomes equal or less than the average value the chopping process ceases.

### 2.4. The circuit design of the proposed four H-Bridge STATCOM

This STATCOM is designed to be a continuously and linearly controlled compensating susceptance. Three identical STACTOMs connected in delta-form are required to build a compensating system for balancing 3-wire loads. The balancing system is proposed to operate on 11 KV, 50 Hz ungrounded three phase system. Consequently, the proposed STATCOM is designed to operate on an AC voltage $v_{AC}$ (line-to-line voltage) of 11 KV. The proposed STATCOM is designed such that it can satisfy a reactive current demand (capacitive or inductive) of about 733 A (peak value). The main task in this design is how to determine the voltage tolerance of the IGBT that should be used in the construction of each HB voltage source inverter (HB VSI). If the total DC voltages across the four DC capacitors are allowed to acquire a level of 1.3 $V_m$ during the maximum steady state capacitive reactive current demand, then the expected DC voltage across each DC capacitor will be 0.325 $V_m$. Where, $V_m$ is the amplitude of the AC voltage applied across the STATCOM terminals. Since the amplitude of 11 KV line to line rms voltage is about 15556 V, the expected capacitor voltage is slightly greater than 5 KV. Taking these presumptions into consideration, the IGBT 5SNA 0750G650300, which has maximum continuous voltage and current ratings of 6.5 KV and 750 A respectively is a good choice for meeting the voltage and current requirements. The circuit design of the 4-HB STATCOM is shown in Figure 6. Its design is carried out on PSpice, which is very close in performance to real hardware.

The rough estimation of the reactance of the 4-HB STATCOM reactor can directly be obtained by dividing 0.3 $V_m$ by the STATCOM reactive current rating (733 A (peak value)). Doing this, the inductance of the series reactor is calculated to be 20 mH. This series reactor is divided into two identical reactors and their common point is connected to a shunt capacitor ($C_{SH}$) in order to decrease the carrier frequency ripples associating the STATCOM current. The resistance to inductance ratio for these reactors is chosen to be 0.025 Ω/mH. This choice serves to obtain pure reactive current and reduce STATCOM losses. The second harmonic filter and the DC capacitors are designed such that maximum swings associating the DC capacitor voltages never exceed 5% of their steady state values at maximum reactive current demand (capacitive or inductive). Consequently, for each H-bridge, the DC capacitor and the second harmonic filter are designed as follows: $C_{DC}$ = 2000 μF, $C_F$ = 1000 μF, $L_F$ = 1.25 mH, and $R_F$ = 0.05 Ω. The controller of the DC choppers installed for balancing the DC capacitor voltages can be adjusted to determine the deviation of each DC capacitor voltage from the average value of the four DC voltages.

The STATCOM current is detected by the current transformer CT and then converted through the resistance $R_{CT}$ to the analogue voltage $k_S i_S$. This signal will be processed in the sub-circuit "STATCOM current controller" for generating the 4-HB STATCOM modulating signal $v_{MOD}$. For CT primary to secondary turn ratio of 0.01 and $R_{CT}$ of 0.683 Ω, the constant $k_S$ is calculated to be 0.00683 Ω. The maximum value of $k_S i_S$ is expected to be +5 V at the STATCOM maximum capacitive current demand. The modulating signal $v_{MOD}$ is processed in the sub-circuit "4-HB STATCOM triggering CCT" for producing the 4-level PWM triggering signals in the mechanism stated above.

The DC capacitor voltages tend to be unbalanced during the STATCOM operation. This behavior leads to the production of distorted current waveform through the STATCOM reactor. For treating such undesirable behaviors of DC capacitors, a voltage balancing technique is devised for this multi-level STATCOM. The technique is involved in equipping each HB VSI with a chopping circuit. Each circuit is constructed of an IGBT connected in series to 50 Ω resistor. When any DC voltage exceeds the average value of the four DC voltages, the corresponding chopper starts to discharge the voltage excess through the chopper resistor. Once the excess has recovered, the chopping process ceases. The sub-circuit denoted by "DC capacitor voltages balancer" is designed on PSpice to achieve the balancing process of the STATCOM DC capacitor voltages. The circuit design of the 4-HB STATCOM includes a sub-circuit responsible for detecting the analogue signal $k_3 v_{AC}$ called "STATCOM AC voltage detector". Actually, each IGBT needs a proper driving circuit, thus this STATCOM includes the sub-circuit denoted by "4-HB STATCOM driving CCT" which is a bulk driving circuit for all switching devices. The driving circuit of the IGBT used in this STATCOM is designed according to its datasheet specifications. The AC voltage detector, current controller, triggering circuit, DC capacitors voltage balancer, and driving circuit are designed as built in libraries on PSpice using the suitable components available on this application.

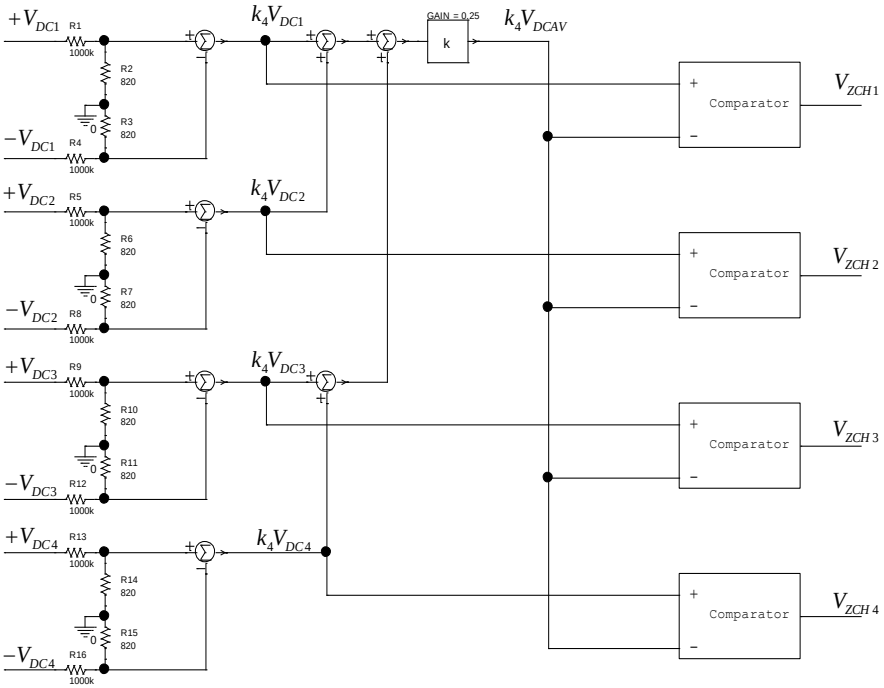



Figure 5. The balancing technique of the DC capacitor voltages of the 4-HB STATCOM

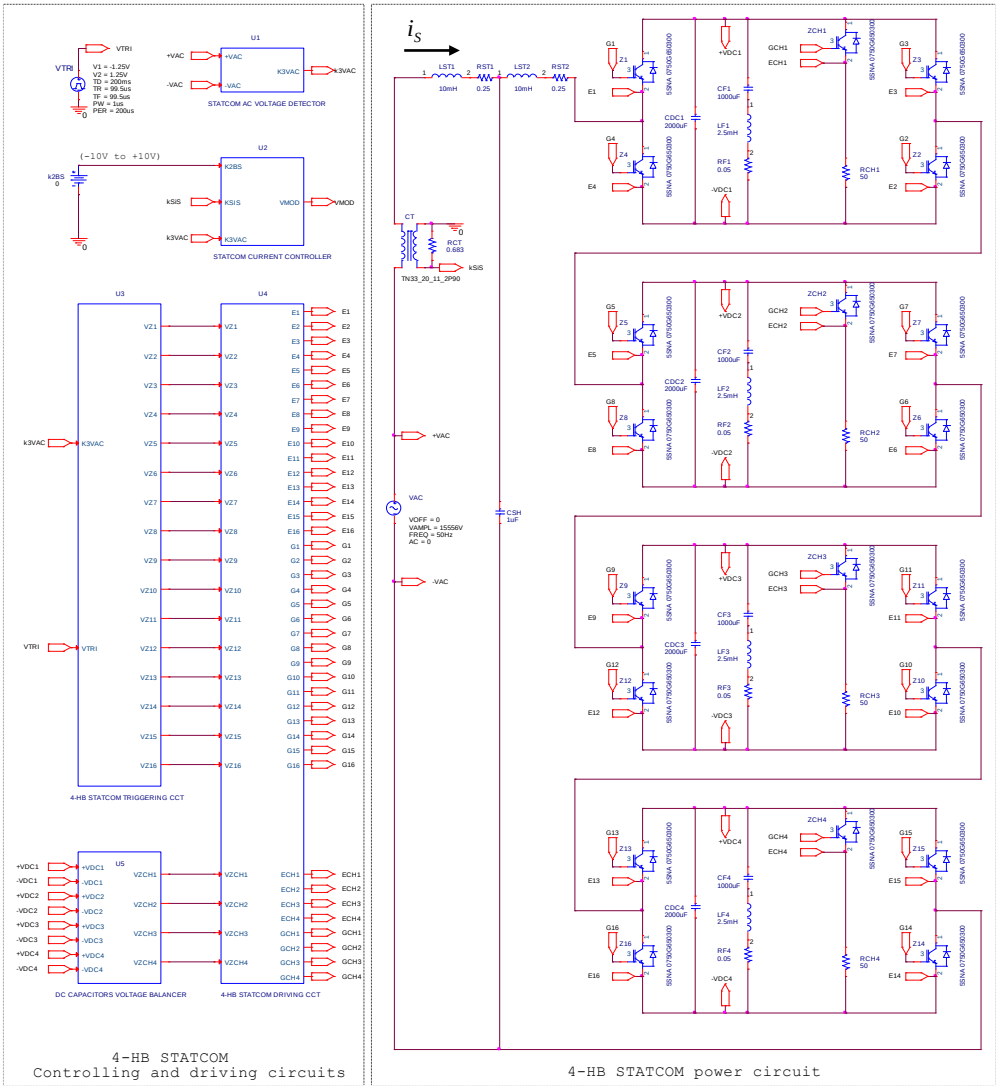



Figure 6. The PSpice circuit design of the proposed 4-HB STATCOM

## 3. RESULTS AND DISCUSSION

The 11 KV, 50 Hz 4-HB STATCOM shown in Figure 6 was tested on PSpice for investigating its control continuity, linearity, and harmonic injection. It is controlled by the analogue voltage $k_2B_S$, which is proportional to the reactive current demand and varying in the range of -10 V to +10 V. +10 V corresponds to maximum capacitive reactive demand of 733A (peak value), while -10 V corresponds to maximum inductive reactive current demand 733 A (peak value). It was operated by a zero phase AC voltage of frequency of 50 Hz and amplitude of 15556 V (peak value), which corresponded to a rms value of 11 KV (the line-to-line voltage). The modulation index of the tested STATCOM was 0.98 and the carrier frequency was 5 KHz. The basic instantaneous parameters measured in the PSpice investigations were the AC source voltage $v_{AC}$; the 4-level VSI generated voltage $v_{VSI}$; the STATCOM current $i_S$; the frequency spectrum $F(S)$ of $i_S$; the DC capacitors voltages $V_{DC1}$, $V_{DC2}$, $V_{DC3}$, and $V_{DC4}$; the DC choppers currents $i_{CH1}$, $i_{CH2}$, $i_{CH3}$, and $i_{CH4}$. Firstly, the STATCOM was tested to show its performance during zero reactive current demand. Figure 7 shows the transient and steady states results of this test. The test corresponded to $k_2B_S$ of zero value. It is obvious that the STATCOM carried zero steady state current at this test.

Disabling the carrier signal for a time of about 200 ms is adopted in this work to speed up the charging process of the DC capacitors in the 4-HB STATCOM. During the disabling of the carrier signal, the discharging process associating the voltage generation of the 4-level VSI inverter is slowed down. STATCOM performance during maximum inductive reactive current is shown in Figure 8. The results of this test corresponded to $k_2B_S$ of -10 V. The performance of the 4-HB STATCOM during maximum capacitive reactive current is shown in Figure 9. The results of this test corresponded to $k_2B_S$ of +10 V.

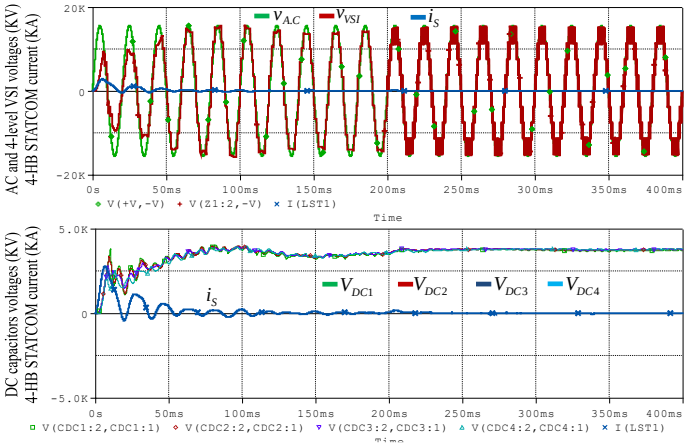



Figure 7. Performance of the 4-HB STATCOM during zero reactive current demand

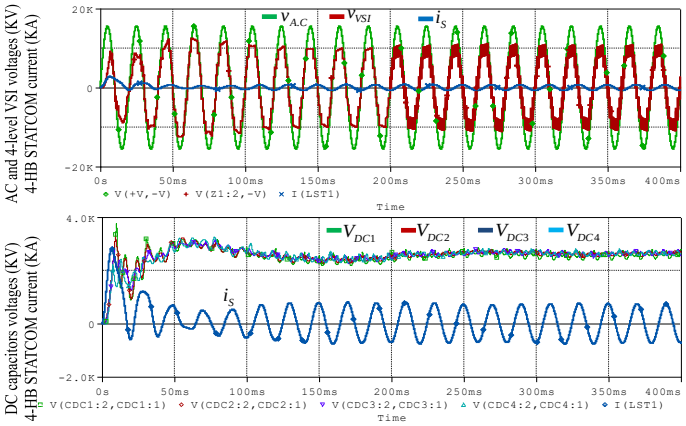



Figure 8. STATCOM performance during maximum inductive reactive current demand

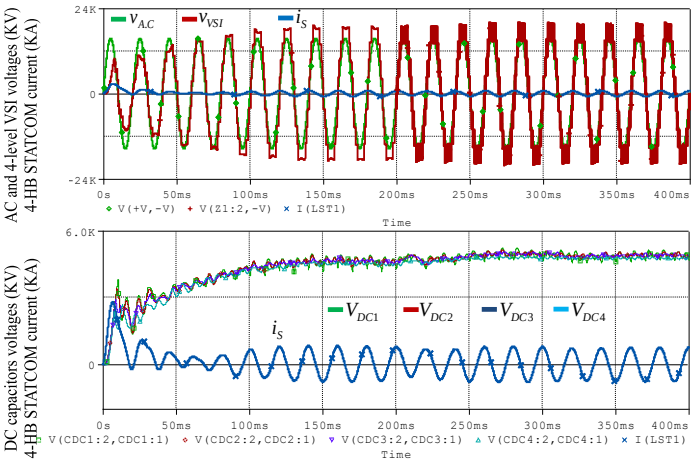



Figure 9. STATCOM performance during maximum capacitive reactive current demand

To investigate the STATCOM for the current harmonics associating its reactive current fundamental, it was tested during steady state operation at different loading conditions. Figure 10 shows the steady state performance of the STATCOM during zero reactive current demand. Figure 11 shows the steady state performance of the STATCOM during maximum inductive reactive current demand of 733 A (peak value). Figure 12 shows the steady state performance of the STATCOM during maximum capacitive reactive current demand of 733A (peak value).

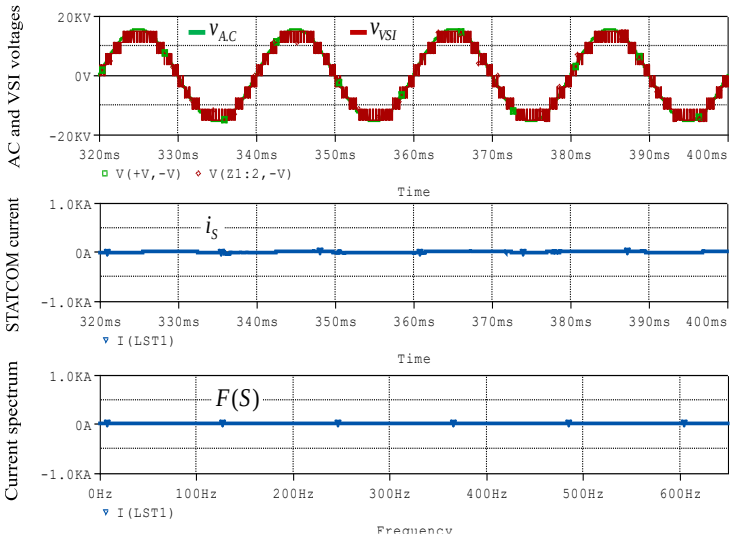



Figure 10. STATCOM steady state performance during zero reactive current demand

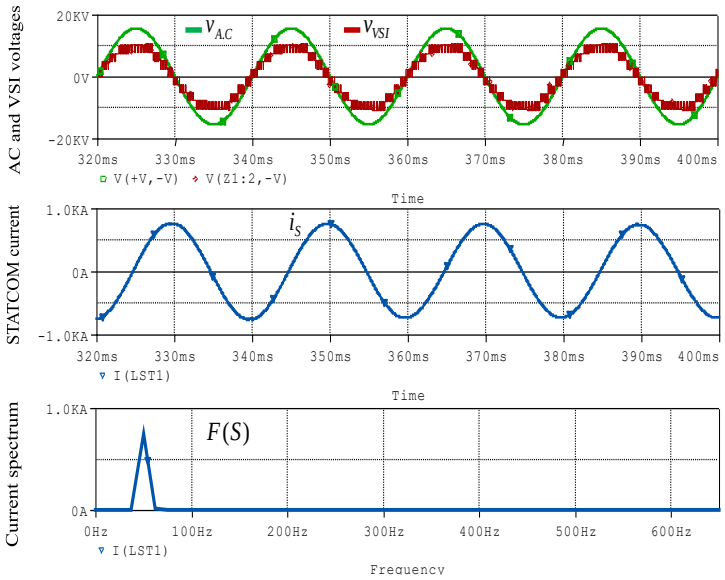



Figure 11. STATCOM steady state performance at maximum inductive current demand

The performance of the proposed STATCOM during an abrupt change in current demand from maximum inductive reactive current to maximum reactive capacitive current is revealed in Figure 13. The abrupt change in current demand occurred at t=300msec. The transition time was about 140 msec. This period of time is required to charge the STATCOM DC capacitors from minimum voltage to maximum voltage. The transition period is governed by the series reactor parameters (resistance and inductance) and the DC capacitor values. High loss reactors significantly reduce the transition time. The frequency spectrums of the STATCOM current in the above steady state tests indicate that it is a harmonic-free reactive device, thus it can be represented by a harmonic-free compensating susceptance. Many tests were carried out on this STATCOM during steady state operation to verify its linearity. The results of those tests are reflected by the graph shown in Figure 14. The devised controller of this STATCOM makes it linearly and continuously controlled within a STATCOM angle range of -5.72° to +5.72°. This is verified by the graph shown in Figure 14. The minus sign in Figure 14 is related to inductive reactive currents.

The STATCOM choppers are responsible for equalizing the voltages of the DC capacitors. Different DC voltages mean generation of current harmonics besides the STATCOM fundamental current. These current harmonics will be injected to the power system network. Figure 15 shows choppers currents at different reactive current demands.

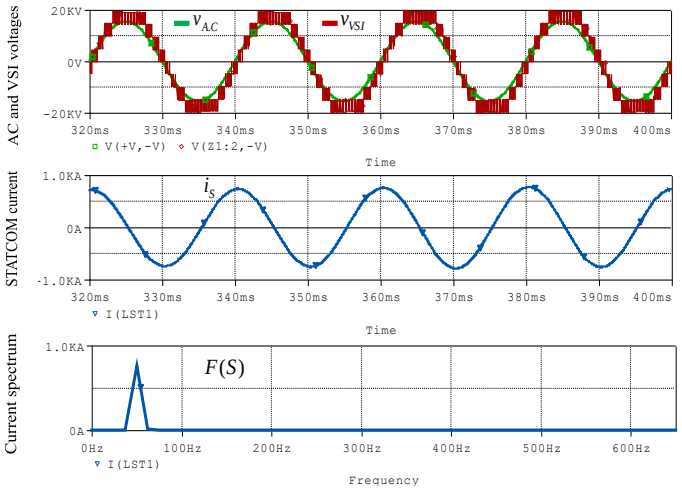



Figure 12. STATCOM steady state performance at maximum capacitive current demand

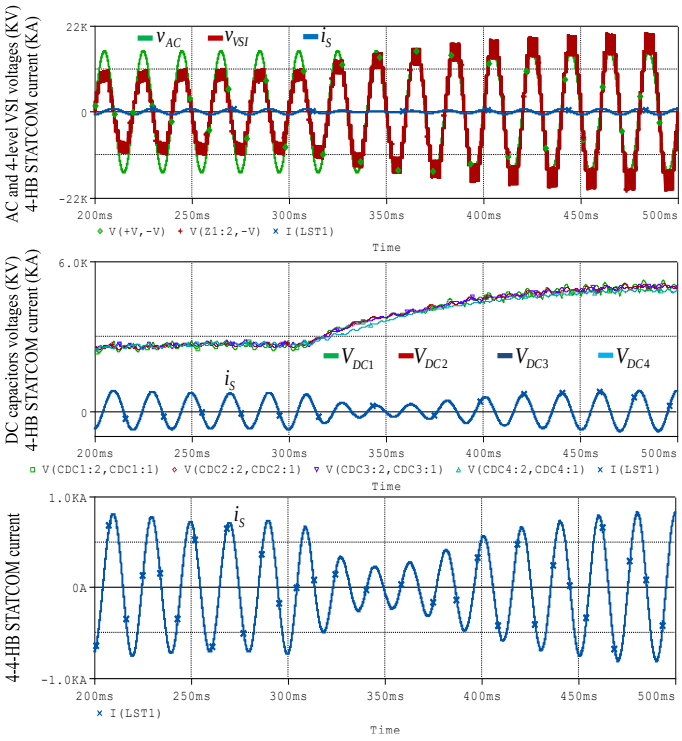



Figure 13. The treatment of the 11 KV, 50Hz 4-HB STATCOM to abrupt change in current demand from maximum inductive reactive current to maximum reactive capacitive current

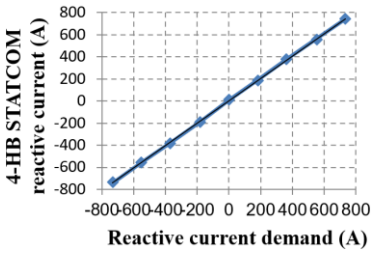



Figure 14. STATCOM steady state reactive current against reactive current demand

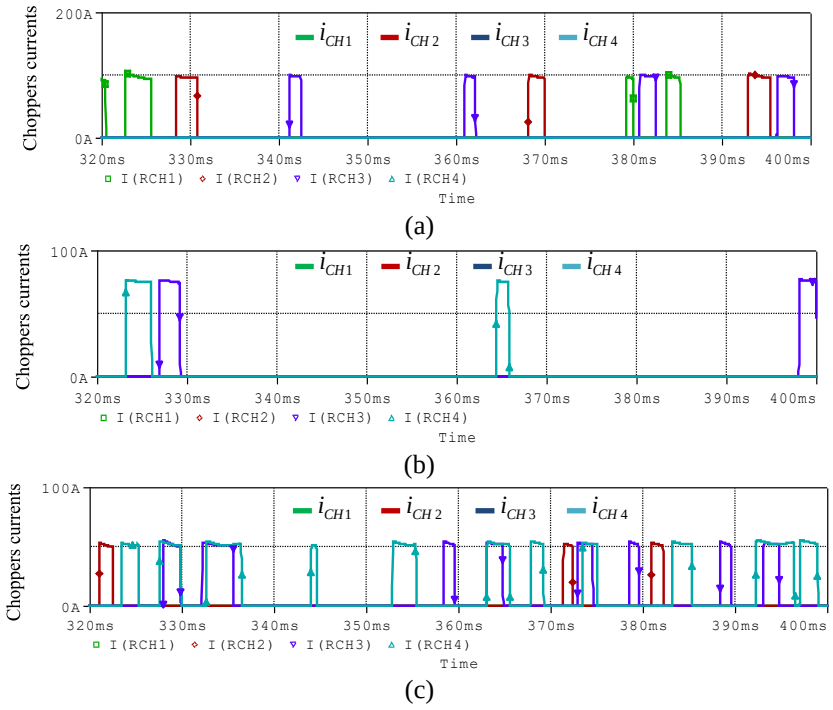



Figure 15. DC choppers currents of the 4-HB STATCOM during different reactive current demand: (a) maximum capacitive, (b) zero, and (c) maximum inductive

## 4. CONCLUSION

The compensating susceptance devised from 4-HB STATCOM is governed by a new adaptive controlling technique and equipped with a voltage equalizer to its DC capacitor voltages. The devised controlling technique makes the STATCOM respond precisely to current demand in a very short time compared with other techniques employing the same passive elements and switching frequency. The controller guarantees continuously and linearly controlled reactive current (inductive and capacitive) without noticeable association harmonics. The DC capacitor voltage of each H-bridge is stabilized by the second harmonic filter installed in parallel with the DC capacitor. This additional modification reduces the need to larger DC capacitor. The 11 KV, 50 Hz 4-HB STATCOM is not in need of charging its DC capacitors initially because it is equipped with a utilized method for charging them rapidly by disabling the STATCOM carrier for a certain period sufficient to build up the required level of DC voltages. This property make this STATCOM adaptive compared to other STATCOMs, since most controlling schemes depending switching frequency control require determined initial values for DC capacitor in order to guarantee balancing them within certain tolerances. This STATCOM is promoted to be deservingly exploited in load balancing systems, which are representing the significant tools for achieving big amount of energy savings in power generation and big reduction in transmission losses.

## REFERENCES

[1] Q. Song, W. Liu, and Z. Yuan, "Multilevel optimal modulation and dynamic control strategies for STATCOMs using cascaded multilevel inverters," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1937–1946, 2007, doi: 10.1109/TPWRD.2007.899771.

[2] H. Akagi, S. Inoue, and T. Yoshii, "Control and performance of a transformerless cascade PWM STATCOM with star configuration," *IEEE Transactions on Industry Applications*, vol. 43, no. 4, pp. 1041–1049, 2007, doi: 10.1109/TIA.2007.900487.

[3] S. Hirve, K. Chatterjee, B. G. Fernandes, M. Imayavaramban, and S. Dwari, "PLL-less active power filter based on one-cycle control for compensating unbalanced loads in three-phase four-wire system," *IEEE Transactions on Power Delivery*, vol. 22, no. 4, pp. 2457–2465, 2007, doi: 10.1109/TPWRD.2007.893450.

[4] H. Iman-Eini, J. L. Schanen, S. Farhangi, and J. Roudet, "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers," *IEEE Transactions on Power Electronics*, vol. 23, no. 5, pp. 2428–2442, 2008, doi: 10.1109/TPEL.2008.2002055.

[5] J. A. Barrena, L. Marroyo, M. Á. Rodriguez Vidal, and J. R. Torrealday Apraiz, "Individual voltage balancing strategy for PWM cascaded H-bridge converter-based STATCOM," *IEEE Transactions on Industrial Electronics*, vol. 55, no. 1, pp. 21–29, 2008, doi: 10.1109/TIE.2007.906127.

[6] B. Singh, P. Jayaprakash, T. R. Somayajulu, and D. P. Kothari, "Reduced rating VSC with a zig-zag transformer for current compensation in a three-phase four-wire distribution system," *IEEE Transactions on Power Delivery*, vol. 24, no. 1, pp. 249–259, 2009, doi: 10.1109/TPWRD.2008.2005398.

[7] Y. Xu, L. M. Tolbert, J. D. Kueck, and D. T. Rizy, "Voltage and current unbalance compensation using a static var compensator," *IET Power Electronics*, vol. 3, no. 6, pp. 977–988, 2010, doi: 10.1049/iet-pel.2008.0094.

[8] H. M. Pirouz and M. T. Bina, "Modular Multilevel Converter Based STATCOM Topology Suitable for Medium-Voltage

Unbalanced Systems," *Journal of Power Electronics*, vol. 10, no. 5, pp. 572–578, Sep. 2010, doi: 10.6113/JPE.2010.10.5.572.
[9] A. M. Obais and J. Pasupuleti, "Design of a continuously controlled linear static Var compensator for load balancing and power factor correction purposes," *International Review on Modelling and Simulations*, vol. 4, no. 2, pp. 803–812, 2011.
[10] M. Hagiwara, R. Maeda, and H. Akagi, "Negative-Sequence Reactive-Power Control by a PWM STATCOM Based on a Modular Multilevel Cascade Converter (MMCC-SDBC)," *IEEE Transactions on Industry Applications*, vol. 48, no. 2, pp. 720–729, Mar. 2012, doi: 10.1109/TIA.2011.2182330.
[11] X. Yang, "A design approach for DC voltage controller of CHB-based STATCOM," *WSEAS Transactions on Circuits and Systems*, vol. 12, no. 5, pp. 141–150, 2013.
[12] A. M. Obais and J. Pasupuleti, "Design of an almost harmonic-free TCR," *Research Journal of Applied Sciences, Engineering and Technology*, vol. 7, no. 2, pp. 388–395, 2014, doi: 10.19026/rjaset.7.266.
[13] A. M. Obais and J. Pasupuleti, "Automatic power factor correction using a harmonic-suppressed TCR equipped with a new adaptive current controller," *Journal of Power Electronics*, vol. 14, no. 4, pp. 742–753, 2014, doi: 10.6113/JPE.2014.14.4.742.
[14] W. T. Nunes, L. F. Encarnação, and M. Aredes, "An improved asymmetric cascaded multilevel D–STATCOM with enhanced hybrid modulation," *Electronics* , vol. 4, no. 2, pp. 311–328, 2015, doi: 10.3390/electronics4020311.
[15] E. Kontos, G. Tsolaridis, R. Teodorescu, and P. Bauer, "Full-bridge MMC DC fault ride-through and STATCOM operation in multi-terminal HVDC grids," *Bulletin of the Polish Academy of Sciences: Technical Sciences*, vol. 65, no. 5, pp. 653–662, 2017, doi: 10.1515/bpasts-2017-0070.
[16] G. Farivar, C. D. Townsend, B. Hredzak, J. Pou, and V. G. Agelidis, "Low-Capacitance Cascaded H-Bridge Multilevel StatCom," *IEEE Transactions on Power Electronics*, vol. 32, no. 3, pp. 1744–1754, 2017, doi: 10.1109/TPEL.2016.2557351.
[17] G. T. Son and J. W. Park, "Current limit strategy of voltage controller of delta-connected H-bridge STATCOM under unbalanced voltage drop," *Journal of Electrical Engineering and Technology*, vol. 13, no. 2, pp. 550–558, 2018, doi: 10.5370/JEET.2018.13.2.550.
[18] K. Varalakshmi, R. L. Narasimham, and G. Tulasi Ramdas, "Eccentric operation of STATCOM using predictive controller," *International Journal of Power Electronics and Drive Systems*, vol. 9, no. 1, pp. 150–156, 2018, doi: 10.11591/ijpeds.v9.i1.pp150-156.
[19] A. A. Z. Diab, T. Ebraheem, R. Aljendy, H. M. Sultan, and Z. M. Ali, "Optimal design and control of MMC STATCOM for improving power quality indicators," *Applied Sciences (Switzerland)*, vol. 10, no. 7, 2020, doi: 10.3390/app10072490.
[20] A. Miremad, K. K. Monfared, H. Iman-Eini, and Y. Neyshabouri, "Design and control of a STATCOM based on hybrid cascaded H-bridge and full-bridge neutral point clamped multilevel inverter," *IET Power Electronics*, vol. 13, no. 17, pp. 4019–4030, 2020, doi: 10.1049/iet-pel.2020.0726.
[21] T. Ahmed, A. Waqar, R. M. Elavarasan, J. Imtiaz, M. Premkumar, and U. Subramaniam, "Analysis of Fractional Order Sliding Mode Control in a D-STATCOM Integrated Power Distribution System," *IEEE Access*, vol. 9, pp. 70337–70352, 2021, doi: 10.1109/ACCESS.2021.3078608.
[22] S. G. Mian, P. D. Judge, A. Junyent-Ferr, and T. C. Green, "A Delta-Connected Modular Multilevel STATCOM with Partially-Rated Energy Storage for Provision of Ancillary Services," *IEEE Transactions on Power Delivery*, vol. 36, no. 5, pp. 2893–2903, 2021, doi: 10.1109/TPWRD.2020.3029312.
[23] I. Marzo, A. Sanchez-Ruiz, J. A. Barrena, G. Abad, and I. Muguruza, "Power balancing in cascaded H-Bridge and modular multilevel converters under unbalanced operation: A review," *IEEE Access*, vol. 9, pp. 110525–110543, 2021, doi: 10.1109/ACCESS.2021.3103337.
[24] V. F. Pires, A. Cordeiro, D. Foito, and J. F. Silva, "A Multilevel Converter Topology for a STATCOM System Based on Four-Leg Two-Level Inverters and Cascaded Scott Transformers," *IEEE Transactions on Power Delivery*, vol. 37, no. 3, pp. 1391–1402, 2022, doi: 10.1109/TPWRD.2021.3086399.
[25] J. Ballestín-Fuertes, J. F. Sanz-Osorio, J. Muñoz-Cruzado-Alba, E. L. Puyal, J. Leiva, and J. R. Rivero, "Four-Legs D-STATCOM for Current Balancing in Low-Voltage Distribution Grids," *IEEE Access*, vol. 10, pp. 779–788, 2022, doi: 10.1109/ACCESS.2021.3138827.

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