International Journal of Power Electronics and Drive Systems (IJPEDS)
Vol. 14, No. 4, December 2023, pp. 2107~2118
ISSN: 2088-8694, DOI: 10.11591/ijpeds.v14.i4.pp2107-2118

Biopotential multi-path current feedback instrumentation amplifier with automatic offset cancellation loop for resistive bridge microsensors

Younes Laababid, Karim El Khadiri, Ahmed Tahiri
Laboratory of Computer Science and Interdisciplinary Physics (LIPI), Normal Superior School Fez (ENSF),
Sidi Mohamed Ben Abdellah University, Fez, Morocco

Article Info

Article history:

Received Mar 25, 2023
Revised May 13, 2023
Accepted May 25, 2023

Keywords:

AOCL
CMRR
Multi-path CFIA
NEF
RRL

ABSTRACT

This study introduces a refined current feedback instrumentation amplifier (CFIA) specifically designed for amplifying biopotential signals that originate from resistive-bridge sensors. The proposed architecture uniquely incorporates a multipath chopper-stabilized CFIA which has been developed to minimize the effects of bridge offsets, while maintaining low power usage, high input impedance, and reduced noise characteristics. The engineering blueprint employs a ripple reduction loop (RRL) to mitigate output ripple caused by chopper up-modulation. To speed up offset cancellation and to limit the offset caused by bridge mismatch, an automatic offset cancellation loop (AOCL) circuit is integrated within the analog front end (AFE). Crafted using a conventional 0.18 µm CMOS process, the CFIA in this design provides adjustable gain between 20.35 dB to 55.14 dB, with a power supply rejection ratio (PSRR) and a common mode rejection ratio (CMRR) of 103 dB and 114 dB, respectively. The system demonstrates an input-referred noise (IRN) value of 16 ηV/√Hz at 200 Hz frequency, equivalent to a noise efficiency factor (NEF) of 5.18. Operating from a supply voltage of 1.8V, the AFE shows a power consumption of 291 µW.

Corresponding Author:

Younes Laababid
Laboratory of Computer Science and Interdisciplinary Physics (LIPI)
Normal Superior School Fez (ENSF), Sidi Mohamed Ben Abdellah University Laboratory
Fez, Morocco
Email: Younes.Laababid@usmba.ac.ma

1. INTRODUCTION

Micro-electro-mechanical systems (MEMS) technology is currently gaining significant attention due to the inherent advantages of miniaturization, high signal-to-noise ratio (SNR), and affordability, which has led to its ubiquitous application across a plethora of sensing devices [1]. Among these, resistive MEMS sensors stand out, offering a unique combination of structural simplicity, superior linearity, and robust durability, making them an optimal choice for the detection of various data, including but not limited to biological signals [2]–[6].

Additionally, MEMS resistive sensors require a change to detect an amount of physical change. This resistive change converts to a low amplitude voltage [7], [8]. For this reason, a good use for MEMS resistive bridge sensors in electromyogram (EMG), electrocardiogram (ECG) and electroencephalogram (EEG) bio-potential signals, is an instrumentation amplifier with high precision signal processing low noise thanks to its high gain and CMRR also, thus eliminating offset voltages by an automatic offset cancellation circuit [9].

The amplitude of biopotential signals typically lies within a minute range of about 5 µV to 20 mV, and these signals operate within the frequency domain of 0 Hz to 1 kHz [10]. As such, the main objective in

designing an instrumentation amplifier for these signals is to prioritize the achievement of low noise, minimal power usage, and enhanced input impedance [11]. When it comes to quantifying energy efficiency and evaluating the trade-off between power consumption and noise in biomedical devices, the Noise efficiency factor (NEF) often serves as the standard measure [12]. It is calculated as in (1).

$$NEF = V_{\text{ni,rms}} \sqrt{\frac{2I_{\text{tot}}}{\pi.U_{\text{T}}.4KT.BW}} \quad (1)$$

Where $V_{\text{ni,rms}}$ is the input referred noise voltage (IRN), I_{tot} is the current, U_T is the thermal voltage, k is Boltzmann's constant, T is the temperature in Kelvins (body temperature =300 K), and BW is the bandwidth of the system in Hz.

The capacitively coupled instrumentation amplifier (CCIA) plays a significant role in precise biopotential measurements. Its purpose is to eradicate DC offset at the electrode-skin interface, effectively blocking undesired potential signals. However, it's worth noting that the CCIA's input impedance is adversely affected by its input capacitance, which results in a lower impedance. As the chopper's frequency escalates, this problem can trigger a decrease in signal amplitude and a reduction in the common-mode rejection ratio (CMRR), consequently influencing measurement precision [13]. A noteworthy correlation can be drawn between the input capacitance of the CCIA and the input impedance.

$$Z_{\text{in}(CCIA)} = \frac{2}{sCin} \quad (2)$$

The current feedback instrumentation amplifier (CFIA) incorporates an input transconductance stage [14], setting it apart from alternate amplifier configurations and contributing to its potential for attaining a high common mode rejection ratio (CMRR) [15]. The CFIA achieves high input impedance effectively by utilizing the gate input capacitance of the input transconductance (Cg). This capacitance includes parasitic capacitors (Cp1, Cp2, and Cp3), coupled with the switched-capacitor (SC) resistor (CH1) of the input chopper. The combined effect of these components plays a crucial role in determining the final input impedance.

$$Z_{\text{in}}(CFIA) = \frac{2}{sC_g} \approx \frac{2}{2\pi f_{chop} C_g} \quad (3)$$

Figure 1 shows the tripartite structure of the CFIA's amplification stages. The overall amplification of the CFIA is shown as (4).

$$G_{CFIA} \approx \frac{G_{m1}}{G_{m2}}\left(1 + 2\frac{R_2}{R_1}\right) \quad (4)$$

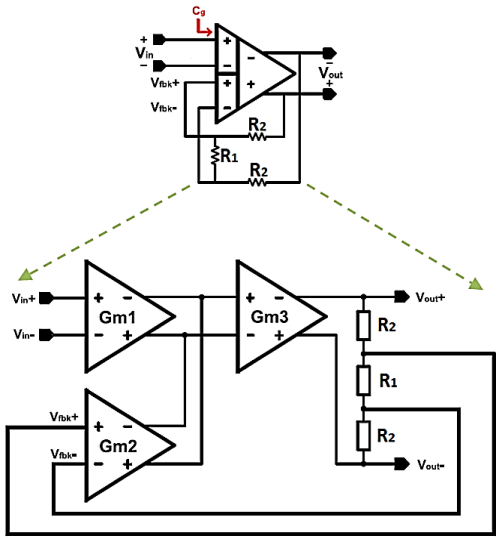


Figure 1. Structural design of CFIA

Trans conductors Gm1 and Gm2 serve the crucial role of converting the input voltage and the feedback voltage to currents in a complementary fashion. A noteworthy prerequisite for attaining substantial and accurate

amplification necessitates the matching of Gm1 and Gm2, as stipulated in [16]. Techniques aimed at reducing noise are vital in fabricating a neural signal amplifier, having the potential to curb the flicker noise that leads to a decrease in biopotential signals emanating from resistive bridges. Two notable strategies-chopper stabilization (CHS) and automatic zeroing (AZ) - have been identified as effective means to attenuate the impact of noise density and DC offset in the baseband, as referenced in [17].

In our research, we introduce a unique analog front-end (AFE) configuration, specifically designed for resistive bridge microsensors. The emphasis in this proposed AFE is on minimal power consumption and noise reduction, achieved by incorporating a chopper-stabilized multipath current-feedback class-AB CFIA and an automatic offset cancellation loop developed. The CFIA applies chopper stabilization methods to effectively reduce offset and 1/f noise. Additionally, the incorporation of a ripple reduction loop (RRL) aims to diminish output ripple. To evaluate the AFE's performance, we built and simulated it using a 180 nm CMOS technology framework and powered it with a 1.8V power supply.

The rest of the parts of the paper are organized as follows: i) Section 2 gives an overview of the resistive bridge AFE design as well as the architecture and sub-blocks; ii) Simulation results and comparisons are described in section 3; and iii) Finally, the conclusion and upcoming work are discussed in section 4.

2. DESIGN AND METHOD

2.1. Overall circuit design

In the field of biomedical signal measurements, the sensitivity of sensors is paramount. They need to be capable of accurately and precisely gauging weak signals while mitigating distortion. In light of this, crafting an appropriate analog front end (AFE) becomes crucial to ensuring high-quality readings. This paper takes cues from previous work [18] to construct a low-noise AFE specifically designed for resistive bridge microsensors. The proposed AFE circuit's topology, depicted in Figure 2, incorporates several components: a multipath CFIA, a 2nd-order low-pass filter (LPF), a buffer, a 12-bit successive approximation register analog-to-digital converter (SAR-ADC), and an automatic offset cancellation loop (AOCL) that features an R-2R digital-to-analog converter (DAC).

The advanced fully differential CFIA under discussion has the capacity to augment the input signal transmuted by the resistive bridge in the first stage. The output stage of the CFIA might encounter an undesired offset from the resistive bridge amid the amplification process. Hence, an AOCL circuit is employed to rectify the external offset originating from the mismatch of the bridge. Internal offsets within the HFP are maintained stable by a high-gain LFP amplifier and a low noise chopper amplifier. To mitigate the output fluctuation engendered by the up-modulated DC offset in the LFP, the employment of an AC-coupled RRL [15]–[18] is seen as a viable strategy.

2.2. Proposed multipath current feedback instrumentation amplifier

The structure of the multipath CFIA is composed of two primary channels - the low frequency path (LFP) and the high frequency path (HFP), as represented in Figure 3. In order to mitigate the effects of 1/f noise and DC offset within the baseband, the LFP employs the CHS technique [19], whereas the RRL is incorporated to restrain the up-modulated ripple. For the purpose of maintaining stability in the CFIA at lower frequencies, Cm2 is introduced to the multipath in conjunction with the compensation capacitors Cm, thereby equating C_{m2} with C_{m1}. The frequency value at unity gain is.

$$f_0 \approx \frac{G_{m11}}{2\pi C_{m5}} \approx \frac{G_{m21}}{2\pi C_{m2}} \quad (5)$$

At the DC operating point, Gm11 = Gm21 = 156 µA/V and Cm51 = 49 pF, so the UGBW is 506 kHz. The LFP consists of five stages this is why its gain is very large compared to the gain of HFP, to obtain an offset-stabilized for the latter which has a residual offset at the input (Gm11). According to (6), we need to strengthen the LFP's gain in order to remove the HFP's offset, therefore Gm3 is designed as a gain-boosted single-stage folded-cascode OTA to reinforce the DC gain and bring down the HFP's offset to 1 µV [15]. The residual input offset can be expressed as (6) [20].

$$V_{offset} \approx \frac{G_{HFP}}{G_{LFP}} \; V_{os,\,in} \quad (6)$$

$V_{os,in}$ here refers to the offset of Gm11. Internal offset stabilization is achieved by transmuting the offset voltage Vos21 into a current, denoted Ios21, at the output of Gm21. This current, once rippled by CH3 modulation, is transformed into a triangle-wave voltage, symbolized by (V), via a Miller integrator (Gm3). Interestingly, the ripple at the output of Gm3 can be represented as (7).

$$V_{Ripple} \approx \frac{V_{os21}.G_{m21}}{2f_{chop}.C_{m31}} \approx \frac{I_{os21}}{2f_{chop}.C_{m31}} \quad (7)$$

The ripple voltage at Gm3's output will be integrated once again by Gm5 as a sinusoidal ripple at the CFIA's output, and its amplitude may then approximately be estimated using (8).

$$V_{Ripple,\,out} \approx V_{Ripple}\frac{G_{m4}}{8f_{chop}.C_{m51}} \quad (8)$$

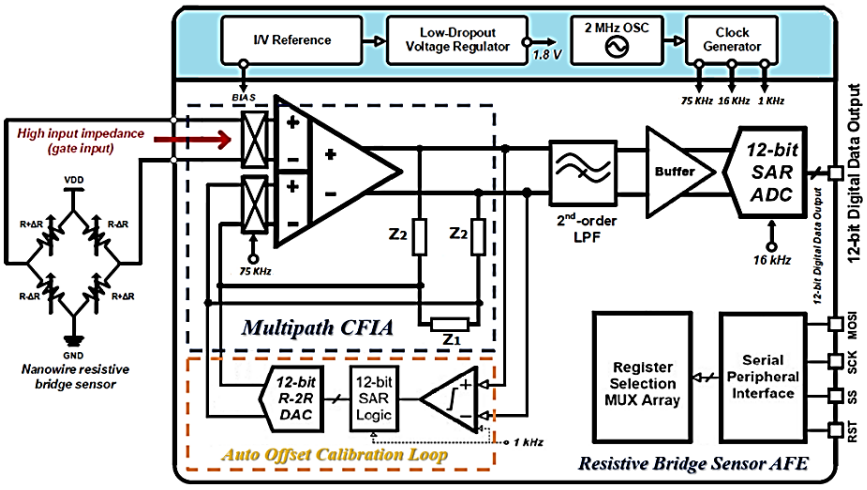


Figure 2. Overall structural layout of the proposed AFE circuit

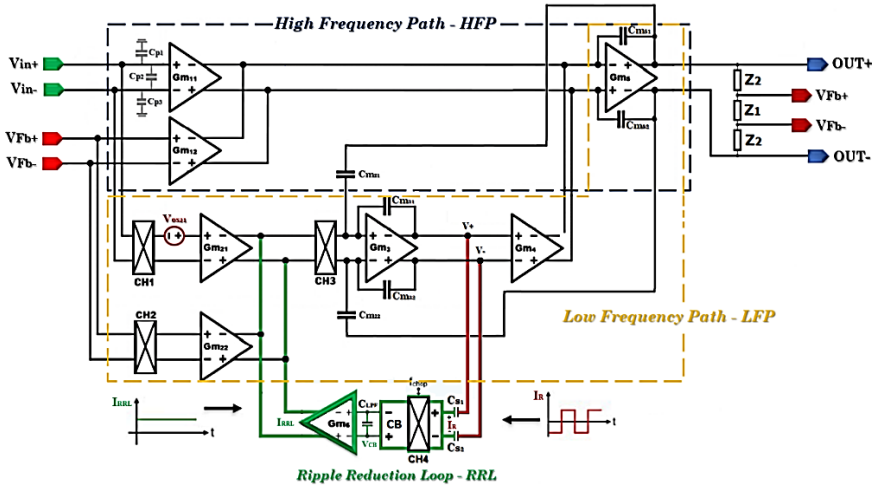


Figure 3. Schematic of the multi-path chopper current feedback instrumentation amplifier

The high frequency ripple of the converted voltage generated at the output of Gm3 is sensed, demodulated and converted into a compensation current by the RRL with good impact, which consists of an input AC coupling capacitors Cs, a current buffer (CB), a CLPF capacitor to mitigate the RRL's second-harmonic ripple when using with output impedance of a current buffer (CB), and a transconductance Gm6. The ripple voltage is transformed by Cs into the current IR, which CH4 then demodulates into DC. The current at the input of CB is given by (9).

$$|IR| \approx |VRipple|.2fchop.C_s \quad (9)$$

As a result, the current, referred to as IR, at the CB's output can be estimated as presented in (10). Here, VCB signifies the output voltage of CB, RCB stands for the DC output impedance of CB, and ACB represents the DC voltage gain of the NMOS cascode in CB.

$$|IR| \approx \frac{VCB}{RCB} \approx \frac{VCB.2fchop.C_s}{ACB} \quad (10)$$

Accordingly, to enhance ripple suppression, the CB is mounted as a gain-boosted Current Buffer. The two output currents of Gm21 and Gm22 merge with the output current of Gm6 (ripple) in (11) to return negatively to the input of CH3.

$$IRRL \approx \frac{Vos21.G_{m21}.ACB.G_{m6}}{2fchop.C_{m31}} \approx \frac{Ios21.ACB.G_{m6}}{2fchop.C_{m31}} \quad (11)$$

The voltage without ripple is transformed to a current through Gm4 and is mixed with the HFP currents and integrated through Gm5. As a result, the ripple is reduced more effectively. The design of current buffer (CB) with in RRL [15] is shown in Figure 4.

The suggested block diagram of the CFIA circuit with feedback can be seen in Figure 5, which is adopted an AC-coupled capacitive feedback network with a parallel pseudo- resistor, in hopes of reducing the chip area and give the low-frequency attenuation properties. We may create a high-pass transfer function using the capacitive feedback [21]. The transfer function of the CFIA can be expressed as (12) without the compensation voltage of DAC.

$$GCFIA \approx \frac{1+sRF.(CF_1+2CF_2)}{1+sCF_1.RF} \approx 1 + 2\frac{CF_2}{CF_1} \quad (12)$$

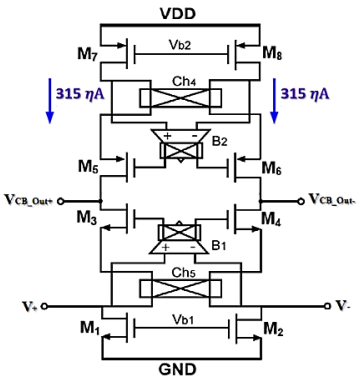


Figure 4. Current buffer design

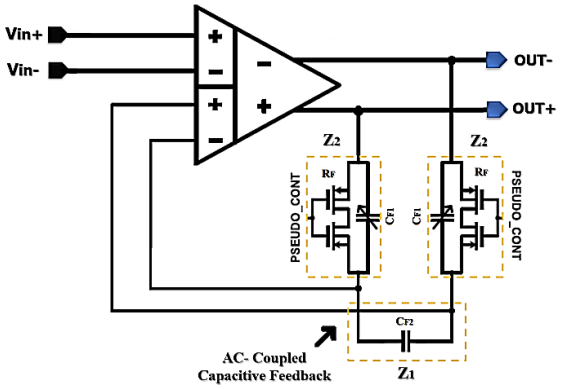


Figure 5. Block diagram of the CFIA circuit with feedback

The SPI enables gain adjustments via a 5-bit programmable weighted capacitor array, CF1, facilitated by controlling each switch within the capacitor array. The range for this programmable gain spans from 20 dB (00000) to 55 dB (11111). The multipath CFIA utilizes a chopping frequency of 75 kHz, synchronized with the non-overlapping clocks.

The detailed representation of the HFP within the suggested CFIA is provided in Figure 6(a). This configuration includes a class-AB output stage, Gm5, along with non-chopped input trans conductors Gm11 and Gm12. The currents transitioned via the trans conductors stages Gm11, Gm12, and Gm4, are combined by an active Miller-compensated class-AB output stage Gm5 [22]. At the Gm5 juncture, the class-AB biasing and elevation of power efficiency is executed through a Monticelli-style floating setup using MP14, MN5, MP15, and MN6. Notably, this Monticelli style is also crucial in curbing signal distortion [23]. The addition of an error amplifier CMFB circuit in the HFP assists in managing the bias current of the cascode stages, thereby ensuring a higher differential output range with minimal power consumption [24]. Figure 6(b) showcases the CMFB. To compensate for the frequency response within the HFP, a nested Miller compensation technique is employed [25].

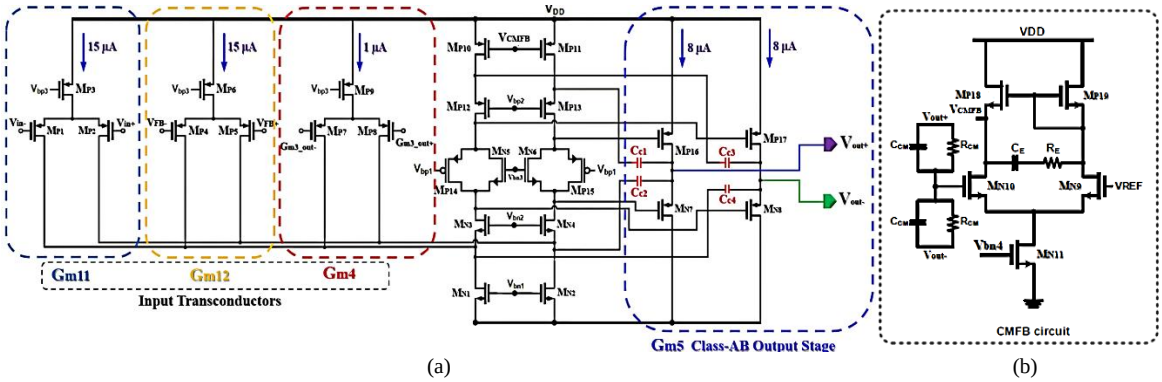
It's important to note that the input referred noise (IRN) of the CFIA is predominantly influenced by the LFP and input stage of the HFP. The IRN dominated by the HFP's input stage, inclusive of thermal and flicker noise components, can be approximated as (13).

$$\overline{V^2_{n,in}} \approx \frac{16KT}{3.g_{m1}}\left[1+\eta\frac{g_{mn2}}{g_{m1}}+\frac{g_{m10}}{g_{m1}}\right]+\frac{2}{C_{ox}f}\left[\frac{KF_1}{W_1L_1}+\frac{KF_2g_{mn2}^2}{W_2L_2g_{m1}^2}+\frac{KF_{10}g_{m10}^2}{W_{10}L_{10}g_{m1}^2}\right]$$

$$\approx \frac{16KT}{3.g_{m1}}\left[1+\eta\frac{g_{mn2}}{g_{m1}}+\frac{g_{m10}}{g_{m1}}\right]+\frac{2}{C_{ox}fW_1}\left[\frac{KF_1}{L_1}+\frac{\mu_n}{\mu_p}\frac{L_1KF_2}{L_2^2}.\frac{ID_2}{ID_1}+\frac{\mu_n}{\mu_p}\frac{L_1KF_{10}}{L_{10}^2}.\frac{ID_{10}}{ID_1}\right] \quad (13)$$

Where μ is the effective mobility of the MOSFET, f is the signal frequency, KF is the process-dependent flicker noise coefficient of MOSFET, Cox is the gate-oxide capacitance of M1,2 and K is the Boltzmann constant. At low frequencies, the thermal noise of the LFP's input stage is dominated, is calculated as (14).

$$\overline{V^2\text{n, th}} \approx 2.\left[\frac{\gamma 4KT}{G_{\text{m21}}} + \frac{\gamma 4KT}{G_{\text{m22}}}\right] \quad (14)$$



(a) (b)

Figure 6. Schematic of the HFP circuit: (a) the high-frequency path in CFIA and (b) the CMFB circuit

2.3. Suggested automatic offset calibration loop circuit design

In response to the offset issue that emerges from the amplification of the resistive bridge sensor at the CFIA's output stage, an automatic offset calibration loop circuit (AOCL) is proposed. The aim of this circuit is to alleviate the unwanted offset [26].

The AOCL comprises a comparator, a 12-bit successive approximation register (SAR) logic module, and a 12-bit R-2R digital-to-analog converter (DAC) [27], as illustrated in Figure 7. During the calibration process, the comparator evaluates the amplified offset that stems from the bridge at the CFIA output node. The result from the comparator then triggers the 12-bit SAR logic, which in turn generates a 12-bit digital control signal intended for the DAC. This signal is subsequently inputted into the 12-bit R-2R DAC [18]–[27]. Consequently, the DAC produces the necessary voltage for offset correction.

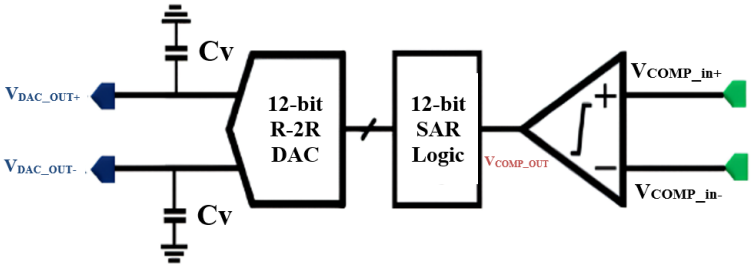


Figure 7. Auto offset calibration loop circuit (AOCL)

A Dynamic Comparator was employed in our design, which makes use of a StrongARM latch architecture, to evaluate the amplified bridge offset at the CFIA output node. The StrongARM latch structure, as represented in Figure 8, shows power efficiency and reduced offset. This design includes a differential pair input, two sets of cross-coupled transistors M3-M6, four clocked PMOS switches S1-S4, and an SR-latch. The SR-latch is responsible for latching the differential outputs and generating VCOMP_OUT. The offset impact of transistors M3-M6 is reduced by deactivating them initially through the pre-charging operation of PMOS switches S1 to S4 [28]. This feature provides the StrongArm architecture with increased offset compensation resilience.

Within the AOCL, the 12-Bit SAR control logic is organized around two sequences of edge-triggered D flip-flops, which sequentially determine each bit. Each D flip-flop is engineered with a transmission gate (TG) and inverters. The first sequence of flip-flops operates as a shift register, receiving data from the comparator. On the other hand, the second sequence of flip-flops functions as a data storage module, with the responsibility of generating the DAC control input, as shown in Figure 9 [29].

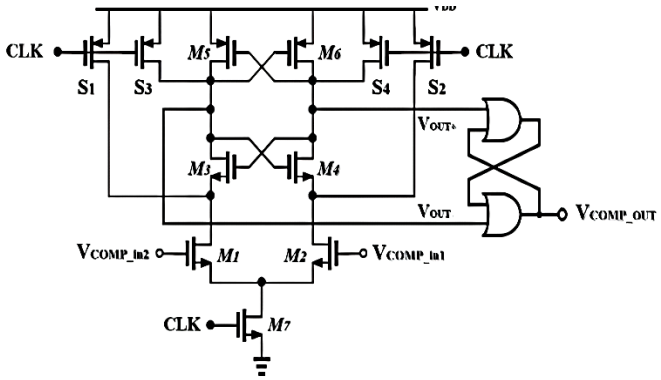


Figure 8. Strong arm latch topologies in AOCL

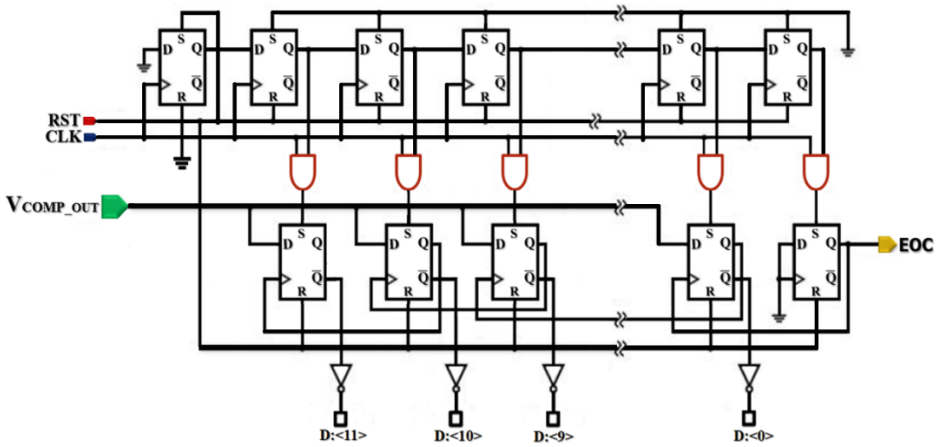


Figure 9. Layout of the 12-bit SAR control logic within the AOCL

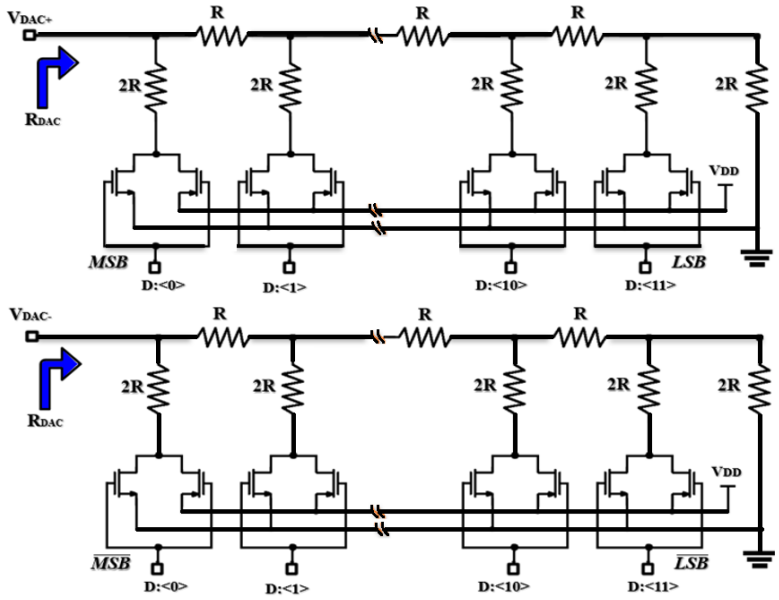


Figure 10. Visual representation of the R-2R DAC's structure within the AOCL

Initially, the SAR is reset, positioning the most significant bit (MSB) of the DAC input at '1', while setting the least significant bit (LSB) bits to '0'. As the comparator evaluates the output offset, VCOMP_OUT progressively modifies the state of MSB and LSB. The end of conversion (EOC) flag is set high (H) upon

completion of offset compensation, signifying the end of the AOCL operation. A capacitor (Cv) is integrated at the output of the DAC to expedite the calibration time for the AOCL operation.

The layout of the R-2R DAC circuit is presented in Figure 10. We employ an R-2R ladder network to enhance precision, albeit at the expense of increased area requirements. The resistors are linked either to a high voltage or to the ground, mediated by a transmission gate. This gate amalgamates a PMOS and an NMOS, with their gates connected to the incoming voltage and their drains merged at a common node. A particular challenge that arises in designing an R-2R DAC is maintaining monotonicity [30]. This is manifested when an increase in the input could potentially result in a decrease in the output. One approach to mitigate this issue involves minimizing the resistance of the transmission gate, achieved by widening it to facilitate smoother current flow within the circuit.

3. RESULTS AND DISCUSSION

The analog front end (AFE) was both simulated and implemented in Cadence using TSMC's 0.18µm technology. It was designed to operate at a supply voltage of 1.8V, consuming only 291 µW of energy, with a total bias current of 162 µA. Figure 11 depicts the measured transfer function of the current feedback instrumentation amplifier (CFIA). The AFE incorporates a multi-path chopper stabilized architecture to mitigate notches caused by the amplifier's transfer function within the chopper frequency band. As a result, the bandwidth is expanded while maintaining a low noise performance [31]. It is evident from the measurements that a gain of 50.77 dB is achieved within the 0.1-1.5 KHz bandwidth. Figure 12 illustrates the programmable gain settings, ranging from a gain of 20.35 dB for (<DIN> = 00000) up to 55.14 dB for (<DIN> = 11111). The unit gain bandwidth (UGBW) is measured at 500 kHz, and the phase margin at UGBW is 77.5°. These results demonstrate that the AFE effectively amplifies weak signals from the resistive bridge sensor while minimizing noise interference.

Figure 13 and Figure 14 show the measured CMRR and PSRR, which report 114 dB and 103 dB respectively over the range of 0.1 to 100 Hz. Figure 15 displays the CFIA's transient response to a sine wave input with a 10-mV amplitude and a 1 kHz frequency. The total IRN of the CFIA is shown in Figure 16, which indicates that the IRN is 70 ηV/√Hz at 1 Hz and 16 ηV/√Hz at 200 Hz.

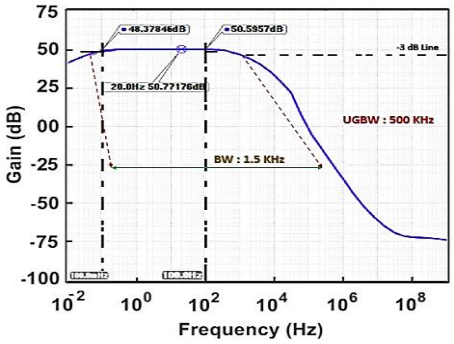


Figure 11. Transfer function of the CFIA

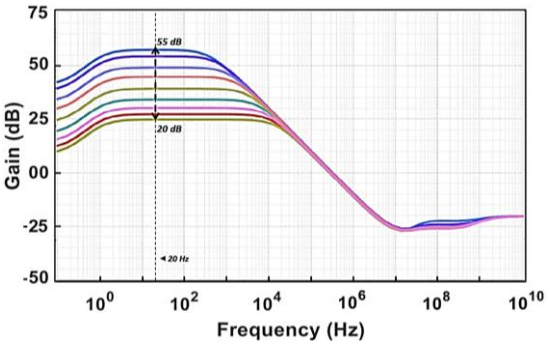


Figure 12. AC Programmable transfer function gain simulation results of CFIA

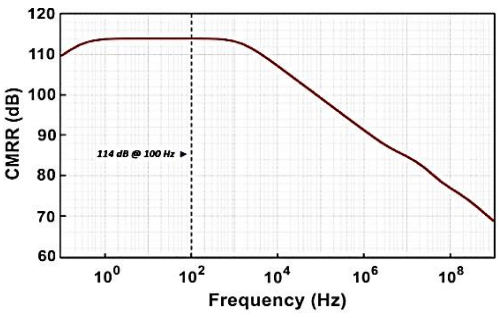


Figure 13. CMRR simulation results

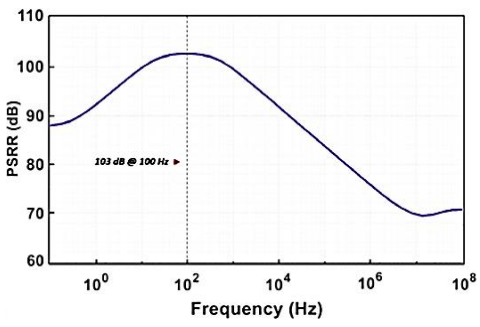


Figure 14. PSRR simulation results

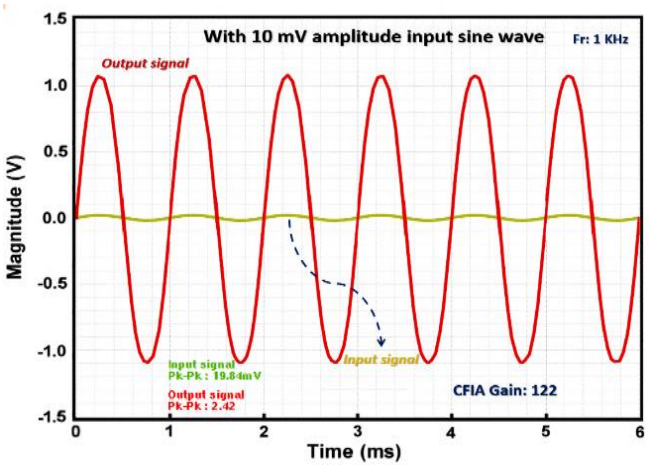


Figure 15. Transient response of CFIA

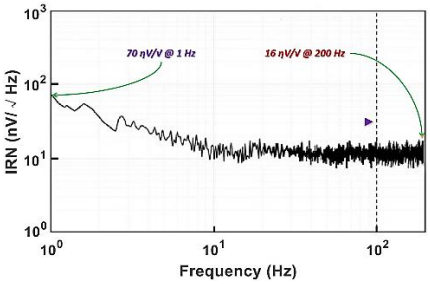


Figure 16. Input-referred noise voltage spectral density of CFIA

Figure 17 displays the simulation results of the automatic offset calibration loop process. The blue curve represents the 1 kHz AOCL clock, the golden line depicts the end-of-conversion (EOC) output from the AOCL, and the red and yellow curves show the differential output of the CFIA. The differential input signals harbor a 250-mV offset. Once the AOCL operation begins, the initial offset is quickly corrected. In the absence of the acceleration capacitor Cv, the offset calibration time amounts to 11 ms. However, when Cv is implemented, it can be seen that the offset calibration time for the AOCL operation drops to 5 ms, as illustrated in Figure 18.

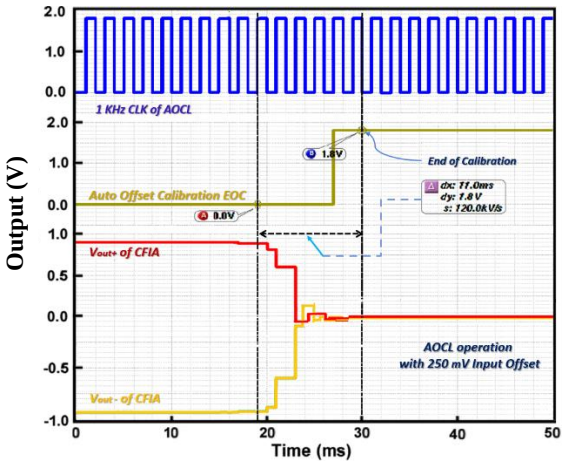


Figure 17. Measurement result of AOCL process without Cv

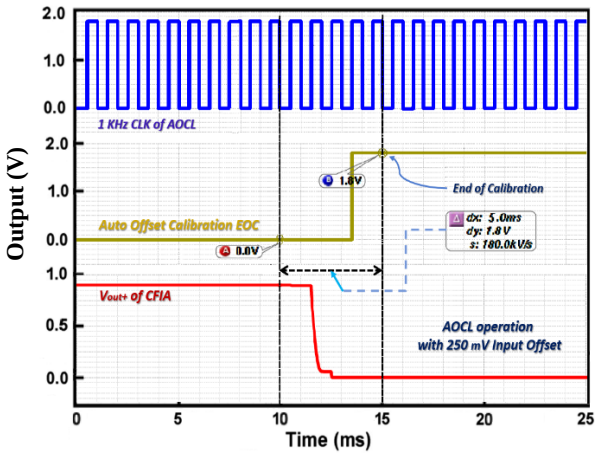


Figure 18. Measurement result of AOCL process with Cv

To ascertain the circuit's resilience in relation to offset fluctuations, we conducted a Monte-Carlo simulation with 200 samples. Figure 19, showcasing the simulation of the variation in input referred offset, reveals the average value of the input referred offset to be approximately 0.9 µV. The DAC outputs' DC operating point amid digital input variation is presented in Figure 20.

Using (1), it is calculated that the multipath CFIA's NEF is 5.18, leading to the energy efficiency factor (PEF), as given in (15) [32].

$$PEF = NEF^2.V_{DD} \quad (15)$$

The performance comparisons between the proposed CFIA and many state-of-the-art IAs are summarized in Table 1. It may be deduced from [14], [18], [33], [34] that the recommended CFIA exhibits a good input-referred offset. It is possible to conclude that the suggested CFIA has better CMRR to reject the power-line interference at the output of CFIA. Although it may be noted that our circuit can operate over a better bandwidth with an important adjustment of the capacitor value while keeping a low power dissipation.

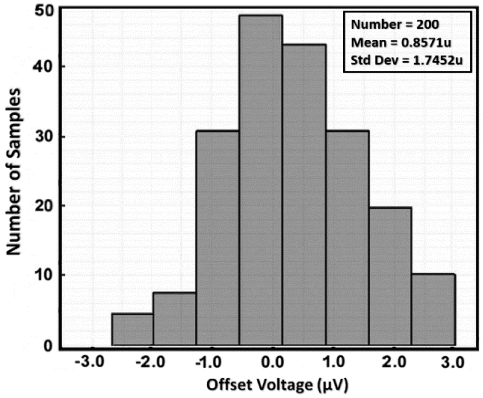


Figure 19. Monte-Carlo simulation results of the input referred offset voltage

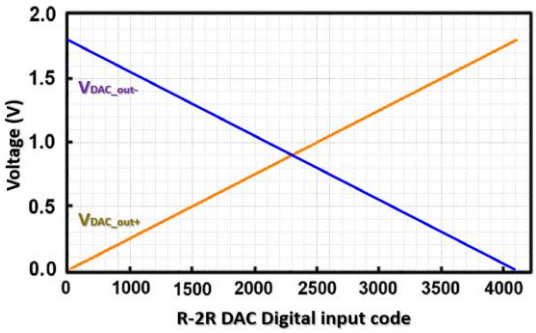


Figure 20. Simulation results CFIA output DC operating point

Table 1. Measured performances summary and comparison

Parameters	This Work	[14] JSSC 2012	[18] ACCESS 2022	[33] ICICM 2019	[34] AICSP 2018	[35] JSSC 2021
Technology (µm)	0.18	0.7	0.18	0.18	0.18	0.18
Architecture	CFIA (Multipath + CH + RRL)	CFIA (Multipath + CH + RRL)	CFIA (Multipath + CH + RRL)	CFIA (CH + RRL)	IA (CH + RRL)	CFIA (Multipath + AZ + CH)
AOCL	Yes	No	Yes	No	No	No
Chopping fr (KHz)	75	30	125	20	94	80
VDD (V)	1.8	5	3.3	3.3	1.6	5
Current (µA)	162	143	123	200	75	550
Power (µW)	291	715	413	660	120	2750
Gain (dB)	50.77	40	44.14	NA	20	NA
GBW (Hz)	0.5 M	900 K	1.92 M	NA	600 K	4.2 M
CMRR (dB)	114	137	100.7	130	NA	NA
PSRR (dB)	103	120	93.2	NA	NA	124
NEF	5.18	9.6	6.1	6.1	4.35	15.4
PEF	48.3	460.8	122.8	122.8	30.28	1185.8
IRN (ηV/√Hz)	16 0.1∼200 Hz	21 1K∼100kHz	15 1∼200 Hz	23 0.01 ∼500 Hz	20 0∼25 kHz	16 100∼50KHz
Input Referred Offset (µV)	0.9	2	1.01	5	4	0.8

4. CONCLUSION

This study presents the development of an analog front-end (AFE) suitable for resistive bridge microsensors, created utilizing a 0.18 µm CMOS process. The system functions on a chopper-stabilized multi-path framework, consuming a total current of 162 µA at a supply voltage of 1.8 V. The readout circuit comprises components such as a multi-path CFIA, AOCL, 2nd-order LPF, a 12-bit SAR ADC, a buffer, and an SPI block. The multi-path structure effectively eliminates the notches caused by the RRL, while the ripple resulting from chopper up-modulation is mitigated through the use of an RRL scheme in the LFP. The proposed circuit, by counteracting the offsets in the bridge, can facilitate low-noise performance. The AOCL component

serves to neutralize the undesired offset instigated by the resistive bridge sensor through the application of a binary search algorithm. The multi-path CFIA is capable of amplifying faint signals, boasting a gain of 50.77 dB, a CMRR of 114 dB, and a PSRR of 103 dB. The system accomplishes an input-referred offset of 0.9 μV and an input-referred noise at 200 Hz measuring 16 ηV/√Hz, thereby decreasing the noise efficiency factor (NEF) to 5.18. The total power consumption registers at 291 μW, demonstrating low-power traits. Given its effective input-referred offset and minimal power consumption, the developed AFE proves to be an ideal candidate for a multitude of resistive-bridge sensor applications.

REFERENCES

[1] H. Sun, D. Fang, K. Jia, F. Maarouf, H. Qu, and H. Xie, "A low-power low-noise dual-chopper amplifier for capacitive CMOS-MEMS accelerometers," *IEEE Sensors Journal*, vol. 11, no. 4, pp. 925–933, 2011, doi: 10.1109/JSEN.2010.2064296.

[2] S. Vetrivel, R. Mathew, and A. R. Sankar, "Design and optimization of a doubly clamped piezoresistive acceleration sensor with an integrated silicon nanowire piezoresistor," *Microsystem Technologies*, vol. 23, no. 8, pp. 3525–3536, 2017, doi: 10.1007/s00542-016-3219-2.

[3] Y. Zhang, Z. Zhang, B. Pang, L. Yuan, and T. Ren, "Tiny MEMS-based pressure sensors in the measurement of Intracranial Pressure," *Tsinghua Science and Technology*, vol. 19, no. 2, pp. 161–167, 2014, doi: 10.1109/TST.2014.6787369.

[4] X. Zhang *et al*., "Printed carbon nanotubes-based flexible resistive humidity sensor," *IEEE Sensors Journal*, vol. 20, no. 21, pp. 12592–12601, 2020, doi: 10.1109/JSEN.2020.3002951.

[5] H. Y. Yu, M. Qin, J. Q. Huang, and Q. A. Huang, "A MEMS capacitive pressure sensor compatible with CMOS process," *Proceedings of IEEE Sensors*, 2012, doi: 10.1109/ICSENS.2012.6411206.

[6] A. Menssouri, K. El Khadiri, and A. Tahiri, "In-Pixel CTIA & Readout Circuitry for an Active CMOS Image Sensor," *WSEAS Transactions on Systems and Control*, vol. 16, pp. 626–632, 2021, doi: 10.37394/23203.2021.16.58.

[7] G. T. Ong and P. K. Chan, "A power-aware chopper-stabilized instrumentation amplifier for resistive wheatstone bridge sensors," *IEEE Transactions on Instrumentation and Measurement*, vol. 63, no. 9, pp. 2253–2263, 2014, doi: 10.1109/TIM.2014.2308992.

[8] J. H. Lee, S. K. Yeh, and W. Fang, "Vertically Integrated Double-Bridge Design for CMOS-MEMS Tri-Axial Piezo-Resistive Force Sensor," *Proceedings of the IEEE International Conference on Micro Electro Mechanical Systems (MEMS)*, vol. 2020-Janua, pp. 693–696, 2020, doi: 10.1109/MEMS46641.2020.9056191.

[9] Y. Laababid, K. El Khadiri, H. Qjidaa, A. Lakhssassi, and A. Tahiri, "The Design of an EEG Bio-Amplifier for the Primary Motor Cortex Zone in 180 nm CMOS Technology," *Lecture Notes in Networks and Systems*, vol. 211 LNNS, pp. 1607–1617, 2021, doi: 10.1007/978-3-030-73882-2_146.

[10] J. G. Webster, *Medical instrumentation application and design*. New York: John Wiley and Sons, 1998.

[11] F. Neves, J. P. Oliveira, and H. Oliveira, "A sub-1V CMOS Instrumentation Amplifier for an AFE Interfacing with Sensors," in *2021 International Young Engineers Forum (YEF-ECE)*, Jul. 2021, pp. 1–6, doi: 10.1109/YEF-ECE52297.2021.9505076.

[12] M. S. J. Steyaert, W. M. C. Sansen, and C. Zhongyuan, "A Micropower Low-Noise Monolithic Instrumentation Amplifier For Medical Purposes," *IEEE Journal of Solid-State Circuits*, vol. 22, no. 6, pp. 1163–1168, 1987, doi: 10.1109/JSSC.1987.1052869.

[13] K. Abdelhalim, H. M. Jafari, L. Kokarovtseva, J. L. P. Velazquez, and R. Genov, "64-Channel uwb wireless neural vector analyzer soc with a closed-loop phase synchrony-triggered neurostimulator," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 10, pp. 2494–2510, 2013, doi: 10.1109/JSSC.2013.2272952.

[14] Q. Fan, J. H. Huijsing, and K. A. A. Makinwa, "A 21 nV/√ Hz chopper-stabilized multi-path current-feedback instrumentation amplifier with 2 μ v offset," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 464–475, 2012, doi: 10.1109/JSSC.2011.2175269.

[15] C. J. Lee and J. I. Song, "A Chopper Stabilized Current-Feedback Instrumentation Amplifier for EEG Acquisition Applications," *IEEE Access*, vol. 7, pp. 11565–11569, 2019, doi: 10.1109/ACCESS.2019.2892502.

[16] J. F. Witte, J. H. Huijsing, and K. A. A. Makinwa, "A chopper and auto-zero offset-stabilized CMOS instrumentation amplifier," *IEEE Symposium on VLSI Circuits, Digest of Technical Papers*, pp. 210–211, 2009.

[17] C. C. Enz and G. C. Temes, "Circuit techniques for reducing the effects of Op-Amp imperfections: Autozeroing, correlated double sampling, and chopper stabilization," *Proceedings of the IEEE*, vol. 84, no. 11, pp. 1584–1614, 1996, doi: 10.1109/5.542410.

[18] M. Yoo, Y. Kwon, H. Kim, G. Choi, K. Nam, and H. Ko, "Low-Noise Resistive Bridge Sensor Analog Front-End Using Chopper-Stabilized Multipath Current Feedback Instrumentation Amplifier and Automatic Offset Cancellation Loop," *IEEE Access*, vol. 10, pp. 12385–12394, 2022, doi: 10.1109/ACCESS.2022.3144688.

[19] M. A. P. Pertijs and W. J. Kindt, "A 140 dB-CMRR current-feedback instrumentation amplifier employing ping-pong auto-zeroing and chopping," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 10, pp. 2044–2056, 2010, doi: 10.1109/JSSC.2010.2060253.

[20] K. A. A. M. Q. Fan, J. H. Huijsing, "Analysis of input impedance, input bias and offset current of a chopped multi-path current feedback instrumentation amplifier," 2011.

[21] G. Choi *et al*., "Current-Reused Current Feedback Instrumentation Amplifier for Low Power Leadless Pacemakers," *IEEE Access*, vol. 9, pp. 113748–113758, 2021, doi: 10.1109/ACCESS.2021.3103987.

[22] J. H. Huijsing, "Operational Amplifiers: Theory and Design," 2001.

[23] D. M. Monticelli, "A quad CMOS single-supply op amp with rail-to-rail output swing," *IEEE Journal of Solid-State Circuits*, vol. 21, no. 6, pp. 1026–1034, Dec. 1986, doi: 10.1109/JSSC.1986.1052645.

[24] Y. Laababid, K. El Khadiri, and A. Tahiri, "Design of a Low-Power Low-Noise ECG Amplifier for Smart Wearable Devices Using 180nm CMOS Technology," *WSEAS Transactions on Power Systems*, vol. 17, pp. 177–186, 2022, doi: 10.37394/232016.2022.17.18.

[25] H. Kim, H. Song, Y. Park, and H. Ko, "Low noise resistive analog front-end with automatic offset calibration loop," *ISOCC 2015 - International SoC Design Conference: SoC for Internet of Everything (IoE)*, pp. 231–232, 2016, doi: 10.1109/ISOCC.2015.7401732.

[26] Y. Kwon *et al*., "Fully differential chopper-stabilized multipath current-feedback instrumentation amplifier with R-2R DAC offset adjustment for resistive bridge sensors," *Applied Sciences (Switzerland)*, vol. 10, no. 1, 2020, doi: 10.3390/app10010063.

[27] X. Zhong, A. Bermak, and C. Y. Tsui, "A low-offset dynamic comparator with area-efficient and low-power offset cancellation," *IEEE/IFIP International Conference on VLSI and System-on-Chip, VLSI-SoC*, 2017, doi: 10.1109/VLSI-SoC.2017.8203481.

[28] B. Razavi, "The StrongARM latch," *IEEE Solid-State Circuits Magazine*, vol. 7, no. 2, pp. 12–17, 2015.

[29] M. D. Scott, B. E. Boser, and K. S. J. Pister, "An ultralow-energy ADC for smart dust," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 7, pp. 1123–1129, 2003, doi: 10.1109/JSSC.2003.813296.
[30] J. A. Schoeff, "An inherently monotonic 12 bit DAC," *IEEE Journal of Solid-State Circuits*, vol. 14, no. 6, pp. 904–911, Dec. 1979, doi: 10.1109/JSSC.1979.1051296.
[31] R. G. H. Eschauzier, R. Hogervorst, and J. H. Huijsing, "A programmable 1.5 v cmos class-ab operational amplifier with hybrid nested miller compensation for 120 db gain and 6 mhz ugf," *IEEE Journal of Solid-State Circuits*, vol. 29, no. 12, pp. 1497–1504, 1994, doi: 10.1109/4.340423.
[32] S. Song *et al.*, "A low-voltage chopper-stabilized amplifier for fetal ECG monitoring with a 1.41 power efficiency factor," *IEEE Transactions on Biomedical Circuits and Systems*, vol. 9, no. 2, pp. 237–247, 2015, doi: 10.1109/TBCAS.2015.2417124.
[33] P. Xie, Q. Duan, Z. Meng, S. Huang, Y. Ding, and L. Han, "A Low-Noise, Low-Power, and Chopper-Stabilized, Current-Feedback Instrumentation Amplifier for Current Sensing Application," *2019 4th International Conference on Integrated Circuits and Microsystems, ICICM 2019*, pp. 162–165, 2019, doi: 10.1109/ICICM48536.2019.8977160.
[34] R. Wei, Z. Liu, and R. Zhu, "Low noise chopper-stabilized instrumentation amplifier with a ripple reduction loop," *Analog Integrated Circuits and Signal Processing*, vol. 96, no. 3, pp. 521–529, 2018, doi: 10.1007/s10470-018-1214-5.
[35] T. Rooijers, S. Karmakar, Y. Kusuda, J. H. Huijsing, and K. A. A. Makinwa, "A Fill-In Technique for Robust IMD Suppression in Chopper Amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 12, pp. 3583–3592, 2021, doi: 10.1109/JSSC.2021.3107350.

BIOGRAPHIES OF AUTHORS

Younes Laababid received his Master degree in Microelectronics from Faculty of Sciences Dhar El Mahraz, Fez, Morocco, in 2019. He is now a PhD candidate in Laboratory of Computer Science and Interdisciplinary Physics (LIPI), Superior Normal School, ENS-FEZ, Morocco. His research interests include renewable energy, CMOS mixed-mode integrated circuit design, development of integrated circuits for the acquisition, shaping and processing of biopotential signals. He can be contacted at email: younes.laababid@usmba.ac.ma.

Karim El Khadiri received M.S. and Ph.D. degrees in Faculty of Sciences from Sidi Mohammed Ben Abdellah University in 2011 and 2017, respectively. Since 2012, he served as a Research Scientist at Faculty of science in the University of Sidi Mohammed Ben Abdellah, Fez, Morocco and guest researcher at LIMA laboratory in UQO Canada. His current interests include switch mode audio amplifier, CMOS mixed-mode integrated circuit design, design techniques for RFID, RF front-ends for passive tags, Li-Ion battery charger and power management. He can be contacted at email: karim.elkhadiri@usmba.ac.ma.

Ahmed Tahiri received the graduate degree DES in Department of Physics, Sidi Mohammed Ben Abdellah University, Morocco in 1997, received the Ph.D. degree in physics from the University Sidi Mohamed Ben Abdellah, Faculty of Science, Morocco in 2005. He completed his doctoral studies in didactics of science in the University of Sherbrooke in Canada in 2010. He is now a professor in Superior Normal School, ENS-FEZ, Morocco. His research interests include image processing, computer science and didactics of scientific disciplines. He can be contacted at email: ahmed.tahiri@usmba.ac.ma.