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Computer simulation of open-circuit fault-tolerant boost rectifier based on SPMC

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ABSTRACT

This paper presents a computer simulation of an open-circuit fault-tolerant boost rectifier based on a single-phase matrix converter using MATLAB/ Simulink. The proposed converter employs a fault identification technique to identify the faulty switch by generating a binary code extracted from the output voltage, magnitude of inductor current, and cycle of the input power supply. Upon identifying the faulty switch, the current is redirected to any available path through operational switches by controlling the switching devices. The aim is to ensure uninterrupted power supply from the source to the load. The paper includes a detailed analysis of the fault identification technique and the options for rerouting the current path. The outcomes of this paper are simulated using MATLAB/Simulink.

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1. INTRODUCTION

Due to the increasing number of electric and hybrid vehicles being released on the market, power converters have become one of the most sought-after equipment. This is because these vehicles require additional characteristics in this technological era. One important characteristic of power converters is their reliability, defined as the ability to continuously supply power to the load even in the event of a fault in major components. Despite the recognition of power semiconductor failure as a key factor in converter destruction, it remains one of the most common causes of converter failure after electrolytic capacitor failure. As such, past research has focused on developing fault-tolerant systems to address this issue involving fault identification technique [1]–[5].

Fault identification in electrical circuits involves identifying and locating faults or failures in an electrical system to prevent equipment damage, ensure personnel safety, and maintain system reliability. To achieve this, a reasonable fault identification technique is necessary, which includes exact estimation, basic configuration, and fast recognition, with the aim of changing the converter configuration and avoiding any subsequent harm in a fault-converter [6]–[9]. There are two types of scenarios where faults can occur namely open-circuit faults (OCFs) and short-circuit faults (SCFs) [10]–[12]. SCFs can occur due to cable leakage, switching device failure, and auxiliary power supply breakdown, which can cause a power system breakdown. Equipment-based protection such as circuit breakers and fuses can be used to prevent equipment damage. However, OCFs as may not damage the system as SCFs, but it can interrupt the process. OCFs can occur due to the lift of the bonding wire, driver failure, or short-circuit fault-induced rupture [10]. Various fault identification in matrix converter have been proposed over the years by researchers using various techniques

such as monitoring the load current and judging the switching state to locate the faulty switch [13]. In [14], the identification of OCF is done by checking the waveform of the rectifier stage output voltage and comparing the measured output current with output current reference in converter stage. Detection of OCF is done by monitoring the voltage error signal in every bidirectional switches [15]. The fault identification methods most commonly applied to modular multilevel converters and single phase matrix converter (SPMC), which have a high number of switches, include capacitor voltage estimation where voltage signals of capacitors are combined and sampled to determine the fault occurrence [16], and comparison between estimated current and expected current with gate signal of arm current [17]. SPMC was first discovered by Zuckerberger [18]. SPMC allows current to flow in both directions while blocking forward and reverse voltage [19]. It is made from four bi-directional power semiconductor such as insulated-gate bipolar transistor (IGBT) and metal-oxide-semiconductor field-effect transistor (MOSFETS). The switches are utilized due to their capability to handle high frequency switching control [19]. SPMC can be used as boost converter to step up the level of input voltage thus producing higher output voltage.

The importance of fault-tolerant feature in power converters often requires additional repairs and can lead to destruction of a converters [20]–[23]. Various fault-tolerant methods have been proposed over the years, each with its own pros and cons. One approach as discussed in [24], involves introducing a pair of back-to-back thyristors between the motor neutral and the supply neutral within the converter in three-phase. Another method, as demonstrated in [15], utilizes a switching configuration of a matrix converter to mitigate the effects of OCF in the circuit, although it does not address open circuit faults in the lower horizontal pair. Additionally, [25] presents an implementation featuring bidirectional switches for a three-phase matrix converter, which also encompasses the neutral point.

Although considerable research efforts have been devoted to the implementation of fault-tolerant in matrix converter recently, however, a little effort has been made to develop fault-tolerant for SPMC based converter. To enhance the reliability of the SPMC based converter, a fault identification technique to identify OCF across a semiconductor switch is proposed in this paper. The fault identification technique is implemented by checking the voltage drop of the output voltage, magnitude of the inductor current and assessment of input supply cycle. Once the OCF across the semiconductor switch is identified, the circuit will direct the current away from the OCF switch by using various switching control. Furthermore, an analysis will be conducted to assess the feasibility of rerouting the existing path option, taking into account the identified open-circuited semiconductor switch in order to maintain uninterrupted power supply to the load. Subsequently, the efficacy of the suggested identification technique will be validated through the utilization of MATLAB/Simulink.

2. BOOST RECTIFIER BASED ON SPMC

A power electronic system comprises one or more power electronic converters, which can shape input power into output power using the switching characteristics of power semiconductor devices. Static power converters are highly efficient in performing various power conversions, with separate ac and dc conversion systems used for AC and DC loads. The boost rectifier based on SPMC is capable of performing all these conversions, thereby reducing the need for learning multiple converter topologies. The boost rectifier based on SPMC circuit is shown in Figure 1 requires four bidirectional switches that can block voltage and conduct current in both directions as in [26]. In the absence of bidirectional switch modules, an IGBT with diode pair is used due to its high switching ability and current-carrying capacities [15]. The boost rectifier based on SPMC's bidirectional switch allows the current to flow in two directions, ensuring that the other switch takes over in case of a fault. Additionally, the boost rectifier based on SPMC can develop any type of input AC or DC and produce any output AC or DC, making it highly advantageous.

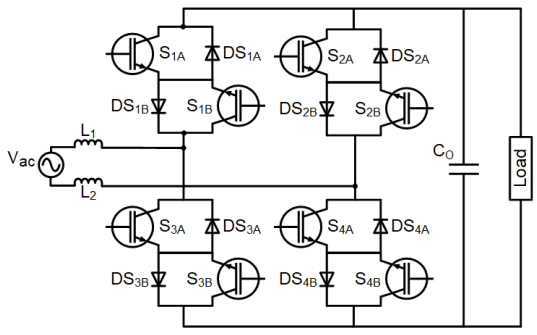


Figure 1. Boost rectifier based on SPMC circuit

Figure 2 illustrates the basic operational sequence of the proposed boost rectifier based on SPMC. During the positive cycle, the current path involves S_{1B} and DS_{1A}, S_{2A} and DS_{2B}, charging inductors L_1 and L_2, as depicted in Figure 2(a) (positive charging mode). Subsequently, the current flows through S_{1B} and DS_{1A}, S_{4B} and DS_{4A}, and passes through the load in Figure 2(b) (positive discharging mode). In the negative half cycle, the current flow through S_{2B}, DS_{2A}, S_{1A} and DS_{1B}. This flow charges inductors L_1 and L_2, as seen in Figure 2(c) (negative charging mode), which mirrors the behavior of the positive charging mode. Finally, the current pathway comprises S_{2B} and DS_{2A}, S_{3B} and DS_{3A}, culminating in a path through the load in Figure 2(d) (negative discharging mode).

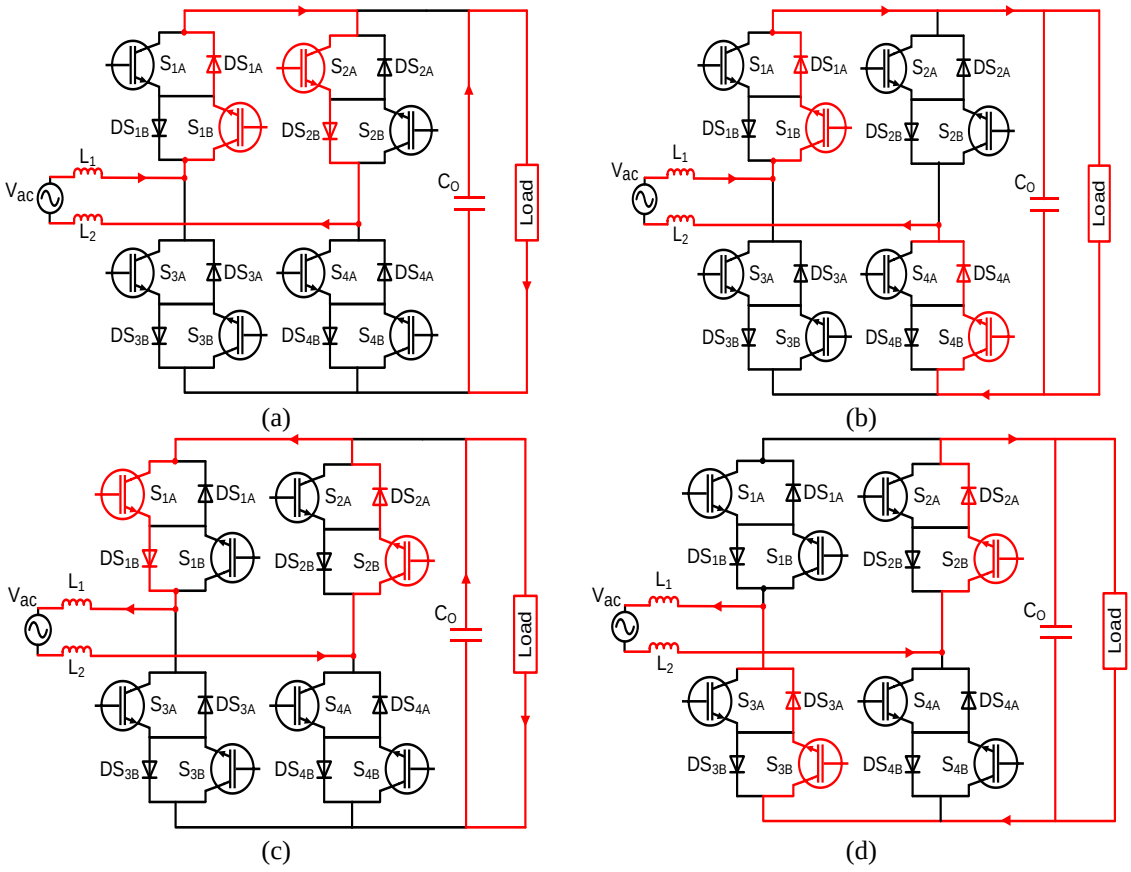


Figure 2. Operation of boost rectifier based on SPMC of (a) positive charging mode, (b) positive discharging mode, (c) negative charging mode, and (d) negative discharging mode

3. OPEN-CIRCUIT FAULT IDENTIFICATION TECHNIQUE

The primary objective of the fault identification technique is to locate the exact faulty switch's location in the event of a fault occurrence. This is achieved by generating a binary code, which serves as a signal sent to a controller. The controller then activates the appropriate current option route (COR) communication, thereby establishing the necessary current pathway within the circuit.

The identification of faulty switches involves an analysis of the output voltage (50 V), assessment of the input supply cycle, and evaluation of the inductor current magnitude. The process begins by observing the output voltage which set at 50 V. When fault occurs, the output voltage level will drop to less than 30 V within half cycle (10 ms). Subsequently, the input power supply's cycle is determined either positive or negative cycle. Then the inductor current magnitude is assessed to determine faulty semiconductor switch. The identification process flowchart is shown in Figures 3(a)-3(d) according to COR. It's important to note that, within each COR, only one or a pair of faulty semiconductor switches is permissible. In this paper, switches “A” (S1A, S2A, S3A, and S4A) operates as operational controlled switches that will determine the current flow of the proposed converter. Switches "B" (S1B, S2B, S3B, and S4B) operate continuously as always-on switches. These “B” switches must remain in the on-state position in to ensure the operational of the SPMC.

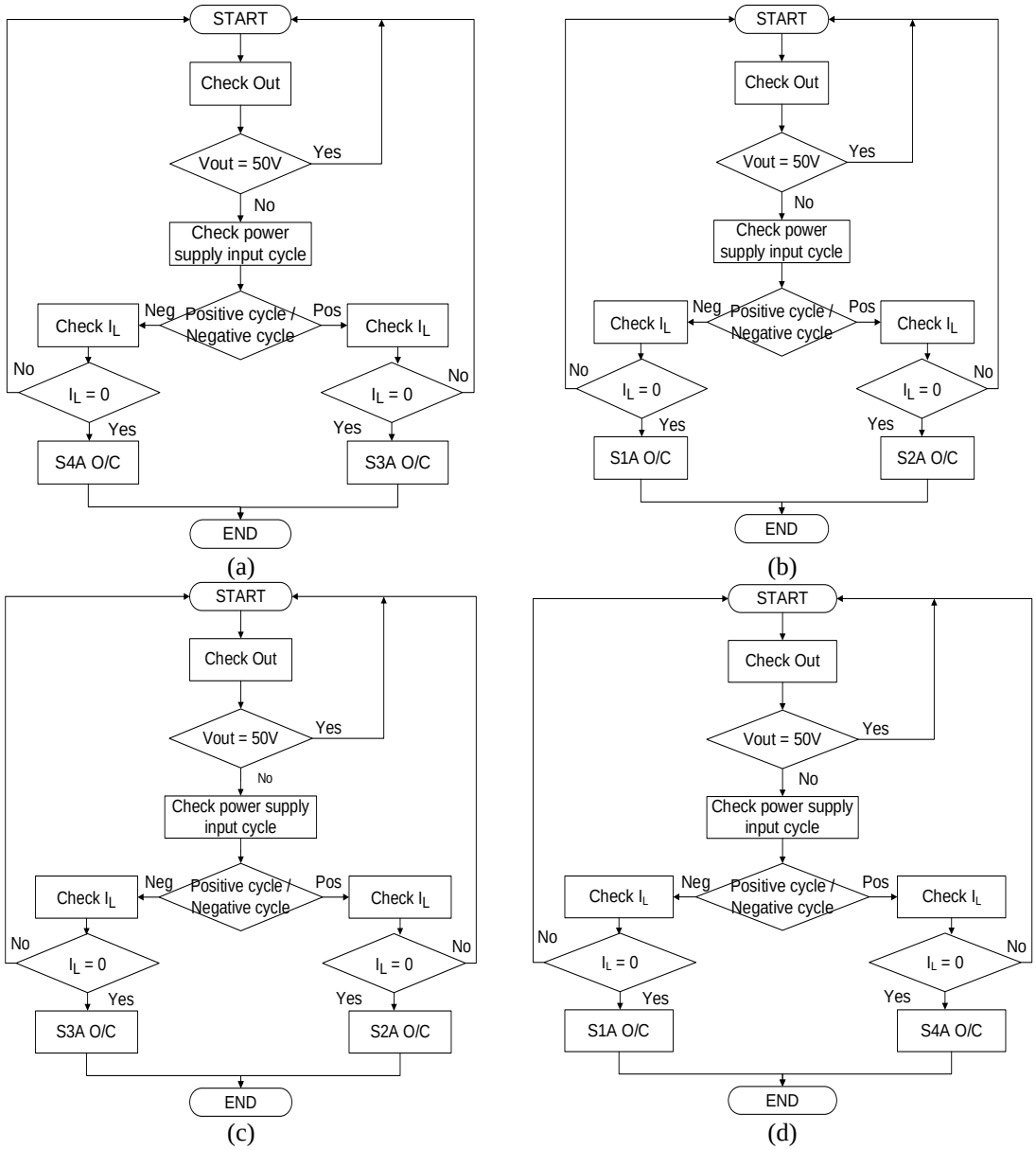


Figure 3. Flowchart for (a) COR 1, (b) COR 2, (c) COR 3, and (d) COR 4

4. PROPOSED FAULT-TOLERANT BOOST RECTIFIER BASED ON SPMC

The proposed switching strategy exhibits the capability of the fault-tolerant boost rectifier based on SPMC to transmit power to the load even in the event of two open-circuited switches. Table 1 provides the potential fault scenarios denoted as Tn and the corresponding fault-tolerant boost rectifier status. Here, n signifies the possibility condition ranging from 1 to 16. Fault occurrences can be categorized into four distinct conditions. First condition, occurs when an open circuit fault (OCF) arises at one of the "A" switches (T8, T12, T14, and T15). In this situation, the fault-tolerant boost rectifier presents two viable operational options. Second fault condition, arises when either horizontal pairs (S1A and S2A or S3A and S4A) or vertical pairs (S1A and S3A or S2A and S4A) are open-circuited (T4, T6, T11, and T13). In this case, the fault-tolerant boost rectifier has a singular operative configuration. Third fault condition, emerges when an OCF occurs at the diagonal pairs (S1A and S4A or S2A and S3A). In this scenario, the fault-tolerant boost rectifier ceases to function as there is no available current pathway. Fourth fault condition, arises when only one switch remains operational. This condition is prohibited, as a minimum of two functioning switches is essential to enable the flow of current. However, if the OCF occurs at one of the switches, the proposed converter still may have functioning as an uncontrolled rectifier provided that there is a diode across the switch as proposed in [15].

COR presents a conceptual switching arrangement designed to reroute a current flow to operational switches in the event of fault occurrence. The COR can be classified into four switching strategies namely COR 1 until COR 4. This paper presents only focus on COR, as the other conditions pertain to full-wave uncontrolled rectifiers, whereas COR is associated with full-wave controlled rectifiers.

Table 1. Faulty possibility table

Fault possibility	S_{1A}	S_{2A}	S_{3A}	S_{4A}	Converter operation
T_1	0	0	0	0	Full wave uncontrolled rectifier
T_2	0	0	0	1	Full wave uncontrolled rectifier
T_3	0	0	1	0	Full wave uncontrolled rectifier
T_4	0	0	1	1	COR 1
T_5	0	1	0	0	Full wave uncontrolled rectifier
T_6	0	1	0	1	COR 3
T_7	0	1	1	0	Full wave uncontrolled rectifier
T_8	0	1	1	1	COR 1 and COR 3
T_9	1	0	0	0	Full wave uncontrolled rectifier
T_{10}	1	0	0	1	Full wave uncontrolled rectifier
T_{11}	1	0	1	0	COR 4
T_{12}	1	0	1	1	COR 1 and COR 4
T_{13}	1	1	0	0	COR 2
T_{14}	1	1	0	1	COR 2 and COR 3
T_{15}	1	1	1	0	COR 2 and COR 4
T_{16}	1	1	1	1	All paths

4.1. Current option route 1 (COR 1)

Figure 4 illustrates the operational sequence of the proposed fault-tolerant boost rectifier in the event of an open circuit fault (OCF) occurring at switches S_{1A} and S_{2A}. During the positive cycle, the current path involves S_{3A} and DS_{3B}, S_{4B} and DS_{4A}, charging inductors L_1 and L_2, as depicted in Figure 4(a) (positive charging mode). Subsequently, the current flows through S_{1B} and DS_{1A}, S_{4B} and DS_{4A}, and passes through the load in Figure 4(b) (positive discharging mode).

In the negative half cycle, S_{4A} is activated, directing the current through DS_{4B}, S_{3B}, and DS_{3A}. This flow charges inductors L_1 and L_2, as seen in Figure 4(c) (negative charging mode), which mirrors the behavior of the positive charging mode. Finally, the current pathway comprises S_{2B} and DS_{2A}, S_{3B} and DS_{3A}, culminating in a path through the load in Figure 4(d) (negative discharging mode). The switching signal during COR 1 is shown in Figure 4(e).

4.2. Current option route 2 (COR 2)

Figure 5, the operational dynamics of the proposed fault-tolerant boost rectifier are presented in the case of an open circuit fault (OCF) occurring at switches S3A and S4A. During the positive cycle, the current follows a path involving S_{1B} and DS_{1A}, S_{2A} and DS_{2B}, charging inductors L_1 and L_2, as depicted in Figure 5(a) (positive charging mode). Subsequently, the current traverses S_{1B} and DS_{1A}, S_{4B} and DS_{4A}, and progresses through the load (positive discharging mode).

In the negative half cycle, S1A is activated, guiding the current through S_{2B}, DS_{2A}, and DS_{1A}, thereby charging inductors L_1 and L_2, as shown in Figure 5(b) (negative charging mode). This mode mirrors the behavior described in the positive charging mode. Finally, the current path encompasses S_{2B} and DS_{2A}, S_{3B} and DS_{3A}, concluding with the flow through the load (negative discharging mode). The switching signal during COR 2 is shown in Figure 5(c).

4.3. Current option route 3 (COR 3)

Figure 6 illustrates the operational behavior of the proposed fault-tolerant boost rectifier in the event of an open circuit fault (OCF) emerging at switches S_{3A} and S_{4A}. Throughout the positive cycle, the current follows a pathway via S_{1B} and DS_{1A}, S_{2A} and DS_{2B}, charging inductors L_1 and L_2, as depicted in Figure 6(a) (positive charging mode). Subsequently, the current's trajectory encompasses S_{1B} and DS_{1A}, S_{4B} and DS_{4A}, progressing through the load (positive discharging mode).

Within the negative half cycle, the activation of S_{4A} directs the current through DS_{4B}, S_{3B}, and DS_{3A}, facilitating the charging of inductors L_1 and L_2, as displayed in Figure 6(b) (negative charging mode). This mode closely parallels the description of the positive charging mode. Ultimately, the current's path includes S_{2B} and DS_{2A}, S_{3B} and DS_{3A}, culminating in the flow through the load (negative discharging mode). The switching signal during COR 3 is shown in Figure 6(c).

4.4. Current option route 4 (COR 4)

Figure 7 (see in appendix) shows the operational sequence of the proposed fault-tolerant boost rectifier under the circumstance of an open circuit fault (OCF) occurring at switches S_{3A} and S_{4A}. Throughout the positive cycle, the current's path encompasses S_{3A} and DS_{3B}, S_{4B} and DS_{4A}, facilitating the charging of inductors L_1 and L_2, as shown in Figure 7(a) (positive charging mode). Subsequently, the current flows through S_{1B} and DS_{1A}, S_{4B} and DS_{4A}, traversing the load (positive discharging mode).

In the negative half cycle, the activation of S_{1A} directs the current through S_{2B}, DS_{2A}, and DS_{3A}, thus promoting the charging of inductors L_1 and L_2, as depicted in Figure 7(b) (negative charging mode). This mode is analogous to the previously described positive charging mode. Finally, the current flows through S_{2B} and DS_{2A}, S_{3B} and DS_{3A}, culminating in its passage through the load (negative discharging mode). The switching signal during COR 4 is shown in Figure 7(c).

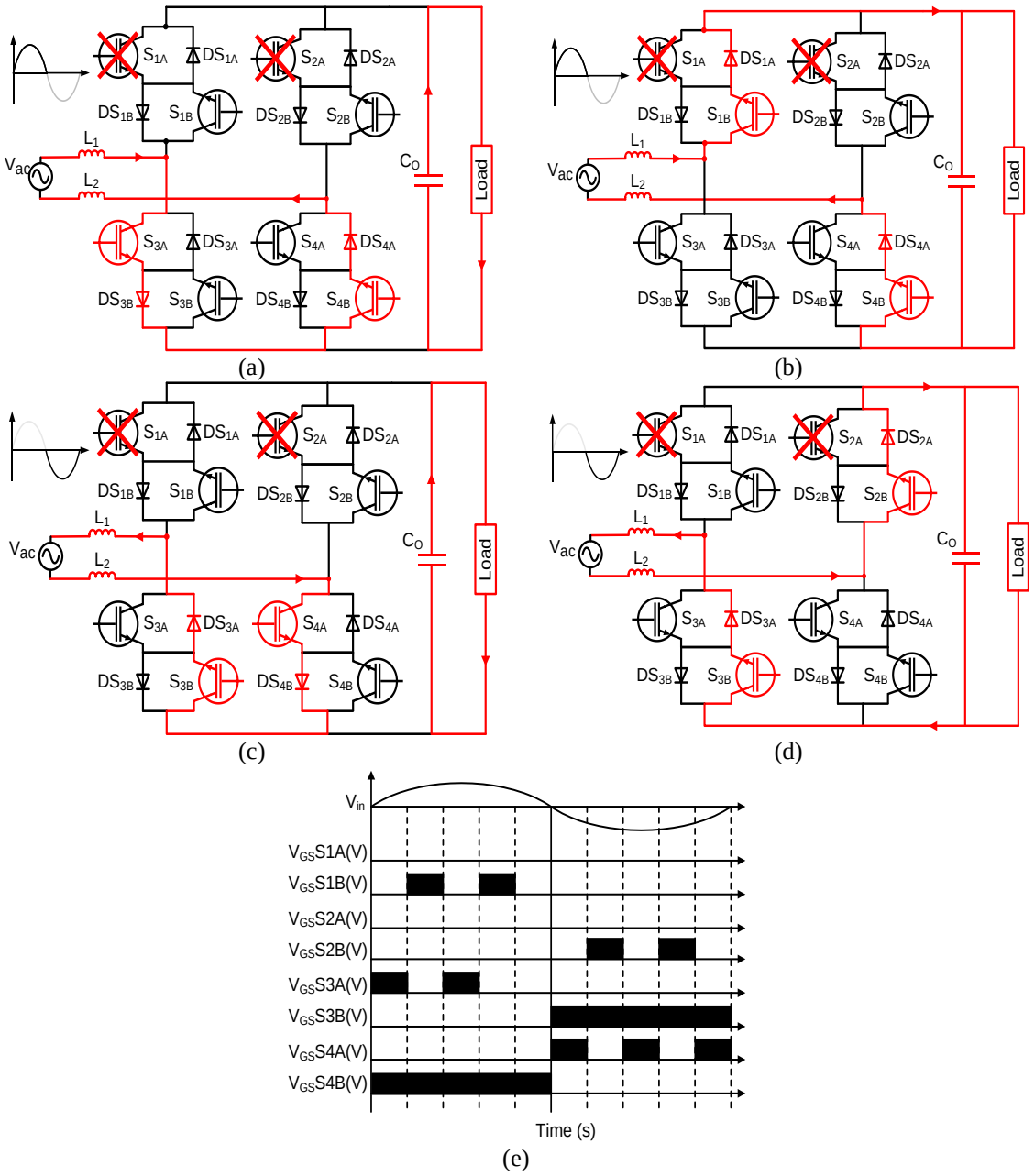


Figure 4. Operation boost rectifier based on SPMC for (a) positive charging mode, (b) positive discharging mode, (c) negative charging mode, (d) negative discharging mode, and (e) switching control during COR 1

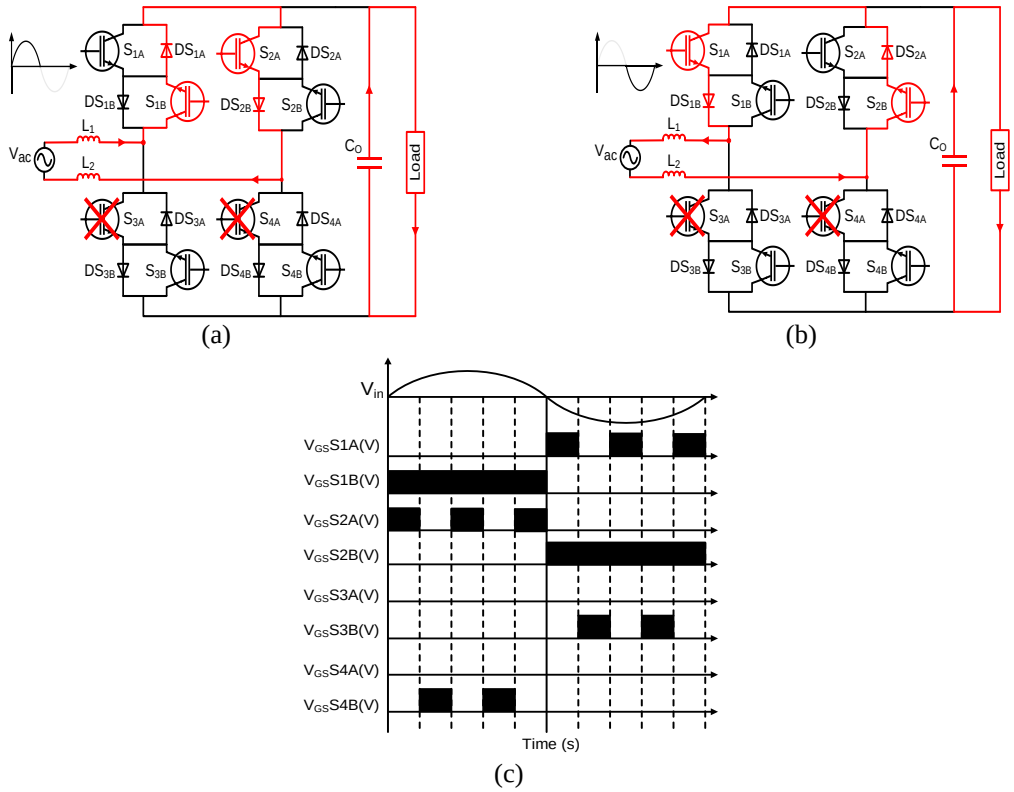


Figure 5. Operation of boost rectifier based on SPMC for (a) positive charging mode, (b) negative charging mode, and (c) switching control during COR 2

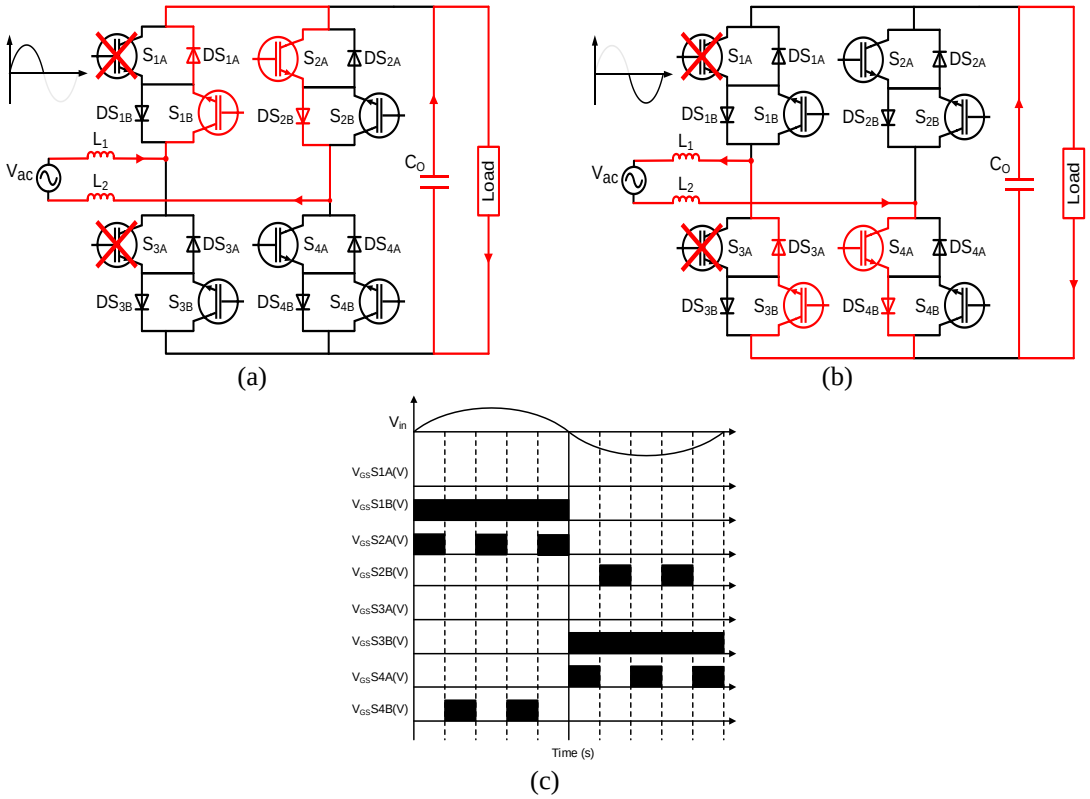


Figure 6. Operation of boost rectifier based on SPMC for (a) positive charging mode, (b) negative charging mode, and (c) switching control during COR 3

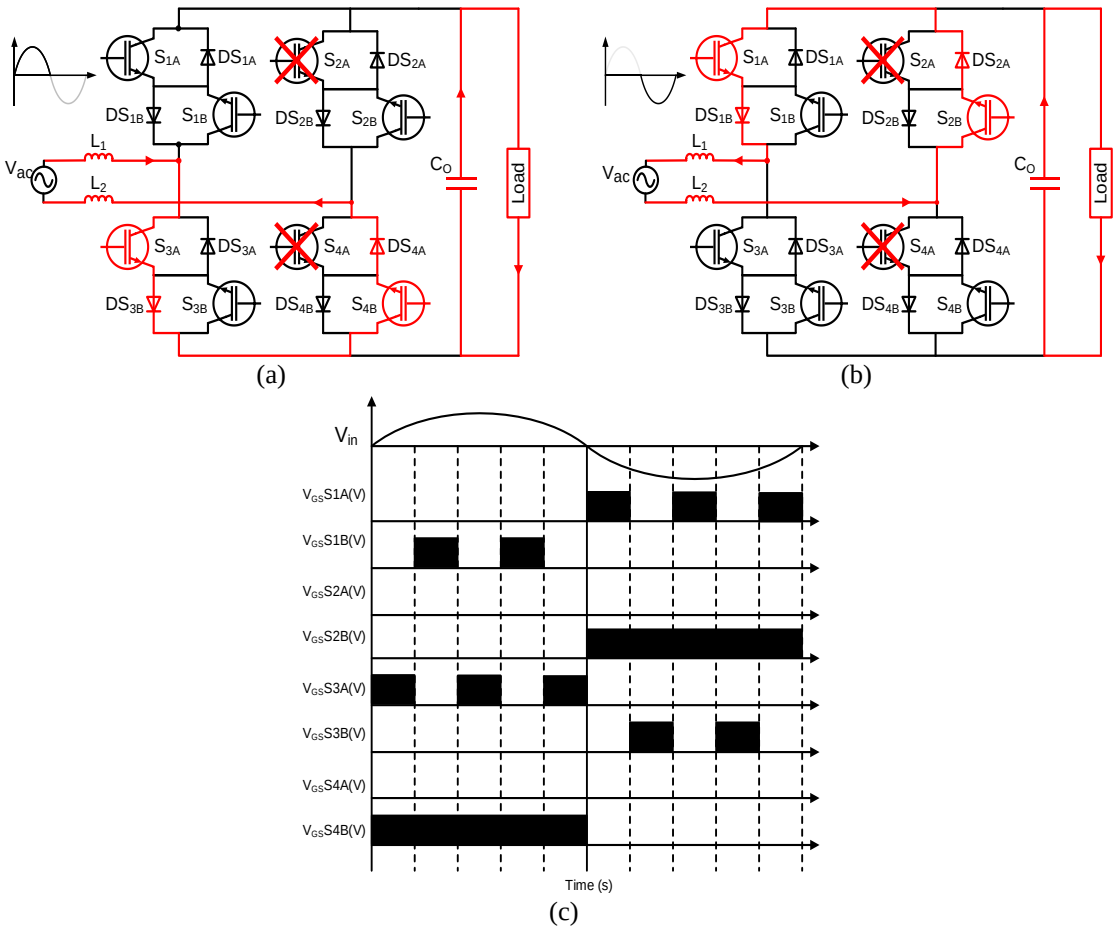


Figure 7. Operation of boost rectifier based on SPMC for (a) positive charging mode, (b) negative charging mode, and (c) switching control during COR 4

5. SIMULATION OF OPEN-CIRCUIT FAULT-TOLERANT BOOST RECTIFIER BASED ON SPMC USING MATLAB/SIMULINK

The proposed functionality fault-identification technique and fault-tolerant strategy performance are evaluated using the MATLAB/Simulink based on parameters given in Table 2. Figure 8 shows the flow of block diagram for the proposed boost rectifier based on SPMC. To control "A" switches, switching signals must be initiated from a signal builder. The signal builder is used to control the modulated signal from multiplier by turning on or off "A" switches based on COR conditions. The input for signal builder is a modulated signal generated from a multiplier which act as medium for PWM generator that modulate 10 kHz and 50 Hz. 10 kHz is a switching frequency generated from the pulse generator and 50 Hz is a signal generated from input supply. MATLAB function is used as a controller for the signal builder to control the "A" switches and to set the duty ratio at 85%. The duty ratio is set at 85% to ensure the output voltage is 50 V by turning "A" switches on or off when the output voltage less than 30 V. If the output voltage is between 50 V and 30 V, the signal builder will be in standby mode and vice versa. Figure 9 shows a simulation of open circuit fault-tolerant boost rectifier based on SPMC. The pulse generator is connected to "B" switch to set it at always-on state. Pulse generator 1 is connected to S_{1B} and S_{4B} while pulse generator 2 is connected to S_{2B} and S_{3B}. Signal from signal builder is generated for "A" switches are labelled S1, S2, S3, and S4.

Table 2. SPMC simulation parameters

Parameters	Values	Parameters	Values
Input Voltage, V_{in}	12 Vac	Boost Inductors, L_1 and L_2	4 mH
Output Voltage, V_{out}	50 Vdc	Capacitive Filter, C_o	47 µF
Input Frequency, f_{in}	50 Hz	Output Resistor, R_o	320 Ω
Switching Frequency, f_s	10 kHz		

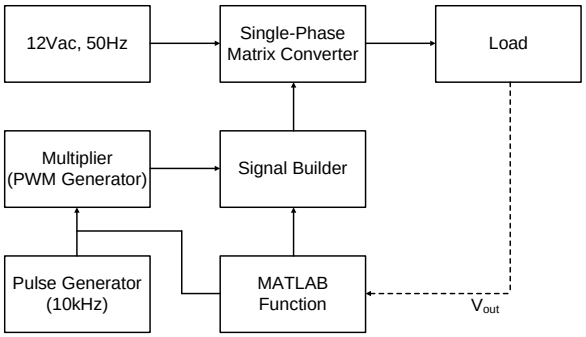


Figure 8. Block diagram flow of open circuit fault-tolerant boost rectifier based on SPMC

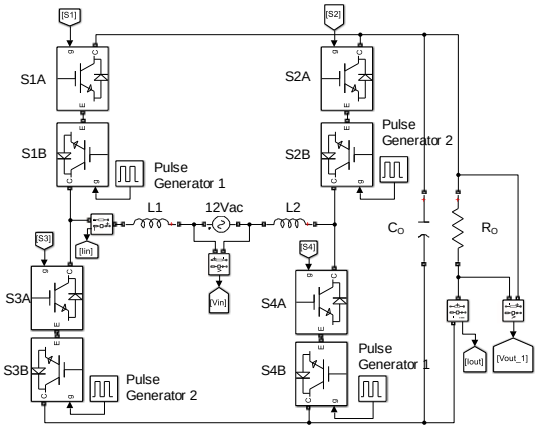
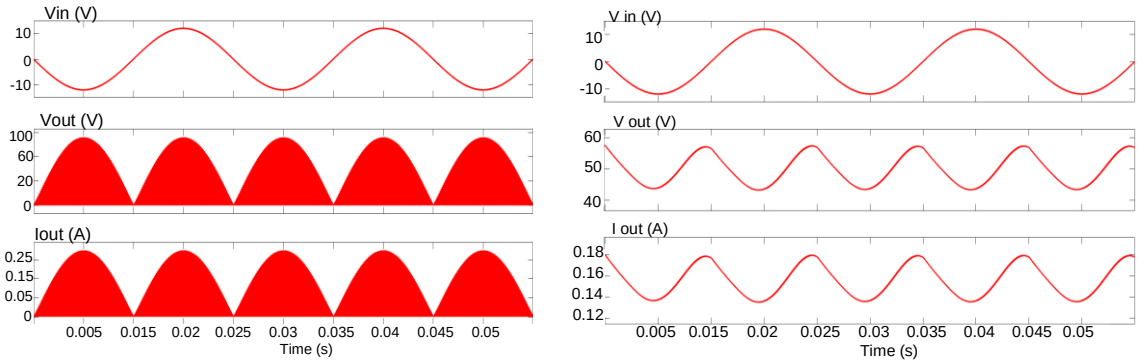


Figure 9. Simulation of open circuit fault-tolerant boost rectifier based on SPMC

6. RESULT AND DISCUSSION

Figure 10(a) shows the outcome of the resistive load simulation conducted using MATLAB/Simulink. The simulation results showcase a distinct cleanliness and smoothness, marked by the absence of any discernible noise or spikes. Simulated components are presumed to behave perfectly, devoid of any real-world variability or noise. The result also shows that the proposed fault-tolerant boost rectifier is able to obtain a boost DC voltage from ac input supply. For the purpose of voltage stabilization, a filter capacitor is integrated in parallel with the resistive load. The inclusion of a capacitive filter leads to the attenuation of output ripples, resulting in a smoother output as shown in Figure 10(b). Comparing the output voltages from both simulations indicating the successful implementation of the capacitive filter. The simulation result proves the workability of boost rectifier based on SPMC.



(a) (b)

Figure 10. Simulation result of resistive load of boost rectifier based on SPMC (a) without capacitive filter and (b) with capacitive filter

Figure 11 illustrates the simulation results for COR 1 to COR 4. All these results are taken during steady-state condition. The voltage signal for every switch in COR 1 until COR 4 is 15 V. For COR 1, switches S3A and S4A are turned on as depicted in Figure 11(a), while S1A and S2A are turned off. In Figure 11(b), switches S1A and S2A in COR 2 are turned on, with S3A and S4A turned off. Moving on to Figure 11(c), switches S2A and S4A in COR 3 are turned on, while S1A and S3A are turned off. Finally, in Figure 11(d), switches S1A and S3A in COR 4 are turned on, while S2A and S4A are turned off. The simulation results for each COR demonstrate that the simulation's functionality closely aligns with the theoretical aspects. The availability of inductor current or input current magnitude for every cycle indicates that there is no fault occurs. The simulation results for CORs demonstrate that the simulated outcomes mirror the theoretical aspects.

Figures 12(a) and 12(b) show the condition of the COR 1 waveforms when fault occurs at switch S3A or S4A. When fault occur during positive half cycle, the output voltage (Vout) is dropped and positive half cycle of input current (Iin) equals to zero the moment of fault occurs. When fault occur during negative half cycle, the

negative cycle of input current (Iin) is equals to zero and the voltage dropped. The same procedure applies to COR 2 as in Figure 13(a) when fault occur at S1A and Figure 13(b) when fault occur at S2A, COR 3 as in Figure 14(a) when fault occur at S4A and Figure 14(b) when fault occur at S2A, and COR 4 as illustrated in Figure 15(a) when fault occur at S1A and Figure 15(b) when fault occur at S3A, respectively.

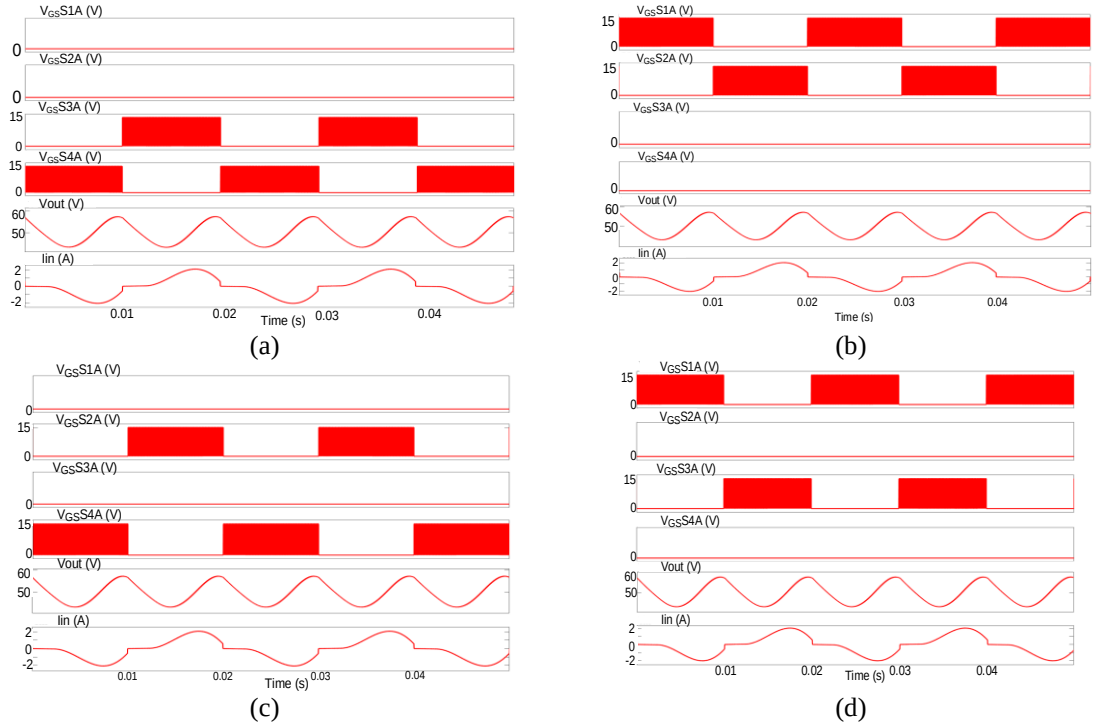


Figure 11. Simulation results boost rectifier based on SPMC (a) COR 1, (b) COR 2, (c) COR 3, and (c) COR 4 switching control during steady state condition

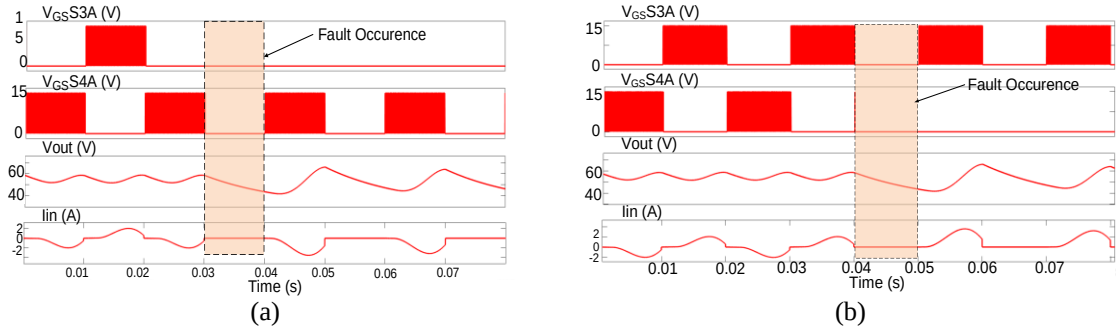


Figure 12. Simulation results of fault identification in COR 1 when fault occur at (a) S3A and (b) S4A

Hence, the integration of fault identification is aimed at precisely pinpointing the location of a faulty switch. It's essential to note that the project's scope encompasses the incorporation of a fault-tolerant strategy, which is a crucial aspect. Enabling the fault-tolerant strategy and facilitating transitions necessitates an effective means of communication between fault identification and fault-tolerant processes. To facilitate this communication, a binary code is introduced to signal the circuit to execute the fault-tolerant transition following fault identification. Tables 3-6 shows the fault identification binary code. As illustrated in Table 3, the binary representation is '110011,' showcasing the fault identification binary code for COR 1. The first two digits indicate that the input current is in a normal condition. The last four digits indicate that VGSS1A and VGSS2A are off while VGSS3A and VGSS4A are on. The 'Normal' condition signifies a normal condition. Conversely, if a fault emerges at switch S3A, affecting the input current, the binary value corresponding to VGSS3A turns to '0', alongside the input current. Consequently, the binary code '100001' signifies that the fault resides at VGSS3A

within COR 1. This binary encoding approach is mirrored in COR 2, COR 3, and COR 4, as shown in Table 4. Table 6 serving as a crucial foundation for future advancements in this project.

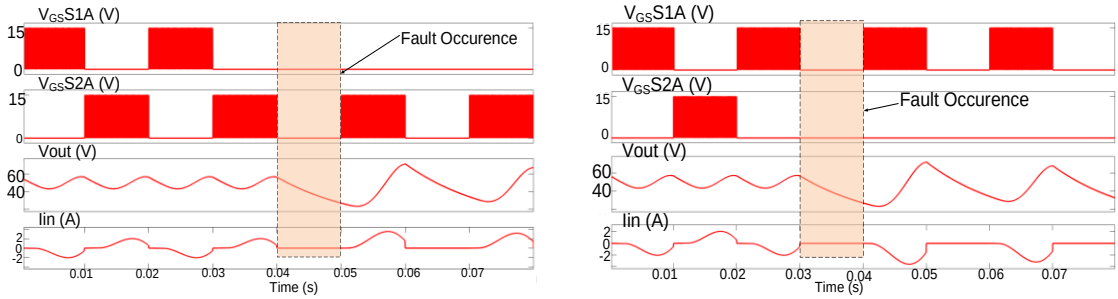


Figure 13. Simulation results of fault identification in COR 2 when fault occur at (a) S1A and (b) S2A

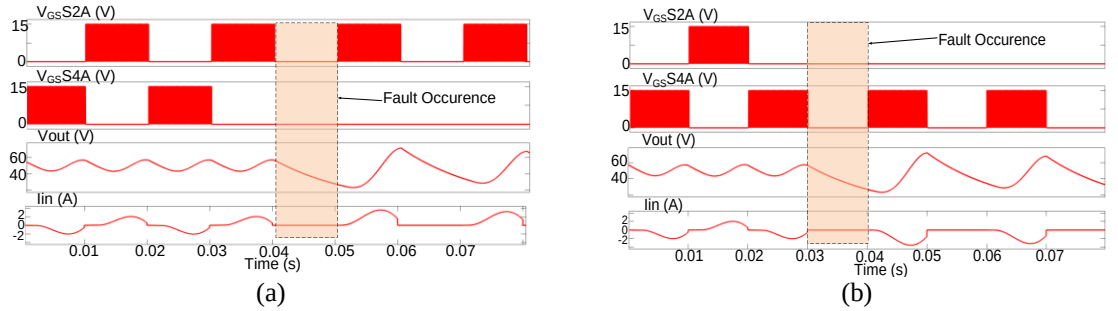


Figure 14. Simulation results of fault identification in COR 3 when fault occur at (a) S4A and (b) S2A

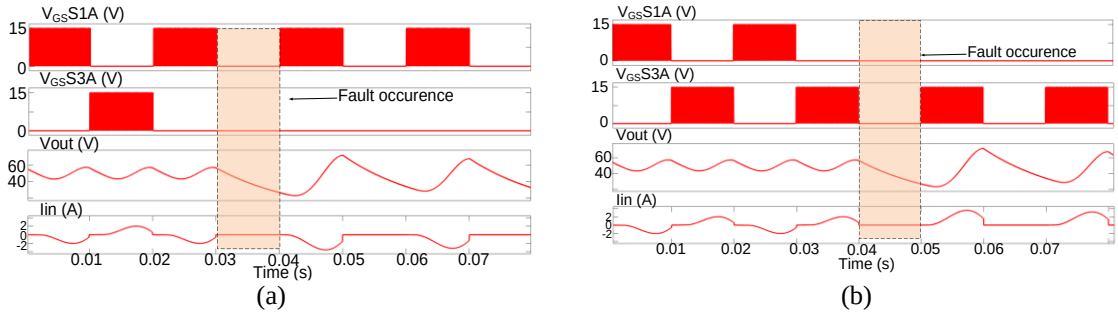


Figure 15. Simulation results of fault identification in COR 4 when fault occur at (a) S1A and (b) S3A

Table 3. Fault identification binary code COR 1

COR 1							
IL/Iin		V_{GS}	V_{GS}	V_{GS}	V_{GS}	Binary	Condition
+ve	-ve	S1A	S2A	S3A	S4A	Code	
1	1	0	0	1	1	110011	Normal
1	0	0	0	0	1	100001	S3A Fault
0	1	0	0	1	0	010010	S4A Fault

Table 4. Fault identification binary code COR 2

COR 2							
IL/Iin		V_{GS}	V_{GS}	V_{GS}	V_{GS}	Binary	Condition
+ve	-ve	S1A	S2A	S3A	S4A	Code	
1	1	1	1	0	0	111100	Normal
1	0	0	1	0	0	100100	S1A Fault
0	1	1	0	0	0	011000	S2A Fault

The fault-tolerant strategy seeks to prevent permanent circuit damage by utilizing the COR in this section to divert current flow away from the faulty switch's location. Illustrated in Figure 16(a) are the results of the fault-tolerant transition from COR 1 to COR 2, while Figure 16(b) presents the outcomes of the fault-tolerant transition from COR 2 to COR 3. Furthermore, Figure 16(c) illustrates the findings of the fault-tolerant transition from COR 3 to COR 4, and Figure 16(d) showcases the results of the fault-tolerant transition from COR 4 to COR 1.

During the transition from COR 1 to COR 2, as depicted in Figure 16(a), in the event of a fault, all voltage signals uniformly drop to zero. The output voltage drops to less than 30 V while the input current

waveform during positive cycle is completely cut-out. After the fault occur initially in COR 1, S1A and S2A are turned on (COR 2) with the assumption that S3A and S4A are open circuited. Once COR 2 is taking over, the output voltage and the input current are recovering. Simulation result shows that fault occurrence is half cycle (10 ms) and the recovering time is one and half cycle (30 ms) approximately. The results from the transition between CORs show that the output power is continuously supplied even when fault occurs. Therefore, the continuity of power supply can be guaranteed.

Table 5. Fault identification binary code COR 3

COR 3							
IL/Iin		V_{GS}	V_{GS}	V_{GS}	V_{GS}	Binary	Condition
+ve	-ve	S1A	S2A	S3A	S4A	Code	
1	1	0	1	0	1	110101	Normal
0	1	0	0	0	1	010001	S2A Fault
1	0	0	1	0	0	100100	S4A Fault

Table 6. Fault identification binary code COR 4

COR 4							
IL/Iin		V_{GS}	V_{GS}	V_{GS}	V_{GS}	Binary	Condition
+ve	-ve	S1A	S2A	S3A	S4A	Code	
1	1	1	0	1	0	111010	Normal
0	1	1	0	0	0	011000	S3A Fault
1	0	0	0	1	0	100010	S1A Fault

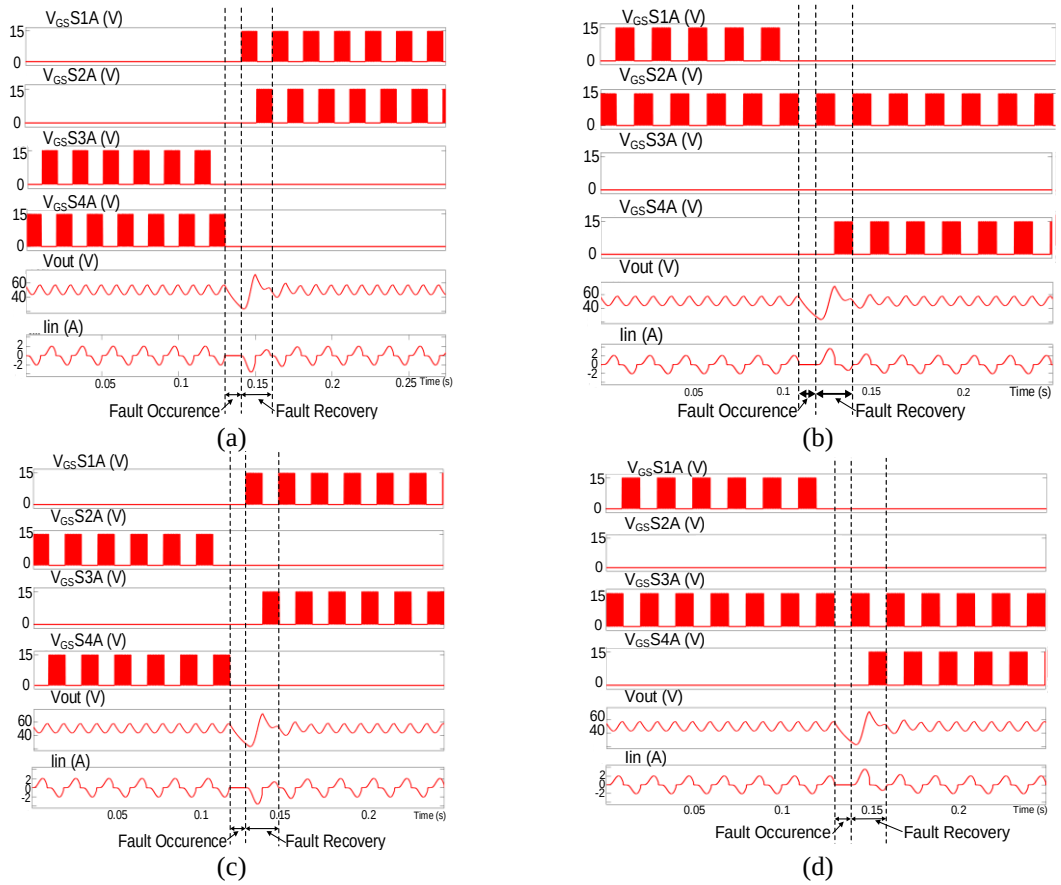


Figure 16. Simulation results of open circuit fault-tolerant boost rectifier based on SPMC
(a) COR 1 to COR 2, (b) COR 2 to COR 3, (c) COR 3 to COR 4, and (d) COR 4 to COR 1

7. CONCLUSION

In conclusion, this paper marks a significant contribution in the area of fault identification, fault-tolerant strategies, and their integration in boost rectifier based on SPMC. The fault identification simulation represents a pioneering step in addressing fault-related challenges in power electronics. By systematically designing a method to identify the exact location of the faulty switches in the proposed boost rectifier based on SPMC. The incorporation of a binary code for communication between system components, along with its integration into fault-tolerant strategies, enhances the circuit's resilience and continuous operation.

The fault-tolerant strategy, employing COR, redirects current flow from faulty switches to maintain circuit continuity. The implementation of Four distinct COR demonstrates their effectiveness in adapting to different fault conditions, ensuring consistent delivery of output voltage and current. The operational dynamics of each COR have been thoroughly elucidated, showcasing their effectiveness in maintaining circuit continuity

even when faults arise. Therefore, the continuity of power supply to the load can be guaranteed to avoid interruption of the whole system.

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