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Design and implementation of grid tied high step-up DC-DC converter with switched capacitor

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ABSTRACT

In this paper, the design and implementation of a three-phase grid-connected inverter coupled with a high step-up DC-DC converter with a switched capacitor is demonstrated. In this converter two capacitors are utilized with a coupled inductor. The charging of capacitors takes place parallel and discharging in series during switch off and switch on time respectively. The energization of the coupled inductor provides the high voltage gain. The passive clamp circuit is used to recycle the leakage energy of the inductor circuit. Therefore, the switch stress is reduced. This high gain converter is given DC input of 40 V and a high voltage 538 V obtained is supplied to the grid connected inverter which uses sinusoidal pulse width modulation (SPWM), to obtain 3phase line-neutral voltage of 415 V from inverter for grid synchronization. A high voltage gain of 13 and efficiency of 96% is obtained for different load and voltage variation. The modeling and the simulation are done using physical security information management (PSIM) Software and all the results are presented in this paper.

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1. INTRODUCTION

To raise the PV voltage to the link's DC voltage, on-grid inverters often use a DC-DC converter. Boost converters are one of many types of DC-DC converters that are frequently utilized. However, a three-phase inverter actually needs a high input voltage and the sole factor affecting the boost converter's output voltage is the duty cycle. Therefore, if the PV voltage deviates greatly from the DC link voltage, it is challenging for the boost converter to provide the voltage required by the inverter.

In this paper, a low-voltage system's three-phase inverter with grid connectivity was designed. This system has the advantage of being able to generate high voltages while taking up less space, and it also allows for the regulation of output voltage. Due to its reliable and straightforward implementation, the grid connection system uses the sinusoidal pulse width modulation (SPWM) approach [1]–[5]. This research suggests a brand-new high step-up ratio and clamp-mode converter to achieve high step-up voltage gain and high efficiency. A significant step-up voltage gain is attained by the suggested converter by adding two capacitors and two diodes to the coupled inductor's secondary side. Two capacitors can be parallel-charged and serial-discharged using the connected inductor. But the connected inductor's leakage inductor could result in significant power loss and a spike in voltage at the switch. To clamp the voltage level of the main switch and recycle the energy from the leakage inductor, a passive clamping circuit is therefore required [6]-[17].

2. METHODOLOGY

Currently, photovoltaic (PV) systems connected to the grid are more common than standalone systems. Since batteries are not required for grid-connected systems, they are more cost-effective. The circuit diagram of the complete model is shown in Figure 1. In this paper, a PV system's grid-connected three-phase inverter was created for usage with three-phase networks in buildings. An on-grid inverter works on a similar principle as an off-grid inverter, but in order for network synchronization to take place, the sine wave produced at the AC voltage that is supplied must match the wave that is owned by the grid. A block schematic of the system that we designed can be seen in Figure 2 where the dc converter is connected to an inverter.

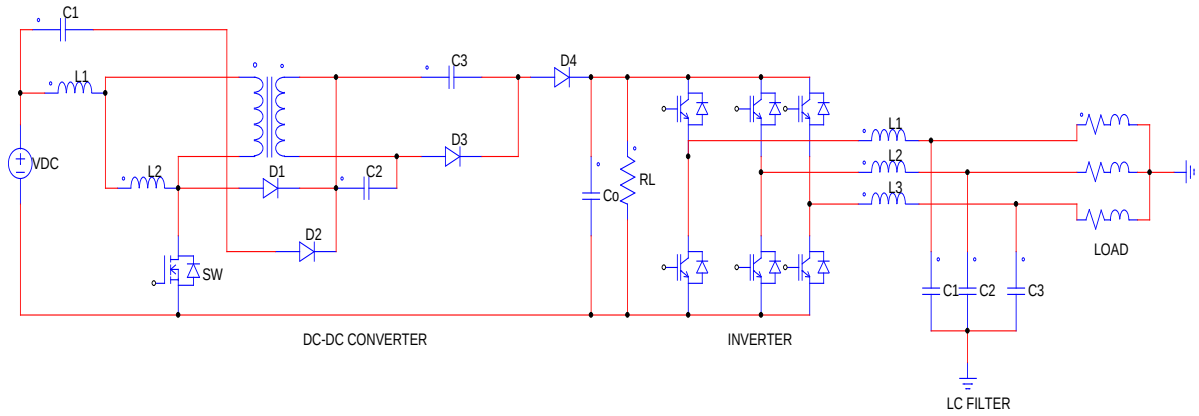

Figure 1. Circuit of the complete model

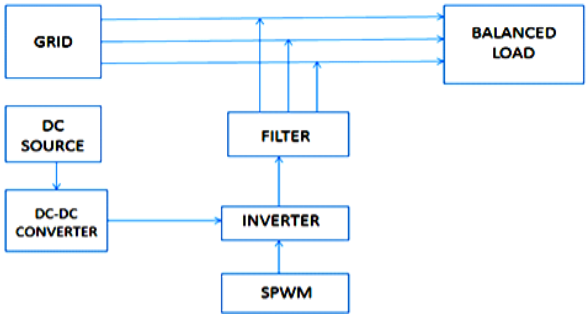

Figure 2. Block diagram of on-grid inverter system

3. HIGH GAIN DC-DC CONVERTER WITH SWITCHED CAPACITOR

A 3-phase inverter requires a certain voltage, which is provided by a DC-DC converter. A novel high-step-up DC-DC converter is required for this project. Utilizing two capacitors and a single connected inductor is the idea. To generate a large step-up voltage gain, the two capacitors are charged in parallel during the switch-off time and discharged in series during the switch-on period by the energy stored in the connected inductor. A passive clamp circuit is also used to recycle the linked inductor's leakage-inductor energy. As a result, the main switch experiences less voltage stress [18]-[30].

3.1. Modes of operation

The suggested converter's circuit topology includes DC input voltage Vin, the primary switch S, coupled-inductor Np and Ns, a clamp diode D1, a clamp capacitor C1, two diodes D2 and D3, an output diode Do, and an output capacitor Co. Capacitors can be parallel-charged and series-discharged to achieve high step-up gain, according to the switched-capacitor technique in [3]. The primary working concept is that when the switch is flipped on, the connected inductor induces a voltage on the secondary side and the magnetic inductor Lm is charged by Vin. Vin, VC1, VC2, and VC3 all release energy in response to the induced voltage and output it in series. The linked inductor functions as a transformer in the forward converter. In order to charge capacitors C2 and C3 in parallel, magnetic inductor Lm releases energy when the switch is switched off. This energy is released via the connected inductor's secondary side. The linked

inductor functions as a transformer in a flyback converter. To make the circuit analysis easier, it is assumed that the following things are true: i) C1, C2, C3, and Co are large, so Vc1, Vc2, Vc3, and Vo are constant in one switching period; ii) The power devices are ideal, but the parasitic capacitor of the power switch is taken into account; and iii) The coupling coefficient of the coupled-inductor k is equal to Lm/(Lm+Lk). The circuit configuration of the proposed converter is shown in Figure 3.

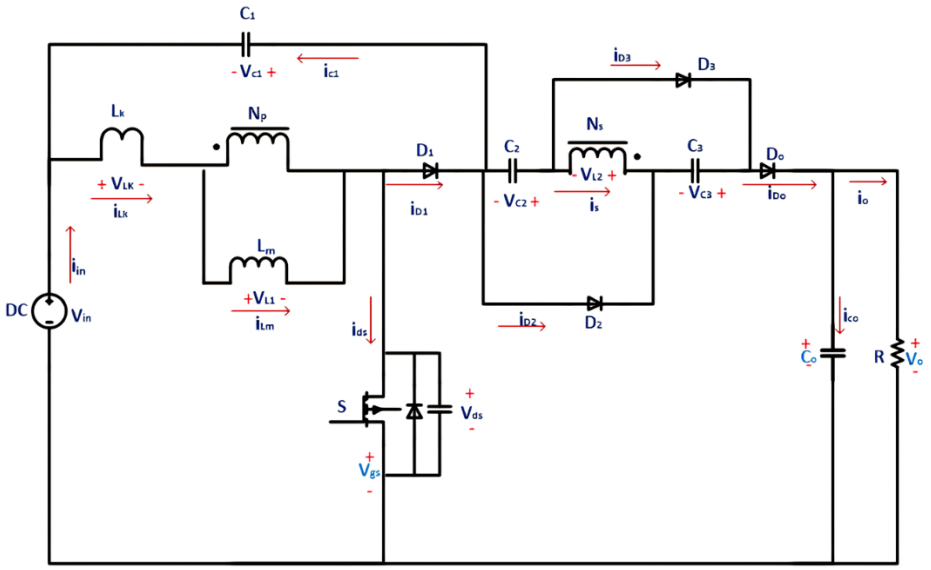

Figure 3. Circuit configuration of the proposed converter

3.2. Continuous conduction mode (CCM Operation)

The operation of the suggested converter is described in this section. Five operating modes are available throughout one switching time in CCM operation. These are the operational modes' descriptions:

i) Mode I

Mode I: S is activated between these two times (t0, t1). In contrast to D1 and Do, diodes D2 and D3 are now on. Figure 1 depicts the current-flow path. Vin=VLk + VLm is how the voltage equation for the coupled inductor's primary side leakage and magnetic inductors is written. With the help of Vin, the leaking inductor Lk begins to charge. The connected inductor's secondary-side current linearly decreases because of the leakage inductor Lk. Energy is supplied to load R by output capacitor Co. This operating mode ends when current iD2 at time t = t1 equals zero. The operation during Mode-I is shown in Figure 4.

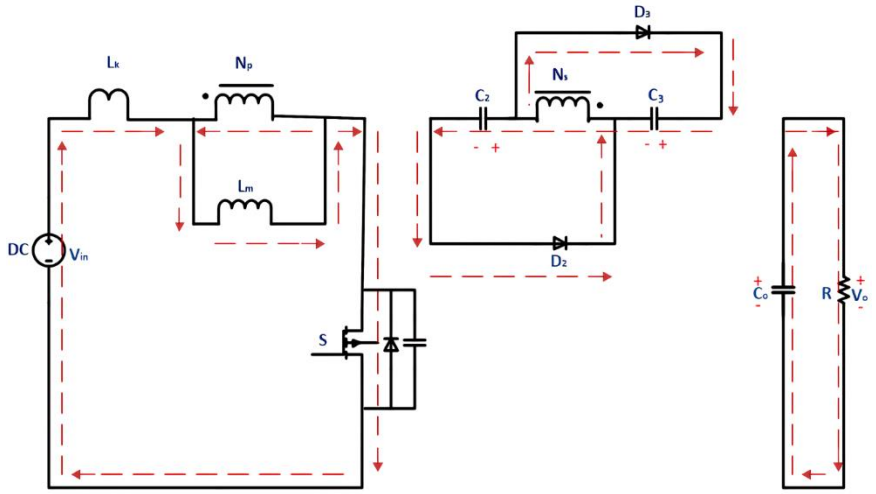

Figure 4. Mode I

ii) Mode II

Mode II [t1, t2]: S is kept powered on during this time frame. When do is turned on, the diodes D1, D2, and D3 are all off. Figure 1 depicts the current-flow path. DC-source Vin produces energy, which is stored by the magnetizing inductor Lm. The linked inductor allows some of Vin's DC-source energy to flow to the secondary side. Induced voltage VL2 on the coupled inductor's secondary side causes Vin, Vc1, Vc2, and Vc3 to connect in series discharge to the high-voltage output capacitor Co and the load R. Switching off S at time t = t2 puts an end to this operational mode. The operation during Mode-II is shown in Figure 5.

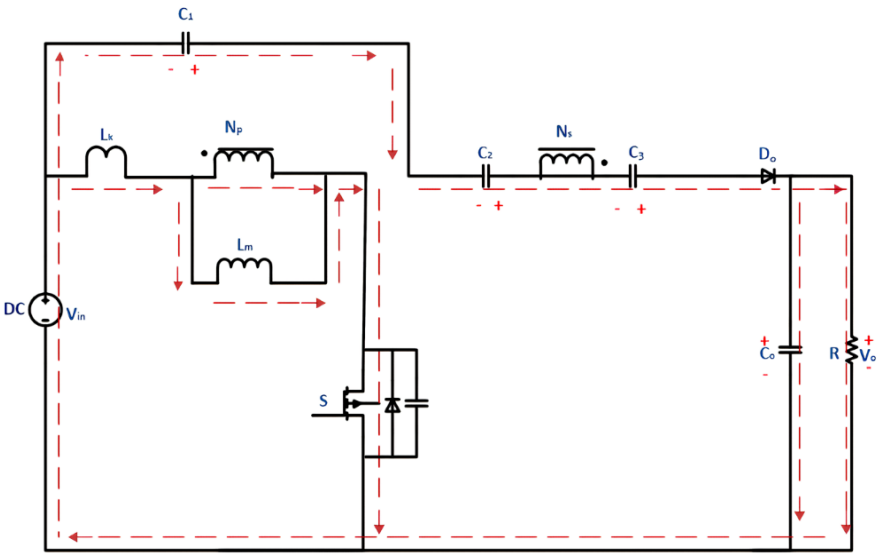

Figure 5. Mode II

iii) Mode III

S is turned off in Mode III [t2, t3] throughout this time period. When Do is turned on, the diodes D1, D2, and D3 are all off. Figure 1 depicts the current-flow path. The parasitic capacitor Cds of the main switch S is charged by the energy of the leakage and magnetizing inductors Lk and Lm, respectively. Energy is supplied to load R by output capacitor Co. When diode D1 conducts and this working mode is terminated at time t = t3, capacitor voltage Vc1 equals Vin+Vds. The operation during Mode-III is shown in Figure 6.

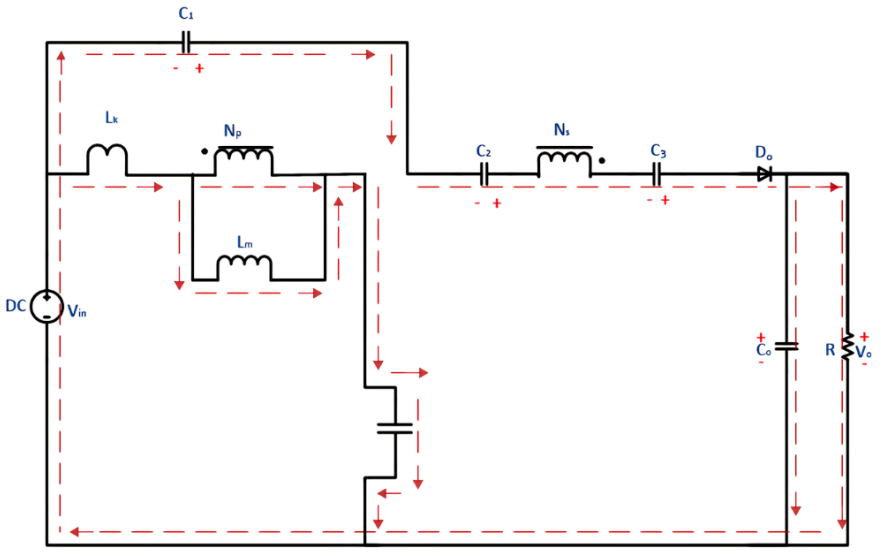

Figure 6. Mode III

iv) Mode IV

S is turned off in Mode IV [t3, t4] throughout this time period. In contrast to D2 and D3, diodes D1 and Do are on. Figure 1 depicts the current-flow path. Charge clamp capacitor C1 is energized by the energy of the leakage and magnetizing inductors. Energy is recycled by the leakage inductor Lk. iLk as of now is rapidly declining. Until the linked inductor's secondary current is equal to zero, the secondary side voltage VL2 of the coupled inductor keeps charging the load R and high-voltage output capacitor Co in series. D2 and D3 begin to turn on in the background. This operating mode expires when Ido is equal to 0 at time t = t4. The operation during Mode-IV is shown in Figure 7.

v) Mode V

S is turned off in Mode V [t4, t5] throughout this time period. Do is switched off, while diodes D1, D2, and D3 are active. Figure 1 depicts the current-flow path. Co is discharged from the output capacitor to the load R. Clamp capacitor C1 is charged by the energy of the leakage and magnetizing inductors Lk and Lm. Through the secondary side of the linked inductor, the magnetizing inductor Lm is discharged, charging capacitors C2 and C3. As a result, capacitors C2 and C3 receive parallel charging. Capacitor C1 is charged by Lk using the leaky inductor's energy. Gradually, the iLk changes from low to high. At t = t6, when S is turned on at the start of the subsequent switching period, this mode comes to an end. The operation during Mode-V is shown in Figure 8.

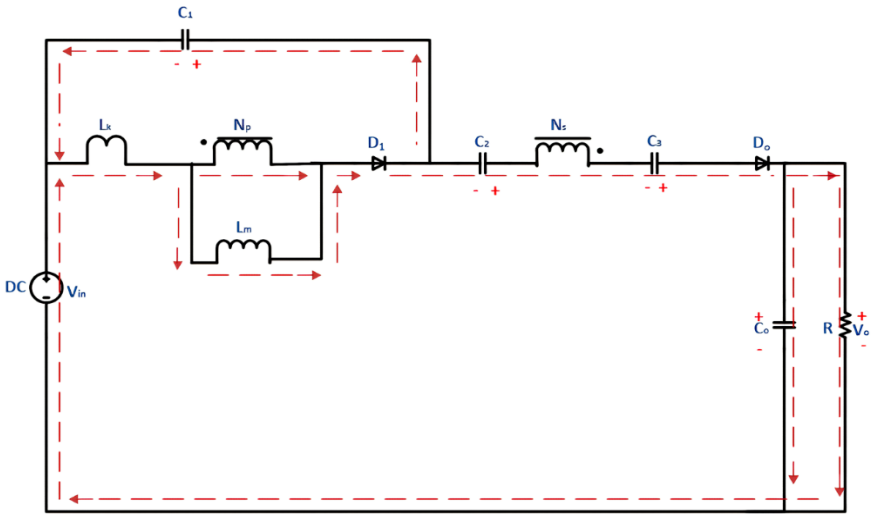

Figure 7. Mode IV

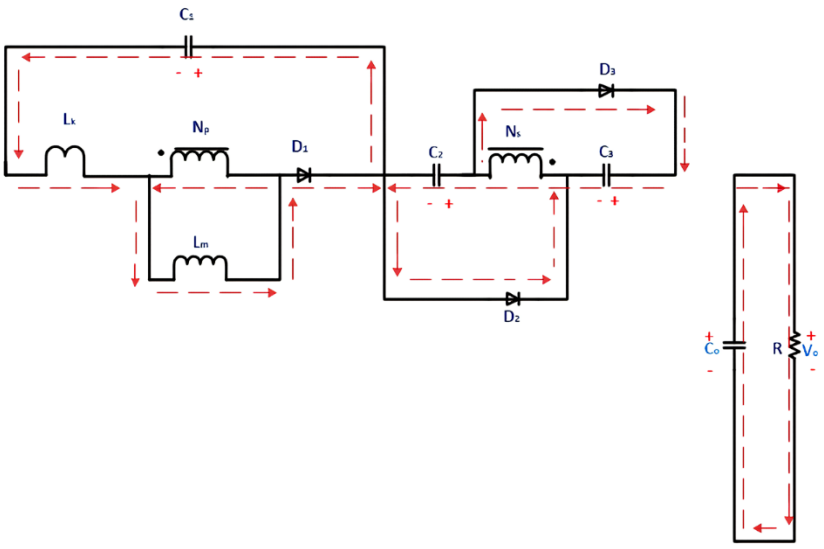

Figure 8. Mode V

To change DC electricity into AC, a circuit known as an inverter is utilized. A voltage source inverter, or voltage source inverter (VSI), is one of the most used kinds of inverters. Equipment that demands a lot of power frequently uses three-phase inverters. 6 switches make up the fundamental three-phase inverter circuit. High power ratings and high frequency switching capabilities are required of the relevant electronic components acting as switches. In order to do this, the insulated gate bipolar transistor (IGBT) was selected for the three-phase inverter architecture. The circuit diagram of three phase inverter is shown in Figure 9.

The MOSFET/IGBT switching in the inverter causes the sine wave to be formed at the inverter output. A sine wave is created by this switching. One of the switching techniques that is frequently used to provide inverter output that takes the form of sinusoidal signals is the SPWM technique. As a method of grid synchronization control in this investigation, SPWM is also employed. The flowchart of the complete system is shown in Figure 10.

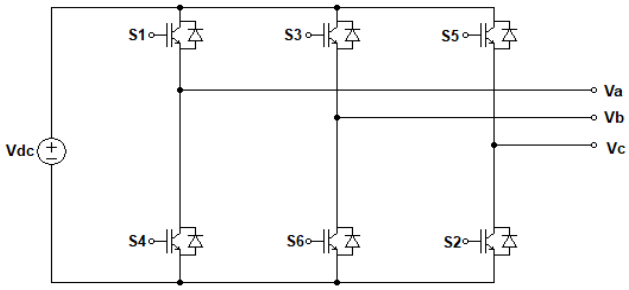

Figure 9. 3-Ø inverter

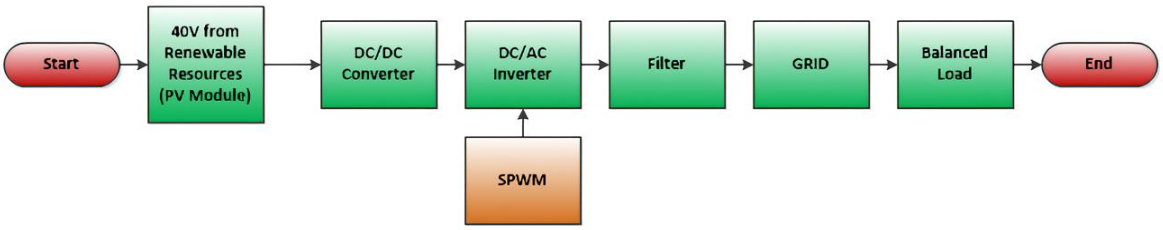

Figure 10. Flowchart of the complete working of the entire system

4. CALCULATION OF LC FILTER

L blocks the dominant harmonics. C provides easy path for n^{th} harmonic ripple currents. We have seen that V_n can be represented as (1).

$$V_n = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t - \frac{4V_m}{15\pi}\cos 4\omega t \quad (1)$$

In order that Capacitor provides easy path for harmonic components. Load impedance ZL >> XC => ZL > > $\frac{1}{n\omega c}$. n = Order of harmonic current. In practice Capacitor provides effective filtering if:

$$Z_{nL} = \frac{10}{n\omega c}$$

$$\sqrt{R^2 + (n\omega L_L)^2} = \frac{10}{n\omega c} \quad (2)$$

Under condition (2) we can neglect the load impedance for analysis: ∴ n^{th} harmonic current $I_n = \frac{Vn}{n\omega L - \frac{1}{n\omega c}}$, V_n = rms of n^{th} harmonic voltage, and n^{th} harmonic rms output voltage across 'C'.

$$V_{on} = V_n \left[\frac{-(\frac{1}{n\omega c})}{n\omega L - \frac{1}{n\omega c}}\right] = \frac{-1}{[(2\omega)^2 Lc - 1]} V_n \quad (3)$$

As 2nd harmonic is most dominant, so ripple voltage can be taken as 2nd harmonic component only. From (1):

$$V_n = \frac{2V_m}{\pi} - \frac{4V_m}{3\pi}\cos 2\omega t - \frac{4V_m}{15\pi}\cos 4\omega t$$

$$V_2 = -\frac{4V_m}{3\pi}\cos 2\omega t$$

$$V_2 = \frac{1}{\sqrt{2}} * \frac{4V_m}{3\pi}$$

$$V_r = V_{o2} = \frac{1}{[(2\omega)^2 Lc - 1]} V_2 \quad (4)$$

$$VRF = \frac{V_r}{V_o} = \frac{V_2}{V_o} = \left(\frac{4V_m}{\sqrt{2}*3*\pi[(2\omega)^2 Lc - 1]}\right) / \frac{2V_m}{\pi}$$

$$= \frac{\sqrt{2}}{3}\left[\frac{1}{(2\omega)^2 Lc - 1}\right] \quad (5)$$

The value of 'C' can be obtained from in (2) as:

$$C = \frac{10}{2\omega\sqrt{R^2 + (n\omega L_L)^2}} \quad (6)$$

And L can be obtained for a given VRF from (5). In this model, we have taken load resistance R_L = 20 Ω and load inductance L_L = 5 mH. The voltage ripple factor is 10%. So, as we know $C = \frac{10}{2\omega\sqrt{R^2+(n\omega L)^2}}$. Hence,

$$C = \frac{10}{2(2 * \pi * 50)\sqrt{20^2 + (2 * 2 * \pi * 50 * 5 * 10^{-3})^2}} = 786.135\ \mu F$$

Also, we know that $L = \frac{1+\frac{\sqrt{2}}{3*VRF}}{4\omega^2 C}$. Hence, $L = \frac{1+\frac{\sqrt{2}}{3*0.1}}{4(2*\pi*50)^2*786.135*10^{-6}} = 18.41\ mH$.

5. SIMULATION RESULTS AND ANALYSIS

5.1. Design parameters

In order to design the DC-DC converter following design parameters are used, where for an input voltage of 40 V an output of 538 V is obtained. A 200 W system is designed using the following parameters. The simulation of the circuit was done using these design parameters: input DC voltage V_{in} = 40 V, output DC voltage V_o = 538 V, maximum output power = 200 W, switching frequency = 50 KHZ, L_m = 48 µH, L_k = 0.25 µH, C_1 = 56 µF, C_2 = C_3 = 22 µF, and C_o = 180 µF/600 V.

5.2. Analysis

The simulation model of the proposed converter is shown in Figure 11 and the complete grid tied model is shown in Figure 12. For an input voltage of 40V a high output voltage of 538 V is obtained from the high gain converter which can be easily synchronized with the grid through a 3-phase inverter as shown in the above figure. An LC filter is also designed to remove the harmonics of the inverter for grid connection. The output voltage obtained from the DC-DC converter is shown in Figure 13.

The gating pulses were obtained by using sinusoidal pulse width modulation technique as shown in Figure 14 and Figure 15 sinusoidal pulse width modulation technique is implemented with the 3-phase inverter. Figure 14 shows the carrier and sinusoidal signal and Figure 15 shows the individual gating pulse of the switches of the inverter. In Figure 16, Figure 17 and Figure 18 the waveforms for three-phase load line to neutral voltage, Line- neutral voltage of inverter output without filter, Line- neutral voltage of inverter output with filter of 415 V obtained are shown.

The variation of output voltage with different load is shown in Figures 19 and 20. The Table 1 shows the output power and efficiency of the converter for different load and input voltage. The change in efficiency with variation in load is shown in Figure 21 and is found to be almost constant at 96%.

Table 1. The output power and efficiency of the converter for different load and input voltage

Input voltage (V_{in}) in Volts	Input current (I_{in}) in ampere	Input power (P_{in}) in watt	Output voltage (Vo) in volts	Output current (I_o) in ampere	Output power (P_o) in watt	Efficiency (%)
40	3.872	142.4	538	0.276	148.7	96
35	3.524	118	455	0.259	118.24	95.86
25	2.823	75.73	315	0.211	66.675	94.97
20	1.899	34.25	252	0.14	36.675	96.38

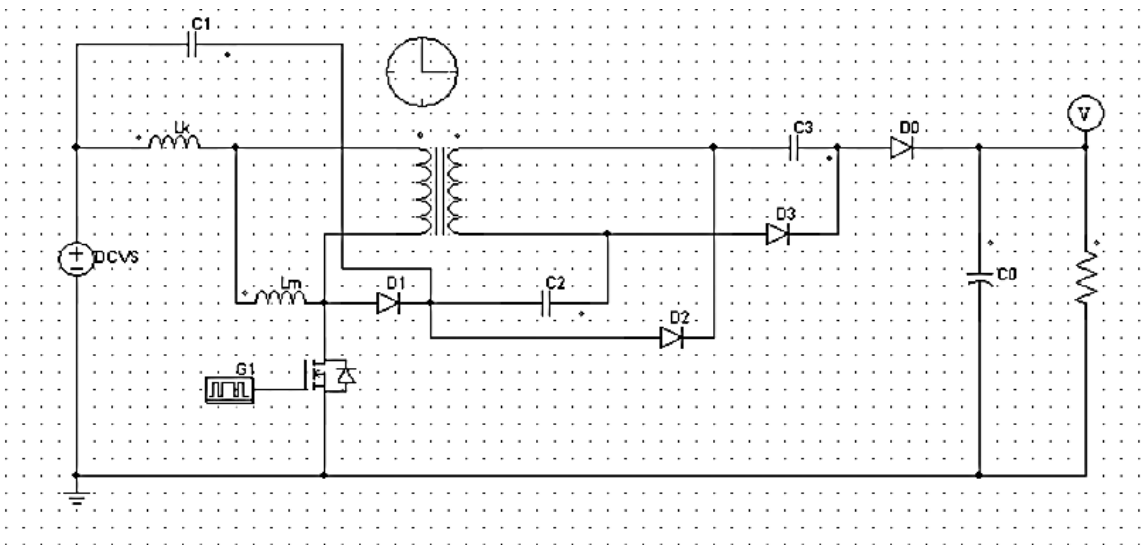

Figure 11. Simulation circuit of the DC-DC converter

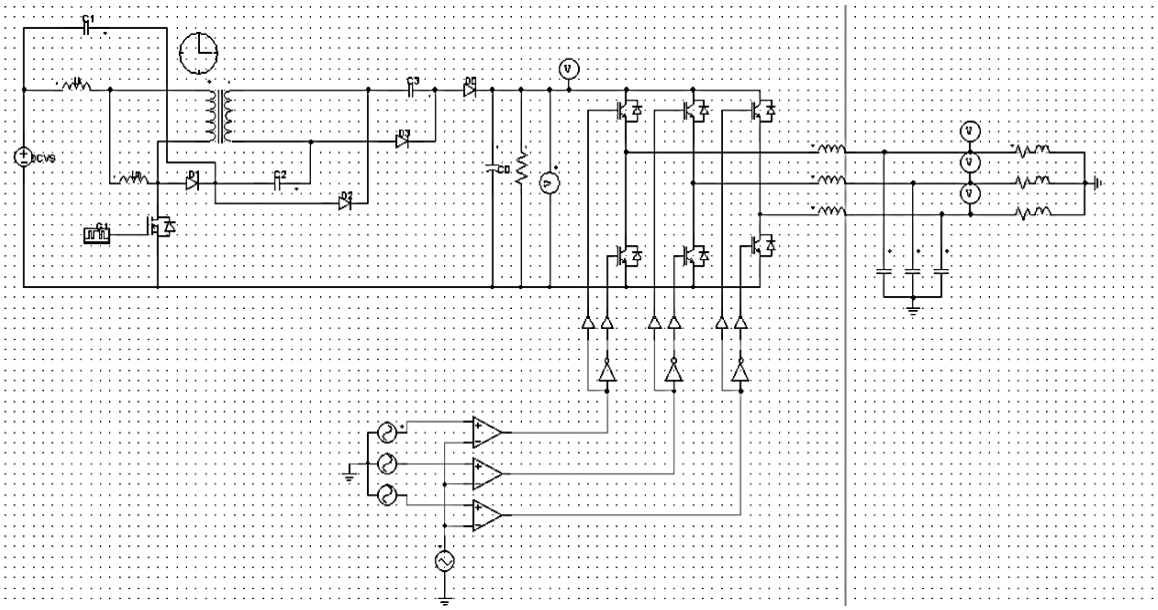

Figure 12. Simulation circuit for a complete model

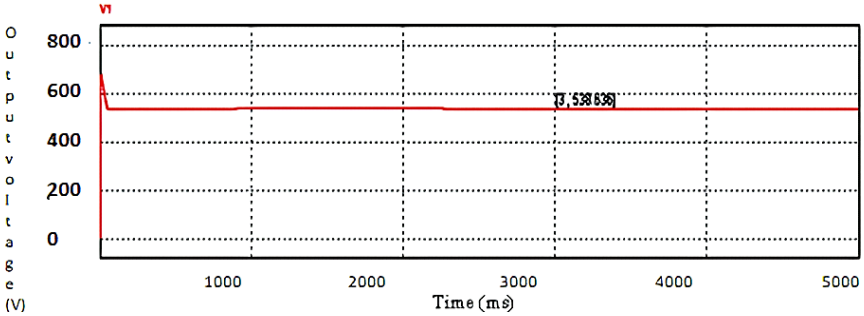

Figure 13. Output voltage of the converter

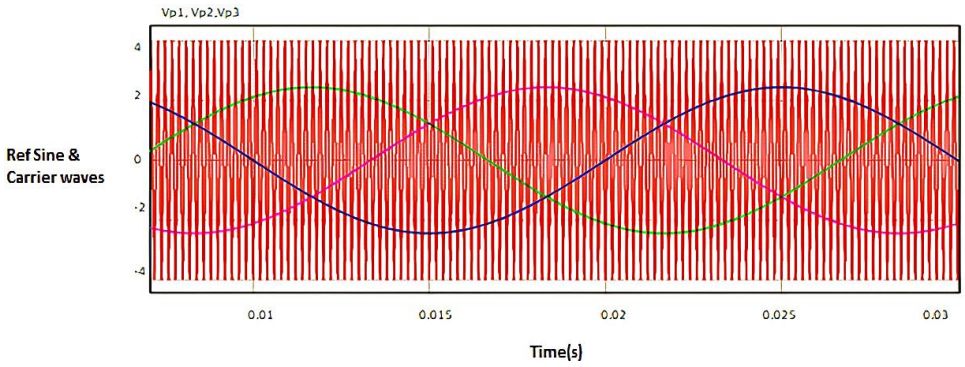

Figure 14. Reference sine waves and carrier triangular signal

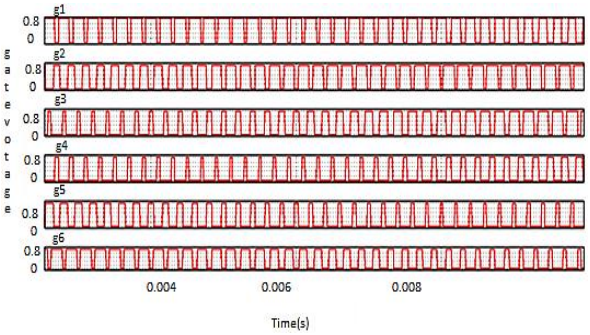

Figure 15. Individual switching signals (g1, g2, g3, g4, g5, g6) for three phase voltage source Inverter

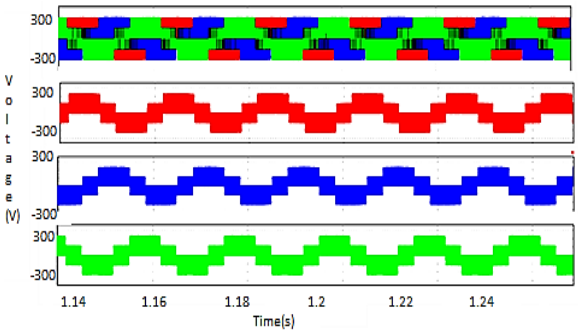

Figure 16. Three-phase load line to neutral voltage

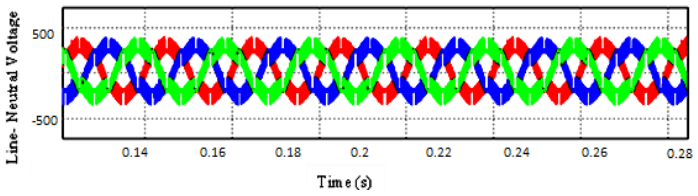

Figure 17. Line- neutral voltage of inverter output without filter

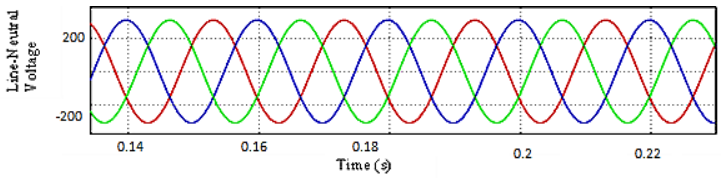

Figure 18. Line- neutral voltage of inverter output with filter

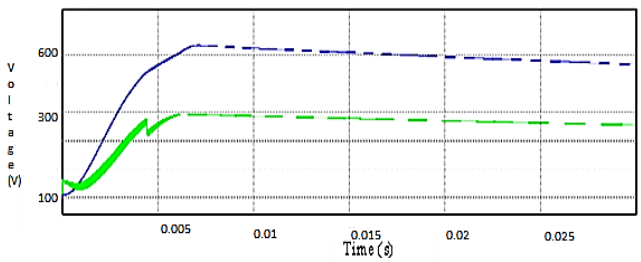

Figure 19. Variation in output voltage with change in load where V_o = 455 V and 252 V

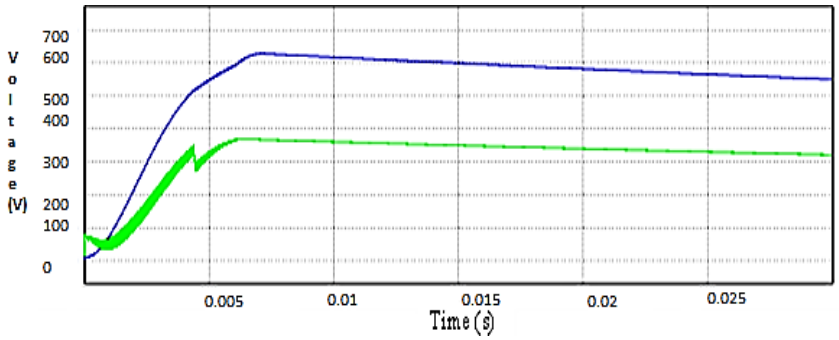

Figure 20. Variation in output voltage with change in load where V_o = 538 V and 315 V

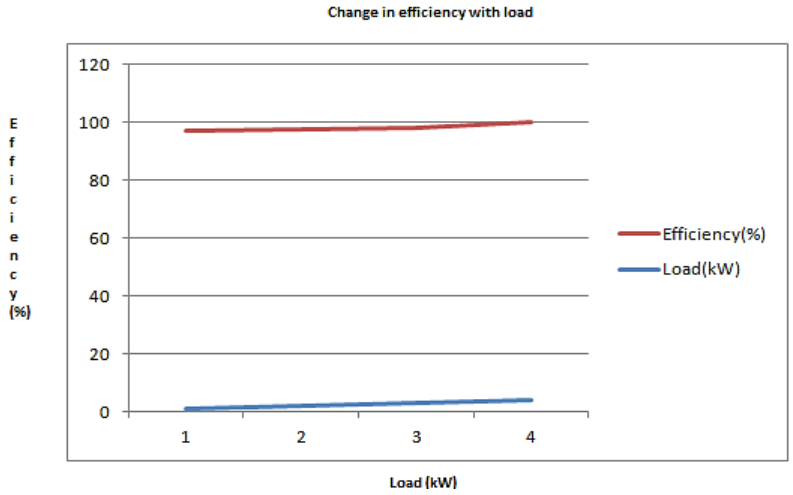

Figure 21. Change in efficiency with variation in load

5.3. Performance limitation and advantages of the proposed converter

A problem with switched capacitor converter is that, it is difficult to ensure good output voltage regulation in the presence of wide load variation and in particular when there is an input voltage variation. In switch converter even if with the ideal components it has a non-zero output resistance, without filter the losses in the converter power stage increase. As the losses increases the efficiency of the converter get compromised.

As in this converter two capacitors and two diodes are added on the secondary side of the couple inductor in order to obtain high voltage gain. Therefore, a passive clamping circuit is used to clamp the voltage across the main switch and to recycle the energy of the leakage inductor. Hence high voltage ratio can be maintained for wide load variation as the losses are reduced during the conversion stage the efficiency is maintained high.

5.4. Comparison with other DC-DC converters

In converter topologies using transformer high voltage gain is achieved by adjusting the turns ratio. But this leads to high voltage spike across the main switch due to leakage inductor energy of the transformer. This will further lead to high power dissipation and losses. The converter using inductors also suffer from high voltage stress across the main switch the magnetic design issues lower conversion efficiency, high noise and high electromagnetic interference.

This proposed converter can be used for high power application as the capacitor can store 10-100 times more energy per volume than inductors. As the clamped circuit is used the voltage stress on the main switch is drastically reduced and hence the losses are also low thereby increasing the efficiency. For high power application the selection of the main switch plays a vital role as conduction lose increases with high R_{DSON} of the main switch but in this topology as the leakage energy of the inductor is recycled with the clamping circuit the main switch with the low R_{DSON} can be selected thereby reducing the conduction losses.

As the reverse recovery problem of the diode is eliminated in this circuit hence the efficiency is improved. It has low electromagnetic interference and lower cost due to reduction in component size and rating.

6. CONCLUSION

In this work the proposed switched capacitor high gain DC-DC converter is modeled and designed which can be connected with a 3-phase inverter for grid synchronization. The simulation model of the proposed converter is done using physical security information management (PSIM) Software and also the 3-phase inverter with SPWM technique is modeled using this software. For grid synchronization, we have used the SPWM method because the phase angle and frequency at the inverter output match the grid. A LC filter was also designed to remove the harmonics of the output voltage during grid synchronization. A high voltage gain of 13 is obtained for different input voltages, hence can be used for high voltage application. Here we used a dc voltage source of 40V and used a high step-up DC-DC capacitor switched converter to increase it to around 538 V and output voltage of the converter applied to the inverter circuit for a grid tied system and we got the three-phase line-neutral voltage of around 415V. With the variation of load and input voltage the efficiency of the proposed converter is found to be 96%, hence it provides high efficiency and good voltage regulation.

REFERENCES

[1] G. G. Ramanathan and N. Urasaki, "Non-Isolated Interleaved Hybrid Boost Converter for Renewable Energy Applications," *Energies*, vol. 15, no. 2, 2022, doi: 10.3390/en15020610.

[2] J. Zhao, D. Chen, and J. Jiang, "A novel transformerless high step-Up DC-DC converter with active switched-inductor and quasi-Z-source network," *IET Power Electronics*, vol. 14, no. 9, pp. 1592–1605, 2021, doi: 10.1049/pel2.12128.

[3] H. Gholizadeh, S. A. Gorji, E. Afjei, and D. Sera, "Design and implementation of a new cuk-based step-up dc–dc converter," *Energies*, vol. 14, no. 21, 2021, doi: 10.3390/en14216975.

[4] Y. Zhang, H. Liu, J. Li, M. Sumner, and C. Xia, "DC-DC Boost Converter with a Wide Input Range and High Voltage Gain for Fuel Cell Vehicles," *IEEE Transactions on Power Electronics*, vol. 34, no. 5, pp. 4100–4111, 2019, doi: 10.1109/TPEL.2018.2858443.

[5] A. F. Algamluoli and X. Wu, "A New Single-Cell Hybrid Inductor-Capacitor DC-DC Converter for Ultra-High Voltage Gain in Renewable Energy Applications," *Electronics*, vol. 12, no. 14, p. 3101, Jul. 2023, doi: 10.3390/electronics12143101.

[6] V. Karthikeyan, S. Kumaravel, and G. Gurukumar, "High Step-Up Gain DC-DC Converter with Switched Capacitor and Regenerative Boost Configuration for Solar PV Applications," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 66, no. 12, pp. 2022–2026, 2019, doi: 10.1109/TCSII.2019.2892144.

[7] R. Stala, Z. Waradzyn, A. Mondzik, A. Penczek, and A. Skala, "DC-DC high step-up converter with low count of switches based on resonant switched-capacitor topology," *2019 21st European Conference on Power Electronics and Applications, EPE 2019 ECCE Europe*, 2019, doi: 10.23919/EPE.2019.8914785.

[8] M. K. Nguyen, T. D. Duong, and Y. C. Lim, "Switched-capacitor-based dual-switch high-boost DC-DC converter," *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4181–4189, 2018, doi: 10.1109/TPEL.2017.2719040.

[9] Z. Waradzyn, R. Stala, A. Mondzik, A. Penczek, A. Skala, and S. Pirog, "Efficiency Analysis of MOSFET-Based Air-Choke Resonant DC-DC Step-Up Switched-Capacitor Voltage Multipliers," *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 8728–8738, 2017, doi: 10.1109/TIE.2017.2698368.

[10] H. Ardi, A. Ajami, F. Kardan, and S. N. Avilagh, "Analysis and Implementation of a Nonisolated Bidirectional DC-DC Converter with High Voltage Gain," *IEEE Transactions on Industrial Electronics*, vol. 63, no. 8, pp. 4878–4888, 2016, doi: 10.1109/TIE.2016.2552139.

[11] F. L. Tofoli, D. de C. Pereira, W. J. de Paula, and D. de S. Oliveira Júnior, "Survey on non-isolated high-voltage step-up dc-dc topologies based on the boost converter," *IET Power Electronics*, vol. 8, no. 10, pp. 2044–2057, 2015, doi: 10.1049/iet-pel.2014.0605.

[12] A. Cervera, M. Evzelman, M. M. Peretz, and S. S. Ben-Yaakov, "A high-efficiency resonant switched capacitor converter with continuous conversion ratio," *IEEE Transactions on Power Electronics*, vol. 30, no. 3, pp. 1373–1382, 2015, doi: 10.1109/TPEL.2014.2317758.

[13] K. Kesarwani, R. Sangwan, and J. T. Stauth, "Resonant-Switched Capacitor Converters for Chip-Scale Power Delivery: Design and Implementation," *IEEE Transactions on Power Electronics*, vol. 30, no. 12, pp. 6966–6977, 2015, doi: 10.1109/TPEL.2014.2384131.

[14] R. W. Erickson and Maksimovic, "Fundamentals of Power Electronics," Wiley: Hoboken, NJ, USA, 2013.

[15] H. Jeong, M. Kwon, and S. Choi, "Analysis, Design, and Implementation of a High Gain Soft-Switching Bidirectional DC–DC Converter With PPS Control," *IEEE Transactions on Power Electronics*, vol. 33, no. 6, pp. 4807–4816, Jun. 2018, doi: 10.1109/TPEL.2017.2738705.

[16] M. A. Salvador, T. B. Lazzarin, and R. F. Coelho, "High Step-Up DC–DC Converter With Active Switched-Inductor and Passive Switched-Capacitor Networks," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 7, pp. 5644–5654, Jul. 2018, doi: 10.1109/TIE.2017.2782239.

[17] L. Mitra and U. K. Rout, "Performance analysis of a new high gain dc–dc converter interfaced with solar photovoltaic module," *Renewable Energy Focus*, vol. 19–20, pp. 63–74, 2017, doi: 10.1016/j.ref.2017.05.001.

[18] L. Mitra and U. K. Rout, "Single switched inductor capacitor coupled transformerless high gain converter for PV application," *2016 IEEE 6th International Conference on Power Systems, ICPS 2016*, 2016, doi: 10.1109/ICPES.2016.7584017.

[19] A. H. Ali Biglo, S. Farzamkia, S. Farhangi, and H. Iman-Eini, "Utilization of Soft-Switched Boost Converter for MPPT Application in Photovoltaic Single-Phase Grid-Connected Inverter," *2020 11th Power Electronics, Drive Systems, and Technologies Conference, PEDSTC 2020*, 2020, doi: 10.1109/PEDSTC49159.2020.9088432.

[20] L. Mitra and N. Swain, "Closed loop control of solar powered boost converter with PID controller," *2014 IEEE International Conference on Power Electronics, Drives and Energy Systems, PEDES 2014*, 2014, doi: 10.1109/PEDES.2014.7041973.

[21] H. Ardi, A. Ajami, and M. Sabahi, "A novel high step-up DC-DC converter with continuous input current integrating coupled inductor for renewable energy applications," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1306–1315, 2018, doi: 10.1109/TIE.2017.2733476.
[22] P. Wang, L. Zhou, Y. Zhang, J. Li, and M. Sumner, "Input-Parallel Output-Series DC-DC Boost Converter with a Wide Input Voltage Range, for Fuel Cell Vehicles," *IEEE Transactions on Vehicular Technology*, vol. 66, no. 9, pp. 7771–7781, 2017, doi: 10.1109/TVT.2017.2688324.
[23] M. Lakshmi and S. Hemamalini, "Nonisolated High Gain DC–DC Converter for DC Microgrids," *IEEE Transactions on Industrial Electronics*, vol. 65, no. 2, pp. 1205–1212, Feb. 2018, doi: 10.1109/TIE.2017.2733463.
[24] F. Ghasemi, M. R. Yazdani, and M. Delshad, "Step-Up DC-DC Switching Converter With Single Switch and Multi-Outputs Based on Luo Topology," *IEEE Access*, vol. 10, pp. 16871–16882, 2022, doi: 10.1109/ACCESS.2022.3150316.
[25] S. Yahyazadeh, M. Khaleghi, S. Farzamkia, and A. Khoshkbar-Sadigh, "A New Structure of Bidirectional DC-DC Converter for Electric Vehicle Applications," in *2020 11th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC)*, Feb. 2020, pp. 1–6. doi: 10.1109/PEDSTC49159.2020.9088414.
[26] D.-Y. Jung, S.-H. Hwang, Y.-H. Ji, J.-H. Lee, Y.-C. Jung, and C.-Y. Won, "Soft-Switching Bidirectional DC/DC Converter with a LC Series Resonant Circuit," *IEEE Transactions on Power Electronics*, vol. 28, no. 4, pp. 1680–1690, Apr. 2013, doi: 10.1109/TPEL.2012.2208765.
[27] T. Zhan, Y. Zhang, J. Nie, Y. Zhang, and Z. Zhao, "A Novel Soft-Switching Boost Converter With Magnetically Coupled Resonant Snubber," *IEEE Transactions on Power Electronics*, vol. 29, no. 11, pp. 5680–5687, Nov. 2014, doi: 10.1109/TPEL.2013.2295887.
[28] W. Yu *et al.*, "High efficiency converter with charge pump and coupled inductor for wide input photovoltaic AC module applications," *2009 IEEE Energy Conversion Congress and Exposition, ECCE 2009*, pp. 3895–3900, 2009, doi: 10.1109/ECCE.2009.5316154.
[29] W. Li, Y. Zhao, Y. Deng, and X. He, "Interleaved converter with voltage multiplier cell for high step-up and high-efficiency conversion," *IEEE Transactions on Power Electronics*, vol. 25, no. 9, pp. 2397–2408, 2010, doi: 10.1109/TPEL.2010.2048340.
[30] S. Saravanan and N. R. Babu, "Non-Isolated DC-DC Converter for Renewable Based Grid Application," *Energy Procedia*, vol. 103, pp. 310–315, 2016, doi: 10.1016/j.egypro.2016.11.291.

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