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Fault-tolerant single-input dual-output converter with preserved output under fault operation

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ABSTRACT

DC-DC converters have played an important role in the auxiliary power supply to electric vehicles, DC micro-grids, and portable electronic applications. To reduce the number of components and to improve the power density, multiport DC-DC converters have been recently proposed. Many multi-output converters are designed based on specific operational constraints on duty ratio or inductor currents. Further, simultaneous control of outputs is critical and involves cross-regulation issues. This paper proposes a single-input dual-output (SIDO) DC-DC converter with fault-tolerant circuit configuration to circumvent these challenges. The designed converter is helpful for the simultaneous control of loads by cross-regulation issues and has simple control without any control constraints on duty ratio or inductor currents. The topology proposed in this paper, can most significantly tolerate the failure during open-circuit for single and multiple switches and gives the preserved output voltage under fault case. The effectiveness and feasibility of the proposed configuration is validated using MATLAB/Simulink.

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1. INTRODUCTION

The DC-DC converters are the good choice for many portable applications. In the last decade, many topologies have been suggested in order to reduce the size, cost, control complexity and to improve the efficiency. Some popular converters capable of parallel operation of the loads among the existing literature [1]–[5] are based on the single inductor concept.

The current ripple-through inductor concept is used to analyze the converter, and the suggested method helps to predict the converter's steady state and dynamic performance [6]. Further, this modeling approach is able to resolve the possible extension output range and issue of cross-regulation, which are significant in single-input multi-output (SIMO) converter design. An effective extension and supplement of the SIMO converter for simultaneous buck-boost and inverted outputs modeling and analysis are presented in [7] to deal with the unanticipated mathematical problems in the SIMO converter suggested in [6], single inductor SIMO converters are derived using computer-aided systematic derivation [8]. It has a low part count and high-power density. A coupled inductor-based SIMO converter with lower output magnitudes is developed for integrated circuit power management [9]. Nayak and Nat [10] introduced the comparative performance of SIDO buck converters, which helps to understand the various converters. The word in [11] a buck-boost mode SIMO converter is proposed with two different control strategies for buck/boost modes to

handle the cross-regulation problem. It is used as the PWM modulator for buck mode operation to reduce the cross-regulation issues due to imperfect tracking of the inductor current. Another control strategy based on duty ratio and current predict control is suggested for the boost mode of operation. However, these methods are partially eliminated the cross-regulation issues and high control complexities for each mode of operation. Zhang *et al.* [12] proposed a SIMO converter with low hardware cost, less computational burden, and constant switching frequency as the objectives. This work suggests a deadbeat control to generate optimal duty ratios using online load current sensing.

Many other SIMO topologies are proposed in [13]–[22] for various applications. Recently, a generalization procedure has been suggested in [13] for generating 4, 6, 8, and 12 outputs using a single voltage source and a single power semiconductor device without a transformer. The converters are combinations of SEPIC, boost, ćuk, and four-phase interleaved ćuk and SEPIC circuit configurations. A SIDO DC-DC buck converter configuration is designed in [14]. It is helpful for bidirectional and unidirectional applications. It is developed with a reduced part count, better power loss sharing among the devices, and lower hardware cost. However, this topology has a control constraint that is one inductor must be charged before the other inductor (i.e., $V_{o1} >= V_{o2}$). And, this approach influences the output voltages during the control of loads. An Integrated DC-DC converter with dual outputs configuration is suggested in [15]. Furthermore, the synthesized topology of each node has emerged as buck voltage in addition to one boost voltage output. However, the control of this circuit is somewhat complex and is based on the time-sharing concept while regulating the individual outputs. Hence the input source and components are underutilized.

Chen *et al.* [16] developed a circuit arrangement using a synchronous buck converter with multiple outputs for power supply of electrical vehicle. It has reduced the switching elements. However, the control methodology of the SIMO converter depends on a constraint such that the current through one inductor should be greater than another inductor (i.e., $i_{L1} > i_{L2}$). This control burden on the power converter has become a significant limitation in regulating the individual outputs of the SIMO converter. Super-lift LUO and buck converter are interfaced to develop the SIDO converter [17]. It can generate both boost and buck output voltages. However, it has an operational constraint, $d_2<d_1$ limited the operating range of d_1 when $d_2$increased.The converter SIDO developed in [18] can generate SIDO and dual input-single output for various practical applications. However, the issues of cross-regulation and appropriate control action for mitigating them are not addressed in this work. Three-output single-input SIMO topology is designed in [19] with low voltage stress and high voltage gain without using coupled inductors and transformers. A three-level SIDO DC converter is developed in [20], capable of simultaneously regulating the boost and buck voltages.

A switched capacitor-based SIMO converter employing differential buck converters for achieving smaller volume and higher efficiency is designed in [21]. This approach has better efficiency than conventional parallel connected buck-converters and switched capacitor-based multiple output converters. However, the circuit topology has more switched capacitors which create a sharp reduction in efficiency, and the operation of the converter requires a complex control strategy to minimize the cross-regulation issues. A SIMO converter with high gain DC output magnitudes using interleaved concept and SEPIC topology is proposed in [22] using coupled inductors and voltage multiplier technique. However, the developed converter in [22] has more numbers of devices and magnetic components in addition to high control complexity. A converter with multiple outputs for multiple loads based on interleaved with four phases is proposed in [23] for bipolar DC micro-grids. This interleaved multiphase converter is helpful for higher voltage and current applications. However, the circuit has more components, and its continuous conduction operation has a mathematical constraint on duty ratio while regulating the output voltage. A systematic approach to deriving switch fault-tolerant step-down dc-dc converter is presented in [24], [25]. It is referred to open circuit switch fault due to power switch fault.

In this paper, the proposed SIDO topology can generate two different output voltages to regulate the different voltages levels. The major advantage of the topology is fault-tolerant on single and multiple switches, and loads are isolated during control, which leads to output voltages not being influenced by each other. The remaining parts of the paper are arranged as follows: proposed SIDO topology and operating modes are described in section 2. Semiconductor stress analysis, details of parameter design, analysis of power loss, fault-diagnostic methodology, and comparative assessment are dealt in section 3. Results and discussions are presented in section 4. Section 5 outlines the conclusions.

2. SIDO TOPOLOGY AND MODES OF OPERATION

The faulty tolerant SIDO configuration is introduced in this manuscript, shown in Figure 1. The components used in this topology: S_1-S_3 are power switches; the input source is the V_{DC}; L_1-C_1 and L_2-C_2 are filter elements. R_1 and R_2 are loads, and D_1-D_3 are diodes. It develops two different output voltages, one is boosting voltage (V_{01}) and the other one is buck-boost voltage (V_{02}). More significantly, the proposed circuit

topology has single and multiple switch failure tolerance and preserved the output voltages under the open circuit fault conditions. The proposed topology has the following benefits:

- No operational constraints on duty ratio like $d_1 < d_2$ or $d_1 = d_2$ etc.,
- Allows simultaneous and individual control of loads
- No control constraints on inductor currents like $i_{L1} > i_{L2}$ or $i_{L1} < i_{L2}$ or $i_{L1} = i_{L2}$
- It has fault tolerance with single and multiple switch failures and continues to operate as SIDO, delivering the preserved output voltage.
- It gives buck-boost operation with positive output polarity without requiring an additional inverting circuit
- The cross-regulation issue in multioutput converters is successfully eliminated

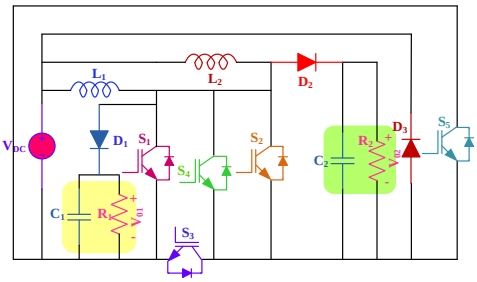


Figure 1. Schematic of proposed fault-tolerant SIDO configuration

The areas of application of this converter include DC nano-grids and solar battery chargers. Low outputs are essential in EVs' auxiliary power system application. Hence, this configuration is more suitable for getting low output (buck-boost) than the input voltage, and the remaining output (boost) is utilized in EV chargers.

2.1. Operating modes

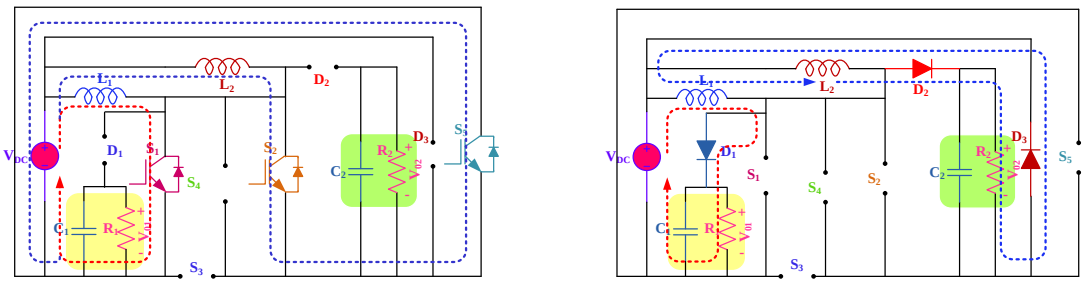
- Switching state 1:

The circuit model of the converter for the switching state 1 is is shown in Figure 2(a). During this state, the S_1, S_2, and S_5 are ON. The input source magnetizes L_1 and L_2.

- Switching state 2:

Figure 2(b) shows the circuit model of the converter during this state. It is observed that the D_1, D_2, and D_3 are forward-biased. The stored energy in the inductors is delivered to the loads.

$$V_{01} = \frac{V_{DC}}{(1-d_1)}, V_{02} = \frac{d_2 V_{DC}}{(1-d_2)} \quad (1)$$



(a) (b)

Figure 2. Switching states: (a) mode 1 and (b) mode 2

From these modes of operation and their circuit models, it is observed that the loads are isolated from each other. Therefore, a change in one load will have no effect on the other load. Mainly, cross-regulation

issues are removed, and the circuit model facilitates that the energy stored in one inductor is restricted Toone specific output. Therefore, the converter enables the independent operation and control of loads.

2.2. Operation of the redundant switches under fault-tolerant case

An undesired open circuit of the switch is considered as switch fault. In the proposed converter, different possible open circuit faults are presumed. The faults are isolated, and the converter is continued to supply power to the connected loads. In other words, even under switch fault conditions, the proposed configuration continue to operate as a SIDO converter, generating preserved output, i.e., boost and buck-boost outputs.

In order to achieve the fault tolerance under switch faults, redundant switches of S_4 and S_5 are added to the designed SIDO converter, as shown in Figure 2(b). These features facilitate the converter to generate equal voltages during pre- and post-fault conditions. Different switch failure cases and the corresponding conducting switches are presented in Table 1 for preserved output voltages.

Table 1. Control of the switches under switch fault condition

Fault on switch	Redundant switching Paths for V_{01}		Redundant switching Paths for V_{02}		Output voltage (V_{01})	Output voltage (V_{02})
	Mode 1	Mode 2	Mode 1	Mode 2		
S_1	S_2, S_3	D_1	S_2, S_3	D_2, D_3	Boost	Buck-Boost
S_2	S_1	D_1	S_1	D_2, D_3	Boost	Buck-Boost
S_3	S_1	D_1	S_2, S_5	D_2, D_3	Boost	Buck-Boost
S_1, S_2	S_3, S_4	D_1	S_3, S_4	D_2, D_3	Boost	Buck-Boost
S_1, S_3	S_2, S_5	D_1	S_2, S_5	D_2, D_3	Boost	Buck-Boost
S_2, S_3	S_4, S_5	D_1	S_4, S_5	D_2, D_3	Boost	Buck-Boost
S_1, S_2, S_3	S_4, S_5	D_1	S_4, S_5	D_2, D_3	Boost	Buck-Boost

3. ANALYSIS OF STRESS, DESIGN OF PARAMETERS, FAULT DIAGNOSTIC METHODOLOGY, CALCULATION OF POWER LOSS, AND COMPARATIVE ASSESSMENT

3.1. Analysis of stress

The analysis of voltage stress [26] for the proposed converter is given in (2). The analysis for the current stress for the mode 1 is given in (3). For the mode 2, the current stress analysis is given in (4).

$$V_{S_1} = V_{S_4} = V_{01}, V_{D_1} = V_{01}$$
$$V_{S_2} = V_{S_3} = V_{S_5} = \left(\frac{V_{DC}+V_{02}}{2}\right)$$
$$V_{D_2} = V_{D_3} = (V_{DC} + V_{02}) \quad (2)$$

$$i_{S_1} = i_{L_1}, i_{S_2} = i_{S_5} = i_{L_2}$$
$$i_{S_3} = i_{S4} = i_{D_1} = i_{D_2} = i_{D_3} = 0 \quad (3)$$

$$i_{S_1} = i_{S_2} = i_{S_3} = i_{S_4} = i_{S_5} = 0$$
$$i_{D_1} = i_{L_1}, i_{D_2} = i_{D_3} = i_{L_2} \quad (4)$$

Where, $V_{S1\text{-}5}$ and $i_{S1\text{-}5}$ are the voltage and current stress of the switches (S_1-S_5), respectively. $V_{D1\text{-}3}$ and $i_{D1\text{-}3}$ are the voltage and current stress of the diodes (D_1-D_3), respectively.

3.2. Parameter design

The calculation of minimum inductance is presented in (5). The inductance ripple current is given in (6). The design of capacitance is given in (7). The design of the parameters for this converter is derived based on the literature[26]. The specifications of the parameter are presented in Table 2.

Calculation of minimum inductance:

$$L_{1min} = \frac{2}{27}\frac{R_{L1max}}{f_s}, L_{2min} = \frac{R_{L2max}(1-d_{min})}{2f} \quad (5)$$

where f_s and d_{min} are switching frequency and minimum value duty ratio. R_{L1max} and R_{L2max} are the maximum resistances of load-1 and load-2, respectively.

The inductor ripple current is (6).

$$\Delta i_{L_1 max} = \frac{V_{01} d_{min}(1-d_{min})}{f_s L_1}, \Delta i_{L_2 max} = \frac{V_{02}(1-d_{min})}{f_s L_2} \quad (6)$$

The design of capacitance is (7).

$$C_{1min} = \frac{d_{max}V_{01}}{V_{cpp}R_{L1max}f_s}, C_{2min} = \frac{d_{max}}{2r_cf_s}, V_{cpp} = \frac{V_r}{2} \quad (7)$$

Where d_{max} = maximum duty ratio, V_{cpp} = peak-to-peak ripple voltage, and r_C is the ESR of the filter capacitor.

Table 2. Parameter specifications

Parameter	Simulation
Input voltage	(V_{DC}): 50 V
Voltage outputs	(V_{01}/V_{02}): 100/50 V
Current outputs	(I_{01}/I_{02}): 2.5/1.5 A
Switching frequency	50 kHz
Inductors	(L_1/L_2): 0.9/1.5 mH
Capacitors	(C_1/C_2): 200/360 uF

3.3. Fault-diagnostic and control methodology

The fault diagnosis and control flow chart are given in Figure 3. Here, the currents i_{L1}, and i_{L2} are measured using the sensors and proceed for the fault diagnosis. If any absolute current value is zero, there is an open switch fault condition. The fault diagnosis is made by sensing the currents (i_{L1}, i_{L2}). Initially, the faults are labeled as F_1 when S_1 failed and similarly F_2 for switch faults of S_2 or S_3. After fault diagnosis, the controls of power switches are done accordingly, as described in Table 1.

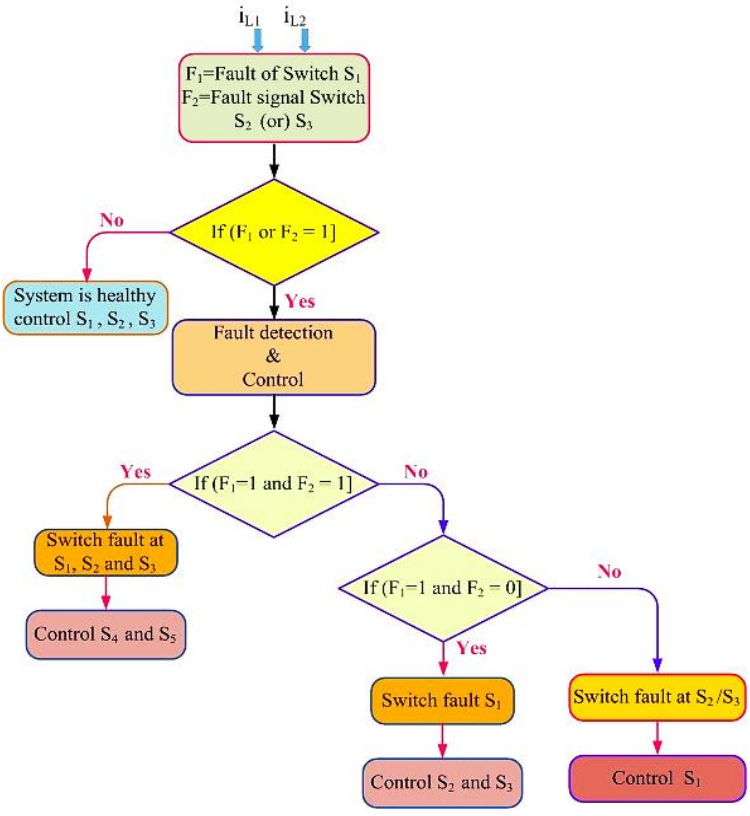


Figure 3. Flow chat for switch fault detection and control

3.4. Calculation of losses

The power losses motioned in [27] determine the efficiency of converter operation. The power loss is presented in (8). The conduction loss (P_c) of IGBT is given in (9). The switching losses (P_s) are calculated using (10). The efficiency is obtained using (11).

$$P_{loss\_IGBT} = P_c + P_s \quad (8)$$

$$P_c = \frac{1}{T}\int_0^T (R_{on} i_F + V_{Fo}) i_F dt \quad (9)$$

$$P_s = (E_{OFF,j} + E_{ON,j}) \times f \quad (10)$$

$$\eta = \frac{P_o}{P_o + P_s + P_c} \quad (11)$$

P_o is the converter output power.

3.5. Performance analysis and comparative assessment

Table 3 and Table 4 (see appendix) present the comparison of performance of the proposed converter and the SIMO topologies developed in the literature. At different duty ratio sets, the proposed structure is tested, and the corresponding plots are presented in Figure 4. From Figure 4(a) and Figure (b), it is noticed that, the proposed converter can generate different outputs voltage and outputs are independently regulate without duty cycle constraint. In addition, the output voltages are not affected regardless of the load variations. As a result, during the control of the converter the cross-regulation issue does not occur.

Table 3. Proposed converter comparison with the different SIMO topologies

Ref.	Control constraint	During control the loads are isolated from each other	Switch fault-tolerant
[13]	V_{01}, and V_{02}, may not control independently	No	No
[16]	$i_{L_1} > i_{L_2}$	No	No
[17]	$D_2 < D_1$	No	No
[20]	-	No	No
[21]	-	No	No
Pro.	No control constraints	Yes	Yes

Table 4. Performance comparison of different SIMO topologies

Ref.	G_{port}	$S_{V\_Stress}/S_{I\_Stress}$	$D_{V\ Stress}/D_{V\ Stress}$	N_S	N_D	N_L	N_C	$N_{component}$	N_{input}	N_{output}
[13]	$V_{01} = \frac{D}{(1-D)}$, $V_{02} = \frac{1}{(1-D)}$ $D < 1$	$V_{Smax} = V_{02}$ $i_S = i_{L_1}$	$V_{D_1} = V_g + V_{01}$ $V_{D_2} = V_{02}$ $i_{D_1} = i_{L_2}, i_{D_2} = i_{L_1}$	1	2	2	3	8	1	2
[16]	$V_{01} = D_1 V_i, V_{02} = D_2 V_i$ $D_1 + D_2 < 1$	$V_{Smax} = V_i, V_{S_{0-2}} = V_i$ $i_{S_0} = i_{L_1} + i_{L_2}$ $i_{S_1} = i_{L_2} - 2i_{L_1}$ $i_{S_2} = i_{L_1} - 2i_{L_2}$		3	-	2	2	7	1	2
[17]	$V_{01} = D_1 V_{in}$ $V_{02} = (D_2 - D_1) V_b$ $D < 1$	$V_{Smax} = V_{in}$	$V_{Dmax} = V_{in}$	3	3	1	3	10	1	2
[20]	$v_{01} = \frac{v_{in}}{(2-d_1-d_2)}$, $v_{02} = \frac{v_{in}(1-d_2)}{(2-d_1-d_2)}$ $0.5 < d_1 \& d_2 < 1$	$V_{Smax} = \frac{V_{01}}{2}$ $V_{S_{1-6}} = \frac{V_{01}}{2}$ $i_{Smax} = i_{L_1}$	-	6	-	2	3	11	1	2
[21]	$V_{01} = \frac{2+D}{3}$, $V_{02} = \frac{1+D}{3}, V_{03} = \frac{D}{3}$ $0 < D < 1$	$V_{Smax} = V_{01}$ $i_{Smax} = i_{L_1}$	-	12	-	3	8	23	1	3
Proposed	$V_{01} = \frac{V_{DC}}{(1-d_1)}$, $V_{02} = \frac{d_2 V_{DC}}{(1-d_2)}$ $0 < d_1 < 1, 0 < d_2 < 1$	$V_{Smax} = V_{01}$ $V_{S_1} = V_{S_4} = V_{01}$, $V_{S_{2-5}} = \left(\frac{V_{DC}+V_{02}}{2}\right)$, $i_{S_1} = i_{L_1}, i_{S_{2,3}} = i_{L_2}$	$V_{D_1} = V_{01}$ $V_{D_{2,3}} = (V_{DC} + V_{02})$ $i_{D_1} = i_{L_1}, i_{D_2} = i_{L_2}$	5	3	2	2	12	1	2

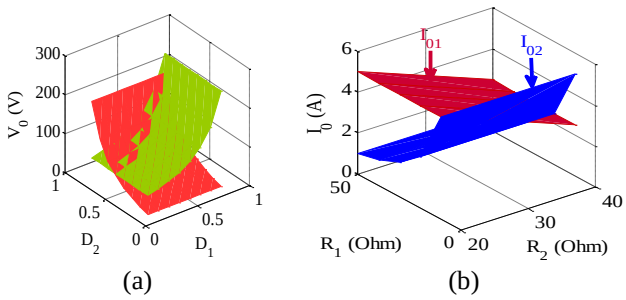


Figure 4. Variation of output voltage: (a) output voltage vs. duty cycle, and (b) load current vs. load

4. SIMULATIONRESULTS AND DISCUSSIONS

4.1. Simulation verification

The configuration proposed in this paper is tested in MATLAB/Simulink. Table 4 presents the details of the parameters. It is tested at an input voltage of 50 V (V_{DC}), switching frequency is 50 kHz and the duty cycle is (50%). In the simulation, the converter is operated at healthy switches. The corresponding V_{01}, $i_{L1,}$ V_{02} and i_{L2} are shown in Figures 5(a)-5(d) respectively. The V_{01} and V_{02} in Figure 5(a) and Figure 5(c) are similar to the theoretical results, i.e., (1). This converter is tested in transient case, i.e., changing in load, whose results are presented in Figure 6. Figure 6(a) and Figure 6(b) depicts the output voltages in the case of a sudden change in ±30% of the load. Figure 6 shows an excellent dynamic response in a load variation. The proposed configuration is tested in a switch fault (S_1, S_2, and S_3).

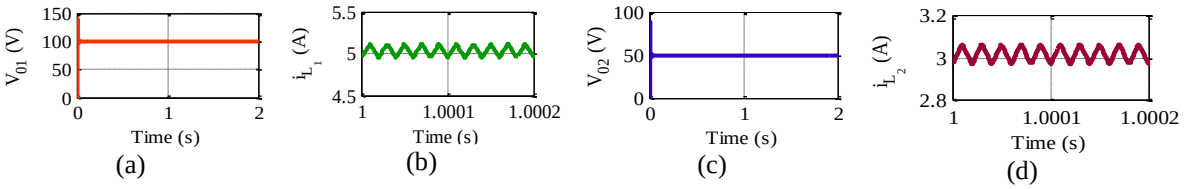


Figure 5. Simulation results in healthy case: (a) V_{01}, (b) i_{L1}, (c) V_{02}, (d) i_{L2}

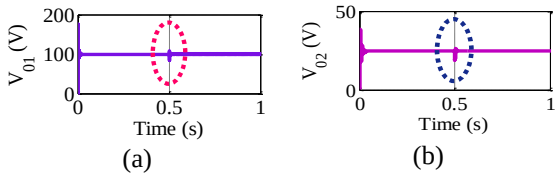


Figure 6. Simulation results at load variation: (a) V_{01}, (b) V_{02}

- Case 1: Fault tolerance during the main switch S_1 failed

This fault tolerance capability of the converter is described using the simulation results shown in Figure 7, Figure 8 and Figure 9. The Figure 7 shows the dual output voltages of the converter. The corresponding gate pulses during the healthy case (from t = 0 to 1 sec) and also in the case of S_1 failed. Exactly at t = 1, the switch fault at S_1 is initiated, and the control strategy is applied as described in Table 1. During the healthy condition, the main switches S_1 and S_2 are controlled, whereas the switches S_2 and S_3 are controlled during the switch fault at S_1. It is observed that during this switch failure also, the converter has preserved output voltage. That means the magnitude of the output voltage, V_{01} is 100 V during healthy and post-fault conditions. Similarly, the magnitude of the output voltage at another load, V_{02}, is also preserved at 50V at the set duty ratio of 0.5.

- Case 2: Fault tolerance during the main switch S_2 failed

Now fault at switch S_2 is considered. The corresponding gate pulses and output voltages are shown in Figure 8. The control strategy to achieve the fault tolerance is described in Table 1and the implementation algorithm is presented in Figure 3. However, Figure 8 shows healthy operation till 1 second, and the fault is initiated at t = 1 sec. One may observe that there are no changes in the magnitudes of the output voltages during a post-fault condition.

- Case 3: Fault tolerance during the multiple switch failures

The multiple switch faults are a lesser chance in real-time operation. However, they are also considered to improve the continuity of operation of the converter. In the proposed converter, the possible multiple faults such as failure of S_1 and S_2 and also the failure of all main power switches S_1, S_2, and S_3 are considered as shown in Figure 9. In this case till t = 1 sec, healthy condition, multiple failures of switches (S_1, S_2) are initiated at t = 1 sec and failure of all the main switches (S_1, S_2, S_3) is initiated at t = 2 sec. The control operation for fault tolerance is followed as shown in Table 1. The proposed converter efficiency, power loss distribution losses of the power devices in healthy and fault cases are illustrated in Figures 10(a)-10(c) respectively.

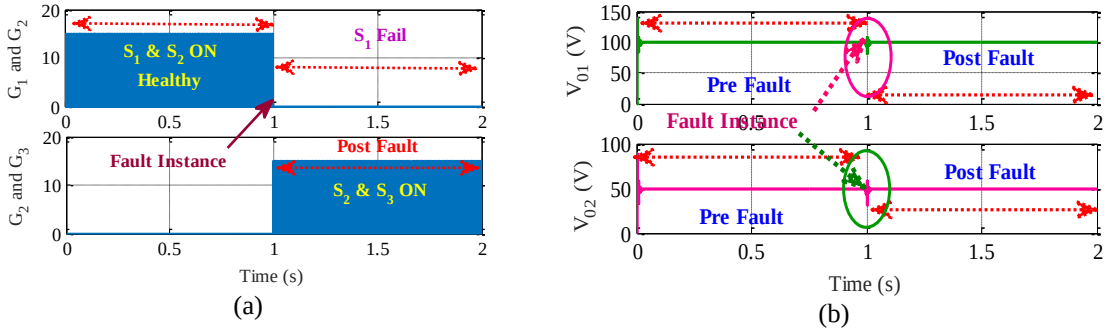


Figure 7. Gate pulses for switches and output voltage during S_1 failure case

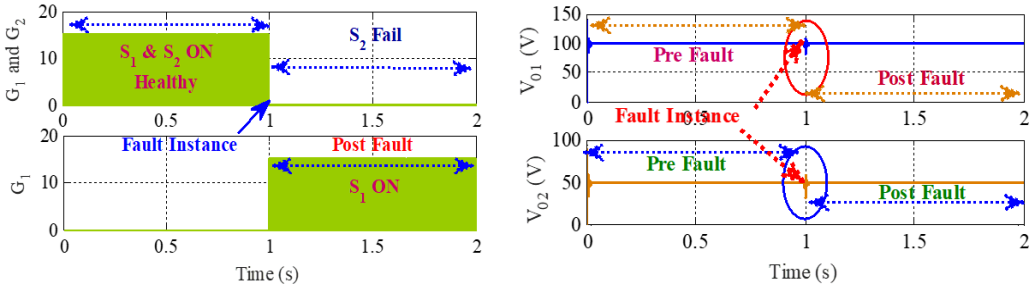


Figure 8. Simulation gate pulses for switches and output voltage during S_2 failure case

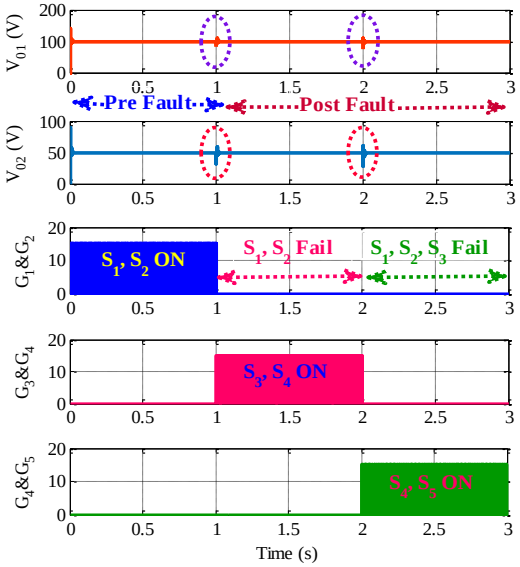
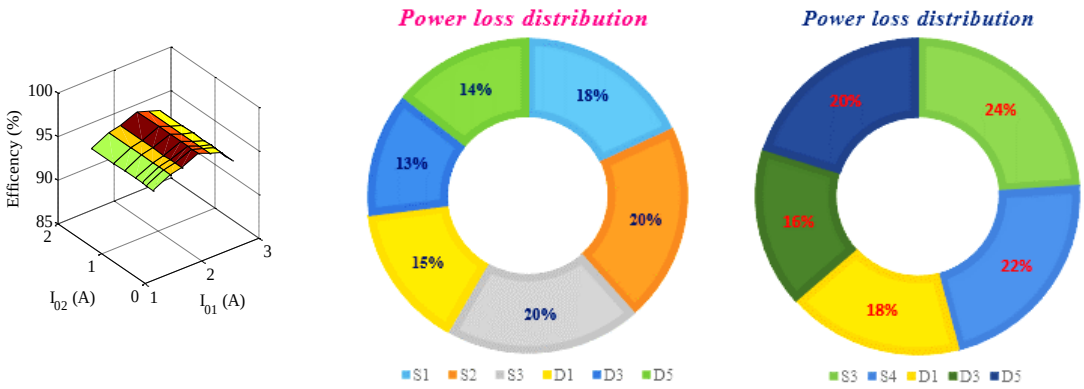


Figure 9. Simulation results during multiple switch faults (both S_1 and S_2 fail at t = 1 sec, and all S_1, S_2, and S_3 failed at t = 2 sec)



(a) (b) (c)

Figure 10. Performance of the converter (a) efficiency, (b) power loss distribution of the switches and diodes in healthy case, and (c) power loss distribution of the switches and diodes in switch fault case

5. CONCLUSION

The proposed SIDO converter is analyzed in this paper. The highlight of this configuration is that it is free from any assumption on operating duty cycle ($d_1>d_2$ or $d_1=d_2$ or $d_1<d_2$) and inductor charging currents ($i_{L1}> i_{L2}>$ or $i_{L1}< i_{L2}$). The proposed configuration's working principle and operating modes are also described in detail in this paper. Its ability to generate different output voltages without stated assumptions has been well established with simulation verifications. The illustrated results, such as output voltages not getting influenced by the variation of inductor current and load current, supported the claim to eliminate the cross-regulation problem. More significantly, it has switch fault-tolerant capability under single and multiple switch failures. The proposed fault-diagnostic methodology is verified and validated with simulation results.

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