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A multilevel boost inverter with removed leakage current and a reduced number of elements for photovoltaic applications

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ABSTRACT

Recent research has concerted on transformer-less multilevel inverters (TL-MLIs) due to their high-voltage or high-power capacity for converting the low-voltage output of renewable energy sources to the desired output. Moreover, they yield higher efficiency, lower cost and size than the conventional type. However, these inverters usually suffer from leakage current. The proposed inverter attempts to accommodate this concern to the greatest extent feasible. The proposed inverter structure exhibits a common ground between the input and output ports. Due to this, the total common mode voltage (CMV) is constant. The photovoltaic (PV) source to the grid parasitic capacitor is short-circuited due to this common ground feature, which results in negligible leakage current. The proposed inverter also features a boosting output voltage using only a single voltage source with minimum power devices. The number of output levels can be increased with the modular application of the proposed inverter. Finally, the mathematical analysis for the proposed inverter has been accomplished, and the MATLAB/Simulink simulation results are presented. Also, the results show the output voltage boost capability, zero leakage current, and suitable total harmonic distortion for output voltage and current waveforms.

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1. INTRODUCTION

In recent decades, renewable energy sources, especially PV, have received more attention due to evolving critical issues such as global warming and environmental pollution. Various converters with diverse structures have been presented for renewable energy resources [1]–[4]. Various research has been conducted in multilevel converters design, including for solar-based applications in [5]–[13]. This paper discusses in the new inverter topologies, modulation methods, maximum power point tracking systems and special conditions for PVs and the corresponding solutions. Also, developing of the inverters with low leakage current is the main objective of these topologies.

Switched capacitors (SC) or switched inductors (SI) inverters are recently developed to obtain higher voltage gain at the inverter output. This feature allows the inverter to step-up the low input voltage source to the desired output voltage for grid-connected applications. Recently, some research has been conducted to use switched capacitors in the structure of neutral point clamped (NPC)-based inverters to increase the voltage

gain [14]–[22]. In these converters, the switched capacitors are discharged in series with the DC link capacitor to obtain a higher output voltage.

The problem in most of these NPC types of inverters is the existence of current spikes while charging the capacitors. So, in order to resolve this issue, the papers in [23], [24] are proposed. These papers propose new active NPC based structures with voltage-boosting capability. However, the maximum voltage gain is increased up to twice of the input voltage value.

Several studies in [25]–[29] propose the dual mode time-sharing method to prevent additional losses in two-stage transformer-less inverters. In this method, the boost stage only works when the PV voltage is lower than the grid voltage. Pourfaraj *et al*. [25] and Kakar *et al.* [26] provided a dual-mode transformer-less interleaved multilevel inverter with an interleaved boost converter. The main contribution of this inverters is lower current stress across semiconductors and DC-side inductors. Also, the main limitation is the necessity of a comparatively higher number of semiconductors and the presence of high-frequency components on the common mode voltage (CMV). The fault tolerant (FT) capability is one of the important features of the multilevel inverters to keep supplying the output load in various fault conditions in order to increase the reliability of the inverter. Heydari-Doostabad *et al.* [27] proposed a single-phase PV inverter with a common ground and three switches provides reactive electricity to the AC grid. The inverter benefits step-down and step-up for output voltage, regulate active and reactive power, and have low. Anand *et al.* [28] proposed a 5-level common ground type (5L-CGT) inverter with double voltage amplification. However, this inverter is incapable of boost operation with variable duty cycle. Wang and Shan [29] presented a single-stage common-ground zeta inverter with a non-electrolytic capacitor. This inverter addresses common mode (CM) leakage current, voltage step-up/step-down, and electrolytic capacitor lifetime concerns.

In conclusion, propose of a multilevel structure, with eliminated common mode voltage (CMV), zero leakage current and fault tolerant capable inverter with boost voltage gain feature seems necessary to obtain a safe and reliable inverter which is suitable for low-voltage renewable applications. The aim of this paper is to propose a novel 5-level boost inverter with continuous gain control capability. An inductor supplies the input side of the proposed inverter, so a continuous input current has been provided to the input source, making the inverter suitable for PV or other renewable energy applications involving DC/AC operation. In addition, the enhanced levels of the inverter for a 7-level operation have been provided to demonstrate the inverter's modularity. Furthermore, the number of components is low, and the leakage current is close to zero because the negative end of the power source is connected via wires in a direct connection to the grid's neutral terminal. The paper is organized as follows: the structure of proposed 5-level multilevel fault-tolerant boost inverter in section 2. The methodology and switches pulses generation scheme in section 3. MATLAB/Simulink results for inverter in section 4. And finally, conclusion is presented in section 5.

2. PROPOSED MLI STRUCTURE

This section discusses the proposed 5-level inverter with exceptional advantages. The proposed 5-level circuit is shown in Figure 1. In the proposed structure a boost inductor is used in the design to provide continuous input current and to facilitate controllable voltage gain. The converter with the appropriate specifications for PV applications is developed using a single DC source. In addition, the inverter is capable of modular operation and incorporates fewer switches. The proposed inverter has a significantly high boost gain, and the peak output voltage for 5-level and 7-level output voltage levels can be calculated as $\frac{2M}{1-D}$ and $\frac{3M}{1-D}$, respectively.

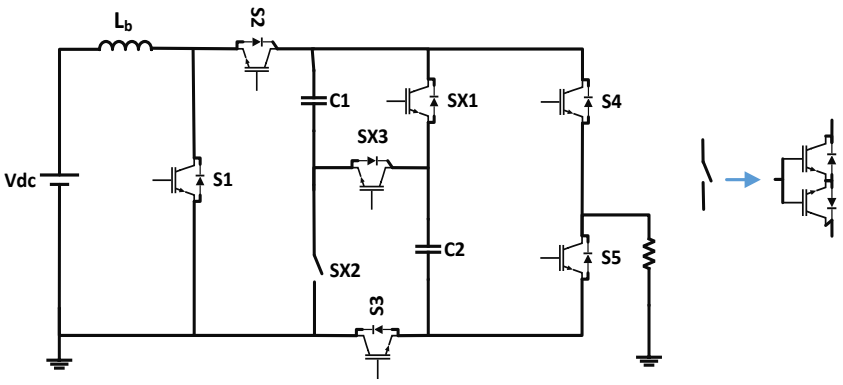


Figure 1. The proposed 5-level inverter structure

2.1. Operating modes

In this part, the proposed 5-level converter's main operating modes have been depicted in Figures 2(a) to 2(o) see in (Appendix), which provide replacement working modes for each voltage stage to maintain the output voltage at fault conditions. Each stage of operation includes both the charging and discharging stages of the input boost inductor. Furthermore, the implementation includes a number of charging and discharging states for different levels of inverter output. This feature also offers advantages such as capacitor voltage balancing and simplified control of the boost duty cycle. Moreover, the input inductor in this inverter is charged when the IGBT S_1 is ON, and it is discharged when the power switch S_1 is off. So, the key waveforms of the proposed inverter have been demonstrated in Figure 2(p) see in (Appendix).

2.2. Essential mathematical calculations

The proposed inverter uses a specific approach to obtain modulation index values between zero and maximum. The maximum DC gain can be expressed as (1).

$$Gi = \frac{2M}{1-D} \tag{1}$$

In the proposed inverter, the capacitors have been charged to the same value, and the corresponding voltage of each capacitor can be obtained as (2).

$$V_{C1} = V_{C2} = \frac{V_{DC}}{1-D} \tag{2}$$

Consequently, the maximum peak voltage is equivalent to the summation of the voltages present on mentioned capacitors. Therefore, it can be obtained as (3).

$$V_{O,Max} = \frac{2V_{DC}}{1-D} \tag{3}$$

The equations in Table 1 illustrates the association between the output voltage and modulation index. The output voltage peak value can be changed by the duty-cycle (D) variations. Table 2 demonstrates the peak output voltage value variations. For the modulation indexes higher than 0.5, due to the level shift PWM (LS-PWM) strategy employed, the inverter output will have a 5-level waveform based on a sinusoidal reference voltage signal. Also, for M<0.5, the converter output will be changed to 3-level.

Table 1. The relationship among the modulation index and the output voltage

Output voltage	Modulation index range	Output voltage range
$V_O = \frac{2MV_{DC}}{1-D}$	0 to 1	$V_O => 0 \quad to \quad \frac{2V_{DC}}{1-D}$

Table 2. Application of the proposed method and the resulting output voltage gain for different modulation index ranges

Modulation index	Possible output levels	Output voltage peak gain
M>0.5	5 Levels	$\frac{V_{O,peak}}{V_{DC}} = \frac{2}{1-D}$
M<0.5	3 Levels	$\frac{V_{O,peak}}{V_{DC}} = \frac{1}{1-D}$

2.3. Design considerations

The proposed inverter design considerations for the power switches, input boost inductor and capacitors are presented in this section. Equations representing the voltage stress of the power switches are obtained, as presented in (4)-(6).

$$V_{Sx1,Sx2} = \frac{1}{1-D}V_{DC}, V_{S1,2,3,4,5,Sx3} = \frac{2}{1-D}V_{DC} \tag{4}$$

Also, the input boost inductor can be designed by the (5).

$$L_{in} \geq \frac{DV_{DC}}{f_s \Delta i_L} \tag{5}$$

Moreover, the inverter capacitors values can be defined as (6).

$$C_{1,2,\dots n} \geq \frac{D(1-D)I_O G}{f_s \Delta V_C} \quad (6)$$

3. METHODOLOGY

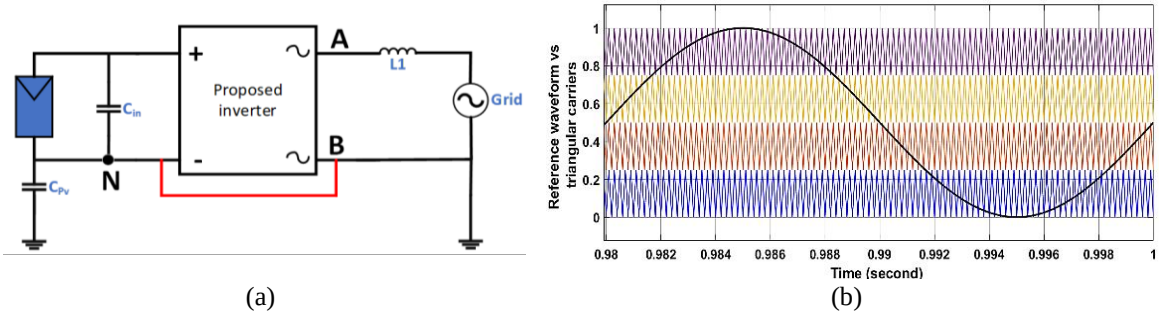
The proposed inverter structure provides a common ground between the output and input sides, which results in a zero CMV and removes leakage current for PV to grid applications. According to Figure 3(a), it can be found that the voltage from point B to the neutral point N (V_{BN}=0) is equal to zero. So, by considering this figure, the total common mode voltage of the inverter can be written as (7):

$$V_{CM.Total} = \frac{V_{AN}}{2} + (V_{AN})\left(\frac{-L_1}{2(L_1)}\right) = 0 \quad (7)$$

Which, the total CMV is equal to zero. Also, according to Figure 3(a), the parasitic capacitor of the PV (C_{PV}) is short-circuited. As a result, the leakage current through C_{PV} is also zero. Furthermore, the proposed inverter has the capability of continuous boost operation, which allows the inverter to obtain a wider output voltage range for lower input voltage sources.

3.1. Modulation and switching rules

The proposed structure uses the level shift modulation method to drive the IGBTs and get the sinusoidal waveform at the output. The waveforms of the carrier signal compared to the reference sinusoidal waveform are shown in Figure 3(b). For a 5-level inverter, there will be four triangular carrier waveforms. For each voltage state, there is at least one scenario for inverter switching. For this reason, the switching table for the proposed inverter, considering five levels from -2 V to +2 V, is described in Table 3. The variety of switching schemes for each voltage state makes the converter flexible for fault-tolerant applications.



(a) (b)

Figure 3. The proposed inverter connection to grid and modulation scheme: (a) the general schematic of proposed inverter connection to the AC grid and (b) the waveform of the triangular carrier signals in comparison with the reference sinusoidal waveform of the proposed inverter

Table 3. The switching conditions for the proposed 5-level inverter

Level	Inductor state	Switching condition	Power switches							
			S1	S2	S3	S4	S5	Sx1	Sx2	Sx3
+2V	Charge	CN1	1	0	1	1	0	0	0	1
	Discharge	CN2	0	1	1	1	0	0	0	1
+1V	Charge	CN3	1	0	1	1	0	1	0	0
		CN4	1	0	1	1	0	1	1	0
		CN5	1	0	0	1	0	0	1	0
	Discharge	CN6	0	1	1	1	0	1	0	0
		CN7	0	1	1	1	0	1	1	0
		CN8	0	1	0	1	0	0	1	0
0	Charge	CN9	1	0	1	0	1	1	1	0
	Discharge	CN10	0	1	1	0	1	1	1	0
	Discharge	CN11	0	1	1	0	1	0	0	0
-1V	Charge	CN12	1	1	0	0	1	1	0	0
		CN13	1	0	0	0	1	0	1	1
	Discharge	CN14	0	1	0	0	1	0	1	1
-2V	Charge	CN15	1	1	0	0	1	0	0	1

3.2. Modular operation of the inverter

The other feature of the proposed inverter is the modular operation capability. This characteristic increases the number of output voltage levels and the peak voltage enhancement of the inverter. In this part, the 7-level structure topology derived from the proposed circuit is illustrated in Figure 4.

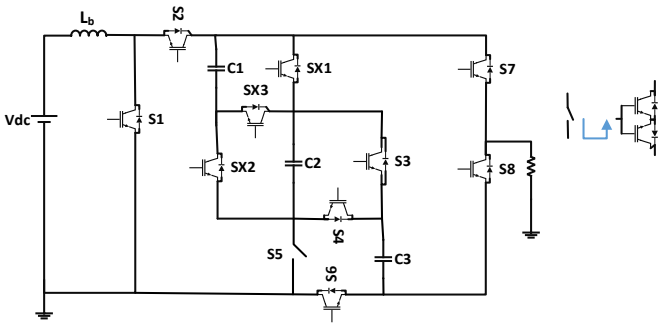


Figure 4. The 7-level structure topology based on the proposed circuit

4. RESULTS AND DISCUSSION

In accordance with the preceding portions, the proposed inverter can have a continuous boost mode, a continuous input current, a common ground mode with zero leakage current, and a 5-level output voltage for the output load. In this section, the key MATLAB/Simulink software results are presented, and the feasibility of the converter is confirmed. Also, the detailed loss analysis result from the PLECS software simulation has been added to the results to show the percentage of the losses per component of the inverter. Table 4 shows the key parameter values used for the inverter throughout simulation. Finally, a comparison between the proposed inverter and other structures is given in Table 5. As shown in Figure 5, by considering the parameter values in Table 4, the output 5-Level voltage is illustrated in Figure 5(a) with a peak value of 240 V which agrees with the equations in Table 2.

In order to show the continuous voltage variations with duty-cycle changes, the output voltage has been illustrated in Figure 5(b). In this figure, the duty cycle has been changed from D=80% to D=20% with 10% steps. This is one of the merits of the proposed inverter, which can control the output voltage's peak value in the extended operation area. Moreover, in Figure 5(c), the value of the modulation index has been changed from 0 to its maximum value (M=1). As can be seen, the inverter produces a 3-level output voltage for M<0.5, whereas for M>0.5 the inverter output voltage waveform is 5-level which agrees with Table 2. Furthermore, the voltage waveforms of the inverter capacitors (C_1 & C_2) are illustrated in Figure 6(a) and Figure 6(b), respectively.

Table 4. The key parameter values for the proposed inverter simulation

Parameter	Value	Parameter	Value
Input voltage (V_{dc})	24 V	Input inductor (L_b)	3 mH
Capacitor values (C_1 and C_2)	1200µF	Output load	100 Ω + 10 mH
Switching frequency	10 kHz	PWM	Level shift PWM
Modulation Index (M)	1	D	80%

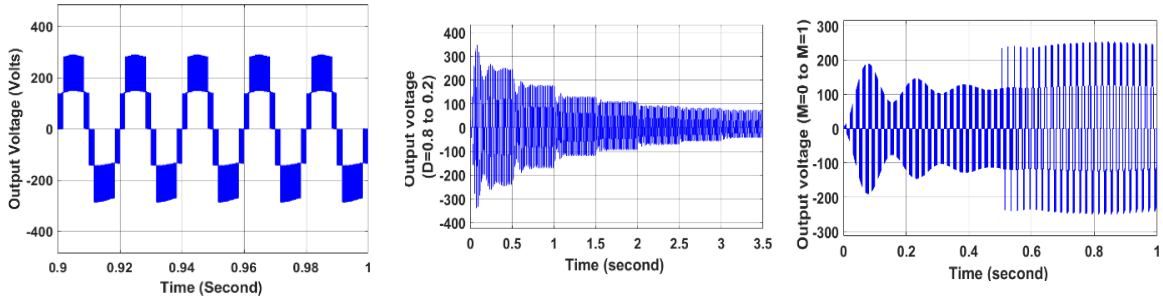
Table 5. Comparative analysis of the proposed structure and its comparable topologies

Structure	N_S	N_{Diode}	N_{Cap}	N_L	N_{Level}	Gain	CC	CG
[27]	3	6	2	2	3	$DV_{dc}/(1-D)$	×	✓
[28]	7	0	2	1	5	$2V_{dc}$	×	×
[29]	6	3	2	1	3	$DV_{dc}/(1-D)$	×	✓
Proposed 5-level	8	0	2	1	5	$2MV_{dc}/(1-D)$	✓	✓
Proposed 7-level	11	0	3	1	7	$3MV_{dc}/(1-D)$	✓	✓

*N_S: Switches count, N_{Diode}: Diodes count, N_{Cap}: Capacitors count, N_L: Inductors count, N_{Level}: Number of voltage levels, Gain: Voltage boost gain, CC: Continuous input current, CG: Common ground and M: Modulation index

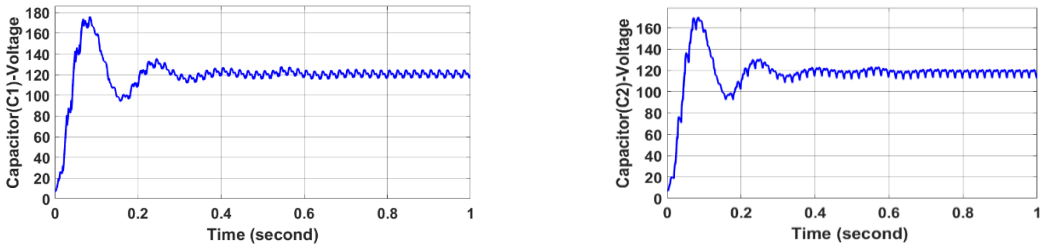
According to the Figure 7(a), the leakage current through the input source parasitic capacitance is zero. Moreover, the output current waveform of the inverter with the aforementioned characteristics in

Table 4, is shown in Figure 7(b). Furthermore, Figure 8(a) reveals the total harmonics distortion (THD) of 26.76% and Figure 8(b) shows 1.11% for the inverter output voltage and current, respectively.



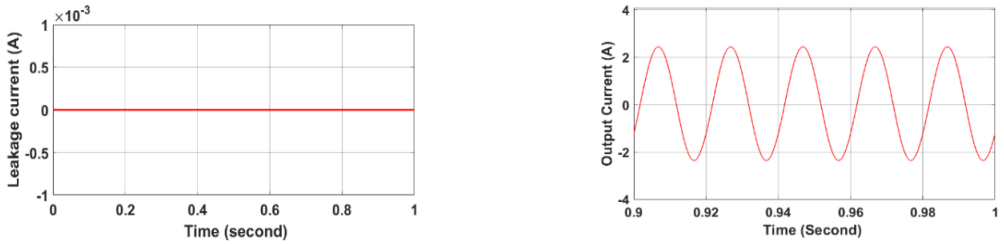
(a) (b) (c)

Figure 5. Output voltage waveforms: (a) output voltage waveform (D = 80%, M = 1), (b) sweeping the duty-cycle from D = 80% to D = 20, and (c) sweeping the modulation index from M = 0 to M = 1



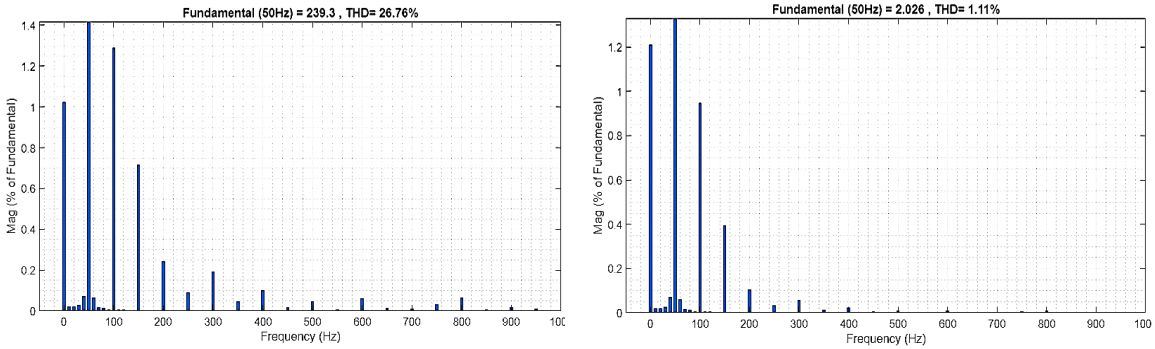
(a) (b)

Figure 6. Voltage waveforms of the inverter capacitors: (a) V_{C1} and (b) V_{C2}



(a) (b)

Figure 7. The current waveforms of the inverter: (a) leakage current waveform and (b) zoomed output current waveform



(a) (b)

Figure 8. The harmonic spectra and THD of the inverter: (a) output voltage and (b) output current

4.1. Inverter comparison and losses analysis

In this part, a comparison between the proposed 5-level- and 7-level proposed inverter with other new structures is presented in the following. It is found from Table 5 that the proposed inverter has higher voltage gain with continuous input current, which makes it suitable for PV and renewable energy applications. Also, the inverter benefits from its modular operation, resulting in higher boost voltage gains. Furthermore, the simulated converter is shown in Figures 9(a) and 9(b). Also, voltage gain comparison is shown in Figure 10(a). Moreover, the loss distribution between the inverter's components in percent and, the efficiency curve of the converter by varying the output power from 0 to 1500 watts with real condition according to the values in Table 6 are shown in Figures 10(b) and 10(c) respectively.

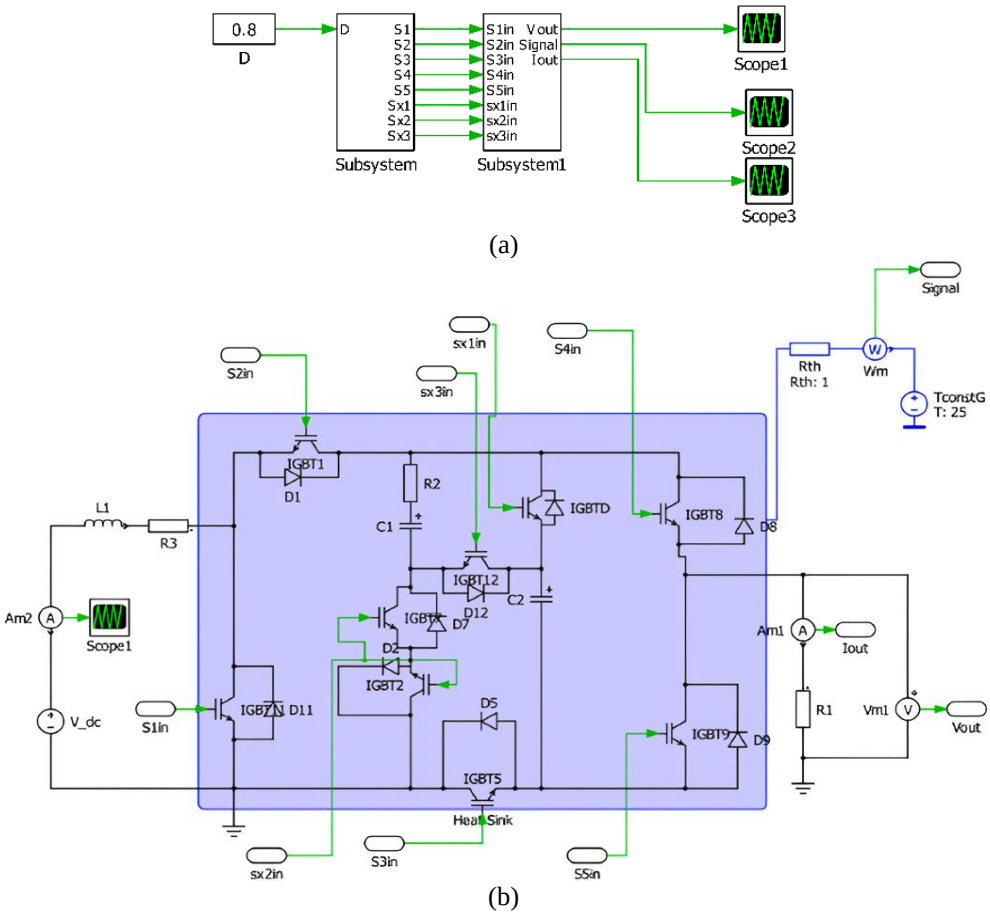


Figure 9. The simulated converter with PLECS software: (a) control system and (b) proposed converter

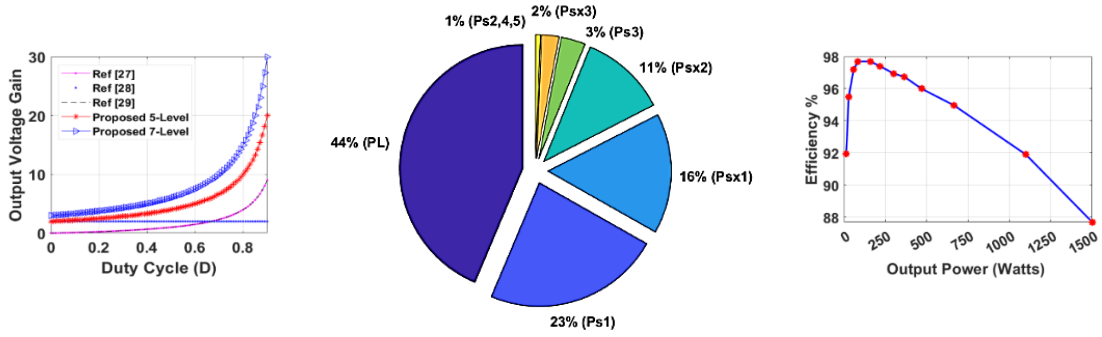


Figure 10. The voltage gain comparison and loss analysis of the proposed inverter: (a) output voltage gains vs duty cycle, (b) loss per components, and (c) efficiency curve

Table 6. Elements and parameters used to compute losses and efficiency

Parameter	Value	Parameter	Value
Power switches	IGBT-FGH60N60SMD	Input voltage	24 V
Input inductor	3 mH (10 mΩ internal resistor)	Duty-cycle (D)	80%

5. CONCLUSION

The present study has proposed a new multilevel boost inverter that features a non-pulsating current at the input, specifically designed for utilization in photovoltaic and other renewable energy systems. For the proposed inverter, the various switching methods for each output voltage level have been illustrated, resulting in advantages such as voltage balancing of capacitors and simple duty-cycle control. In addition, the structure's boost gain is doubled $(2D/1-D)$ for the 5-level structure and tripled $(3D/1-D)$ for the 7-level structure. The mathematical analysis of the inverter has been highlighted, and a comparison has been made between the proposed structure and other new relevant structures. Finally, the MATLAB/Simulink environment simulation results have been provided to demonstrate the inverter's efficacy.

APPENDIX

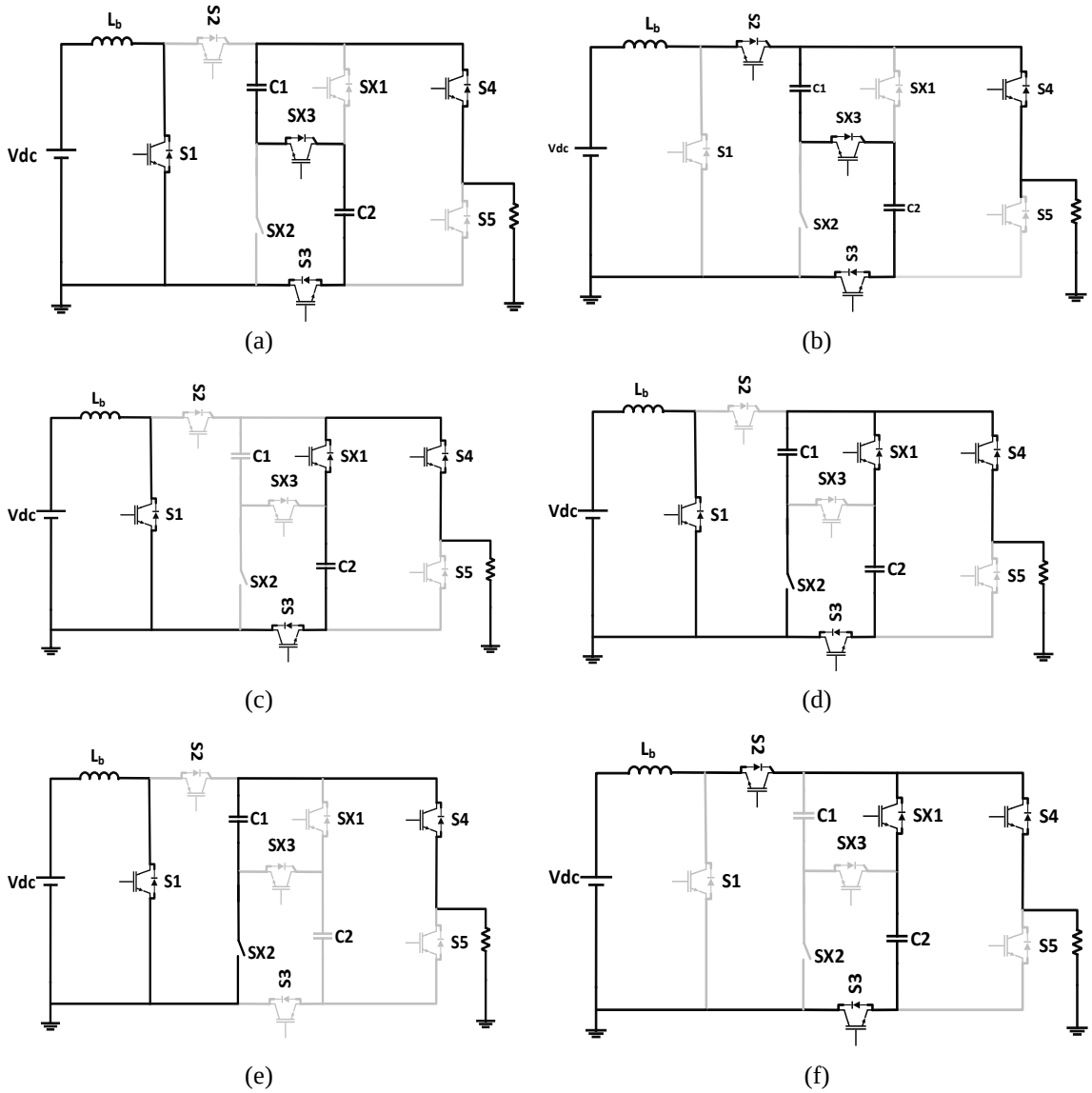


Figure 2. Various operational modes for the proposed 5-level structure, (a) state CN1, (b) state CN2, (c) state CN3, (d) state CN4, (e) state CN5, and (f) state CN6

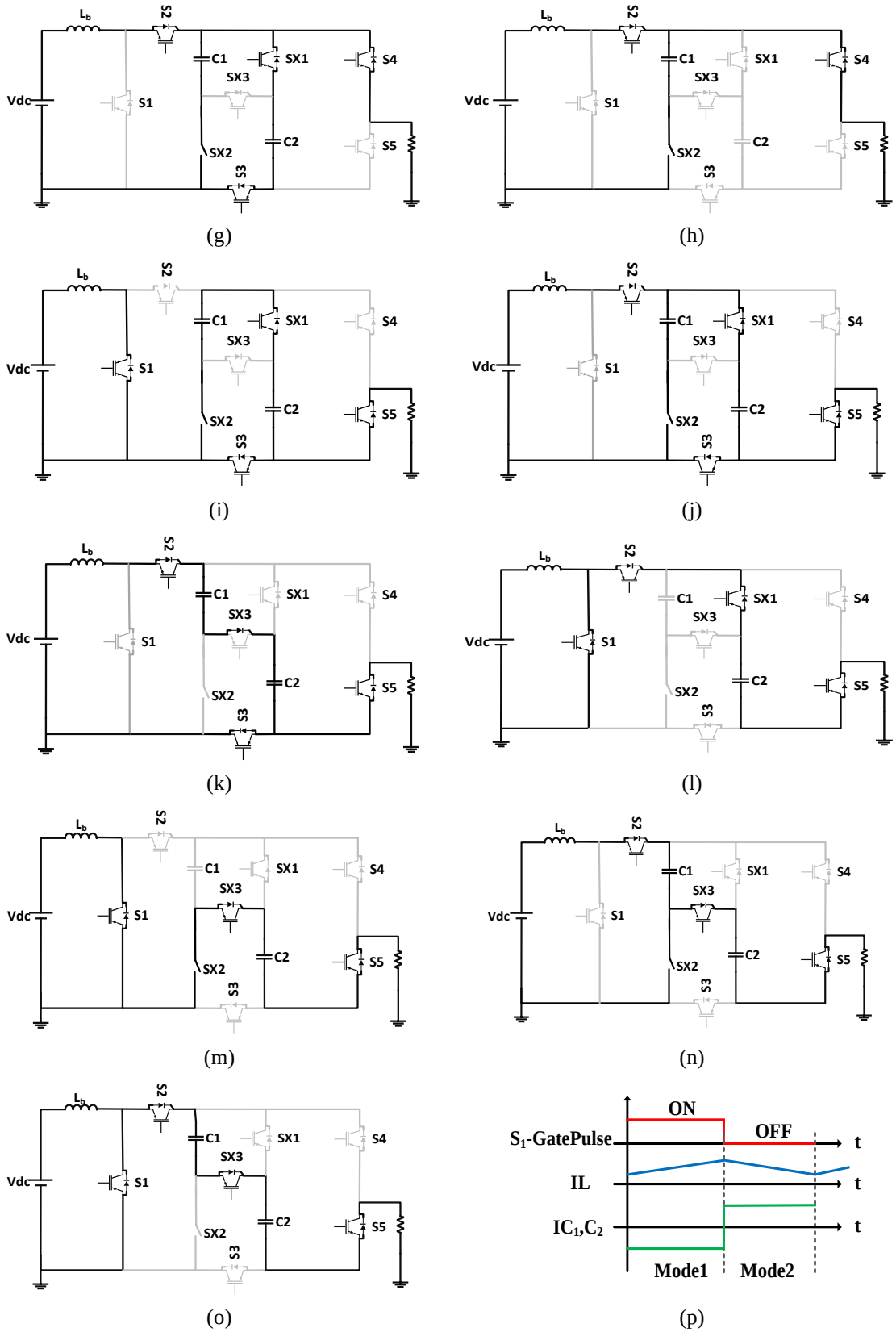


Figure 2. Various operational modes for the proposed 5-level structure: (g) state CN7, (h) state CN8, (i) state CN9, (j) state CN10, (k) state CN11, (l) state CN12, (m) state CN13, (n) state CN14, (o) state CN15, and (p) key waveforms of the inverter in charge and discharge operations (continue)

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