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Fast synchronization with enhanced switching control for grid-tied single-phase square wave inverter using FPGA

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ABSTRACT

Research on grid synchronization has been conducted worldwide by researchers in conjunction with the development of innovative technologies, such as dedicated short-range communication (DSRC) and cellular vehicle-to-everything (C-V2X). However, grid-connected inverters face several challenges, mainly the mismatch in voltage amplitude, frequency, and phase angle, as well as grid voltage disturbance and grid faults. Thus, the control algorithm of this research mainly focused on a half-cycle algorithm to design an enhanced digital switching control for fast synchronization using an FPGA. The control algorithm was developed based on zero-crossing detection (ZCD) and digital phase-locked loop (PLL) modeling techniques using the hardware description language (HDL) and a combination of digital logic blocks in Quartus II software, where the proposed switching was applied using the square-wave switching technique through a 300-watt full-bridge experimental prototype. The performance of the proposed technique was studied, where the total harmonic distortion (THD) for voltage and current resulted in a percentage reduction of 89.29% and 78.05% for voltage and current, respectively, after filter implementation. Also, the resulting signal synchronized in every half cycle and matched the voltage amplitude, frequency, and phase angle of the grid signal in 10 ms.

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1. INTRODUCTION

In recent decades, distributed generation (DG) based on renewable energy sources has grown in popularity, and strict grid-synchronization criteria have been enforced for the integration of dispersed generators with utility grids [1], [2]. Grid synchronization is the act of reducing the differences in voltage, frequency and phase angle between the original grid signal and the generated signal, where the electrical grid synchronizes the input signal by referring to the signal's frequency without exceeding the voltage from the grid [3], [4]. Since the intermittent nature of renewable energy sources such as wind and solar makes their integration with electrical grids unstable, attention must still be devoted to this issue [5], [6]. As a result, the

system requires grid synchronization and better power quality, which may be achieved by implementing appropriate control techniques and algorithms.

Research papers were reviewed with a focus on systems connected to the electrical grid and developed and simulated using software [3], [7]–[12]. The studies defined single-phase grid-connected modules, the methods for developing single-phase grid-connected inverters, the switching control and grid synchronization for single-phase input. Yazdani *et al*. [3] compared a proposed three-phase adaptive-notch-filtering (ANF) synchronization technique with existing three-phase synchronization algorithms, which were categorized into filtering algorithms, phase-locked loop (PLL)-based techniques, and ANF-based methods. Their results showed that the method of the synchronous reference frame with a PLL (SRF-PLL) and the improved SRF-PLL provided high-speed and accurate synchronization signals under ideal and unbalanced conditions, respectively. Yaai *et al.* [7] proposed a control strategy of a PV grid-connected inverter to stabilize the grid during grid fault by maintaining a balanced output using a fault ride-through control strategy. Fuad *et al.* [8] researched grid voltage synchronization based on various PLL techniques, which were SRF-PLL and decoupled double SRF-PLL (DDSRF-PLL). The results showed that the SRF-PLL technique demonstrated a deficient performance under unstable conditions, while the DDSRF-PLL technique had limitations that were reflected in its performance under harmonically distorted conditions and phase angle jumps. Yang *et al.* [9], Konara *et al*. [10], and Shaikh and Joseph [12] conducted research using MATLAB/Simulink software simulations. Based on the results, the second-order generalized integrator with a frequency-locked loop (SOGI-FLL) was able to synchronize voltage and current accurately compared with the ZCD method under weak-grid conditions [9]. The ZCD method also failed under non-harmonic conditions, while the PLL method precisely synchronized with the grid [10]. In contrast, the PLL algorithm was able to synchronize precisely while detecting grid parameters [12]. Hadjidemetriou *et al.* [11] researched the technique of the multi-harmonic decoupling cell with a PLL (MHDC-PLL) for grid synchronization, which was found to respond quickly and accurately despite grid disturbances. Thus, a novel reformulation of an equivalent decoupling cell and a frequency-adaptive quadrature signal generator for the MHDC-PLL method has been proposed for accurate responses under non-nominal frequency. The research gap was figured out by comparing the proposed research with previous research based on system performance as well as application methods. Apart from that, in this research, a low-pass LC filter was implemented, as its ripple factor was the lowest compared with those of other filters [13]. The significant difference between earlier studies and this research is the digital implementation was based on the field-programmable gate array (FPGA) to generate square wave switching signals with 3rd-harmonic elimination for the full-bridge inverter for a fast-response system.

A fast response is required during synchronization to detect sudden changes in the grid, especially during an unbalanced load, to produce a smoother output with lower distortions such as in vehicle-to-grid (V2G). According to research, V2G technology renders valued grid services a significant application in the worldwide transition to the developing of green and sustainable energy economy, as it enables pollution-free driving [14]. V2G technology returns electricity back to the grid from the vehicle and this system is considered as the grid-tied electrical system, also known as a semi-autonomous electricity generation system, which feeds excess capacity back into the local power grid and draws from the grid when there is insufficient electricity. Thus, grid synchronization is essential for creating a more resilient and sustainable energy industry and it refers to the process of matching the voltage, frequency, and phase of the output signal with those of the grid signal with a faster response time that requires grid-tied inverter, also called the synchronous inverter, which utilizes a local oscillator to synchronize the frequency and converts DC voltage to AC voltage without changing the supply line phase and frequency.

Subsequently, the controller used in this proposed system is a FPGA which is a fast-response semiconductor integrated circuit that uses a very-high-speed hardware description language (HDL) to control a system without changing the hardware and can be configured at any moment after being manufactured [15]. FPGAs also have been widely used for switching in various kinds of converters, such as DC and AC converters, as the main advantage is that FPGAs consume less power than analog control circuits [16]. Furthermore, FPGAs offer greater flexibility, parallel processing capabilities, customization, hardware acceleration and reusability compared with digital signal processors (DSPs) [17]. With the advent of solid-state switching device technologies and fast DSPs, such as FPGAs, PWM algorithms have been developed to produce PWM signals in real-time for microcontroller systems through digital processing [18]. The PWM technique, in its simplest form, generates an on-and-off signal to activate a switch to allow current to flow through a circuit, and PWM signals can be developed using a digital or analog controller [19], [20]. In a complete cycle, the "on" state affects the degree to which current flows, resulting in the amount of current flowing through the circuit being directly proportional to that of the "on"-state system [19].

Thus, the contribution of this paper is developing an enhanced fast-response switching scheme to ensure the system responds in the next half cycle for grid synchronization by using FPGA, where the scheme was developed using Quartus II software based on the integration of ZCD with the digital PLL input which is

crucial for the operation of grid-tied power inverters for the reasons of grid voltage monitoring and synchronization for the HDL-designed circuitry and analyzing the performance of the proposed fast-switching method. In this research, the switching technique implemented was based on the square wave with a phase shift for harmonic elimination. Finally, the proposed system was developed to overcome issues in synchronization by matching the differences in voltage amplitude, phase angle and frequency in a half cycle and responding quicker to the changes. Also, this research focused on the faster-synchronization technique for the effective, dependable, and stable operation of contemporary electrical grids, particularly as the increase in the integration of renewable energy sources has made easing seamless grid integration and minimizing grid interruptions crucial for the smooth transition to a future with more sustainable energy. The rest of the manuscript was organized as: i) Section 2 consists of the research methodology of the proposed system; ii) Section 3 documents the results and detailed analysis of the experimental assessments of the research; and iii) Section 4 concludes the overall manuscript.

2. RESEARCH METHODOLOGY

In this section, the methodology used to complete the research is presented. In the first subsection, the overall block diagram of the proposed circuit is presented. Also, the proposed system's algorithm, software development and hardware configuration are presented in the subsequent subsections.

2.1. Proposed circuit's block diagram

In the proposed system, the main controller implemented were an FPGA, at where the control structure developed in synchronous reference frame (SRF) since it was crucial to align the reference signal with the grid signal so that the current injected into the grid could be precisely controlled. Whereas, the other key components were a single-phase full-bridge inverter, a zero-crossing detector, gate driver units, an LC filter and two types of transformers, which were an isolation transformer and a step-up transformer. Figure 1 shows the complete block diagram for the hardware configuration of the proposed system.

The isolation transformer was connected to the zero-crossing detector, and the FPGA board was supplied with a DC source of 5 V. The FPGA board was then connected to the gate driver unit, which was then connected to the single-phase full-bridge inverter supplied with 24 V of DC source. Then, the inverter circuit was connected to the designed LC filter and step-up transformer to generate the AC voltage to be synchronized with the grid voltage. The controlling technique used in the FPGA board was ZCD with the implementation of the PLL.

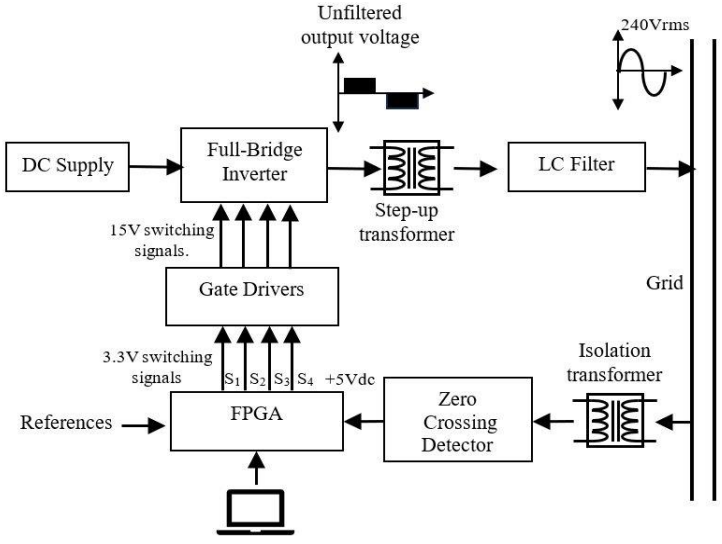

Figure 1. Proposed circuit's block diagram

2.2. Proposed system's algorithm

The designed algorithm's flowchart for producing the synchronized signal based on the ZCD-integrated PLL component is shown in Figure 2. The ZCD output operation circuit generated a high signal of "1" and a low signal of "0" for sinusoidal waveforms that were detected in the positive and negative cycles,

respectively. Thus, based on the ZCD output that transmitted a signal to the FPGA board input used for the inverter gate operation, the chosen FPGA board would emit digitalized switching signals for either positive or negative sinusoidal waveform, hence establishing a fast synchronization system with enhanced switching control. In this proposed system, initially, the switch trigger is based on the ZCD input. Hence, when the ZCD output emitted 1, the positive (+ve) counter was enabled and started counting for the positive cycle and at the same time generated a positive sine wave. In contrast, when the ZCD output emitted 0, the negative (-ve) counter was enabled and started counting for the negative cycle and at the same time generated a negative sine wave.

The control algorithm of this research was developed based on ZCD and digital PLL modeling techniques. PLL is an electronic circuit with a voltage or voltage-controlled oscillator that continuously adjusts to match the input signal's frequency and it is widely used in various fields, most notably in communication systems and power electronics, due to its easier implementation, robustness, dynamic performance, and effectiveness [21]–[23]. In this proposed system, the PLL was used to match the phase of the generated signal with the phase of the grid signal, where the phase detector would detect and eliminate the phase difference between the reference input signal and the generated signal. Besides that, to match the frequency or period of the generated signal and that of the AC signal, ZCD was used in the proposed system to detect the shift of a signal waveform from positive to negative, producing a narrow pulse that would ideally correspond to the zero-voltage condition while detecting the frequency and phase angle of the grid [24], [25]. In a variety of applications where precise phase and frequency control is required, integrating ZCD with the PLL can improve synchronization, where the PLL's output is able to synchronize with the zero-crossing of the reference signal and provide precise synchronization with the utility grid. Also, maintaining synchronization with the utility grid is crucial in the application of power electronics, such as grid-tied inverters, where the PLL can precisely track the grid voltage's zero-crossing when used in tandem with ZCD. Hence, a phase-locked output waveform may be created to correctly inject or remove power by matching the phase and frequency of the grid.

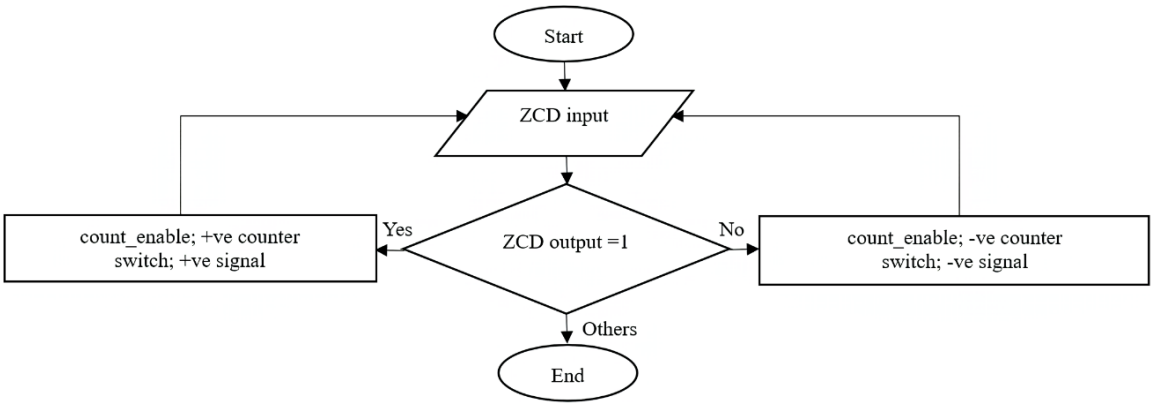

Figure 2. Flowchart of developed algorithm

2.3. Simulation software

The software involved in this research were MATLAB/Simulink and Quartus II. As shown in Figure 3, MATLAB/Simulink was used in the initial design stage for modelling the circuitry. The circuitry was supplied with a 24 V_{dc} source. For the configuration of the inverter, MOSFETs were used as switching devices. An RC integrator circuit was connected in parallel with the input supply, where the output voltage was acquired from across the capacitor, while the input was coupled to the resistance. The capacitor would charge up when the input is high and would discharge when the input is low. Apart from that, the inverter was also connected with a load of 100 Ω. Then, the inverter was connected to the LC filter and the isolation transformer to obtain a sine wave signal, along with the grid signal. Furthermore, the coding of the proposed system algorithm was developed using Quartus II software with the aid of the hardware description language (HDL) and integrated digital logic blocks, such as clocks, counters, switches, and comparators, as well as the digital input from the ZCD. The program's block diagram is depicted in Figure 4. The counter blocks (*lpm_counter0* and *lpm_counter1*) were set to count from 0 to 180000 for positive and negative cycles, where the counting process was enabled by the digital ZCD input. The sampling for each half cycle was set to be large due to advantages such as higher accuracy, reduced aliasing, and a better signal-to-noise ratio. Four pins (PIN_C30, PIN_C29, PIN_D29 and PIN_D28) were assigned to the programmable output blocks to allow the FPGA to interface with the corresponding inverter switches.

2.4. Experimental setup

In this subsection, the components used in the development of the proposed system were described. The system mainly consisted of a single-phase full-wave inverter with four MOSFETs, a zero-crossing detector, a gate driver circuit, a step-up transformer, an isolation transformer, and an LC filter. Figure 5 depicts the hardware configuration of the proposed system, while Table 1 presents the detailed hardware specifications.

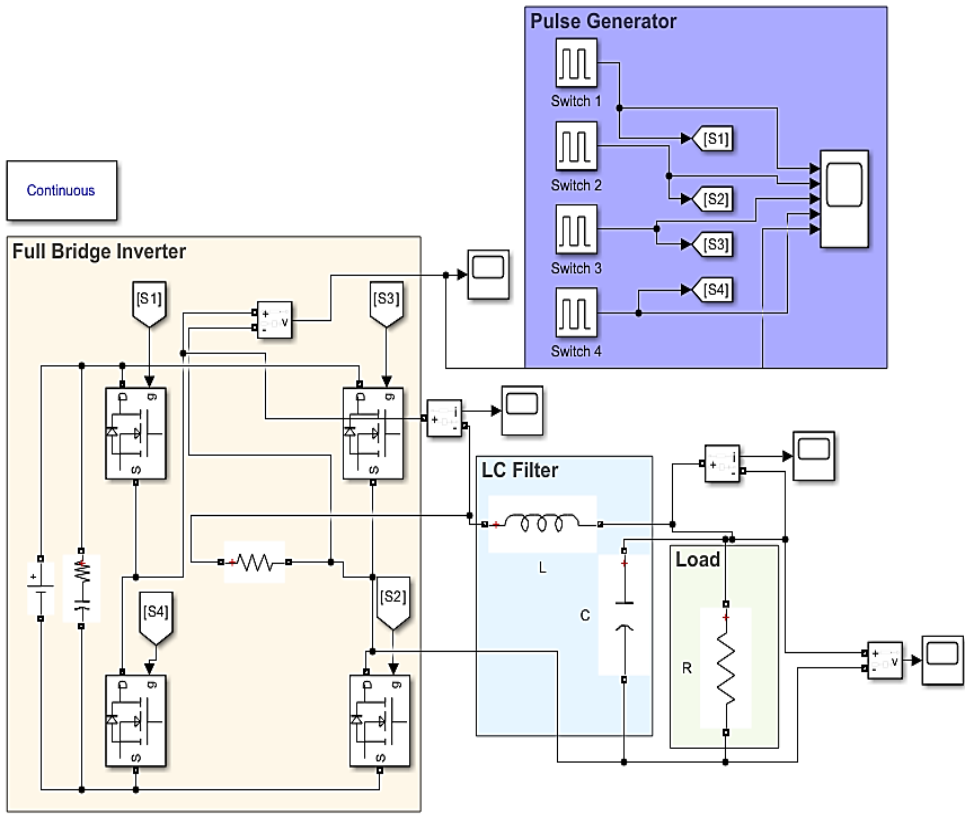

Figure 3. MATLAB/Simulink model

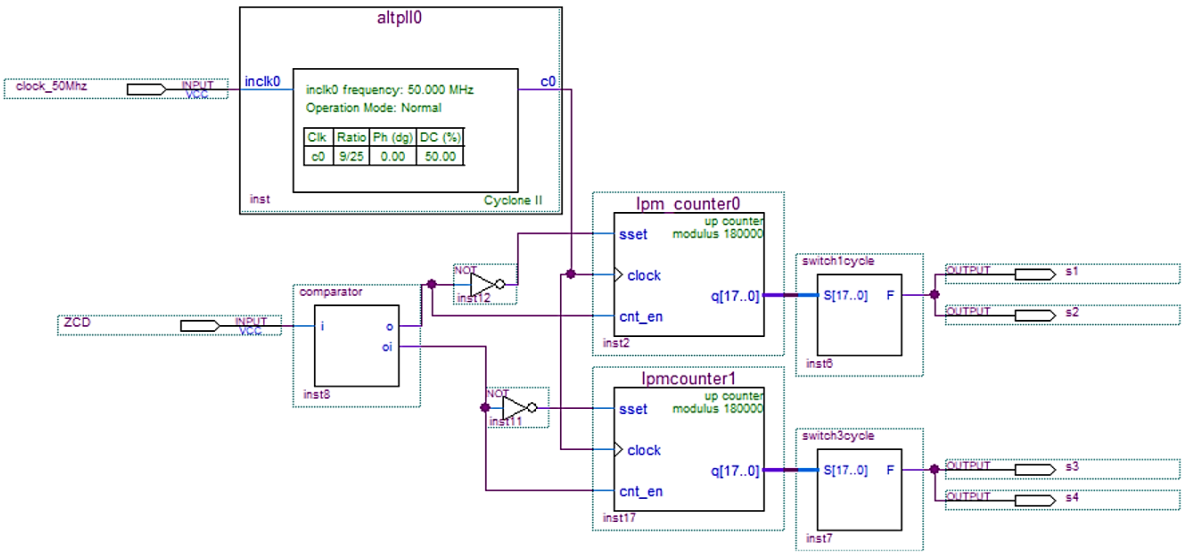

Figure 4. PWM switching signal's block diagram (*.bdf) using Quartus II software

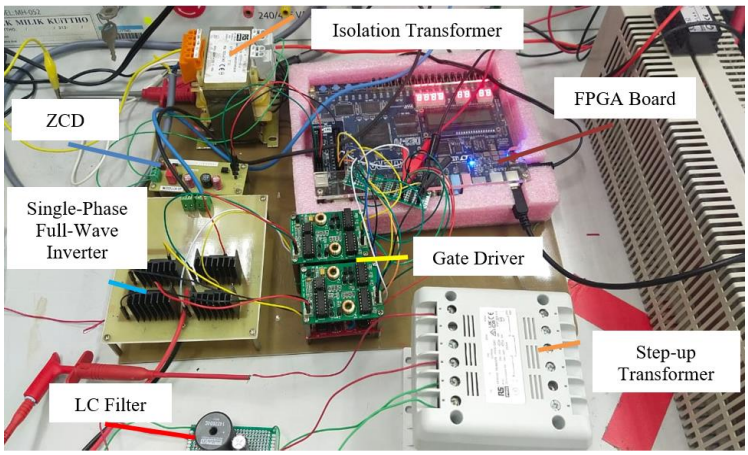

Figure 5. Hardware configuration

Table 1. Hardware specifications

Hardware Components	Descriptions
Controller	FPGA: DE2-70
System frequency	50 Hz
Input voltage	24 V_{dc}
Output voltage	240 V_{ac}
MOSFETs	IRFP460BPBF
Gate driver units	3.3 V– 18 V
ZCD	BM1Z002FJ-EVK-002
LC filter - Inductor	22 mH
LC filter - Capacitor	120 µF
Isolation transformer	160 VA
Step-up transformer	250 VA

2.5. Amplitude and harmonics control in phase-shifted square wave inverter

It is crucial to control the amplitude and harmonics in phase-shifted square wave inverter to ensure its reliability in the proposed system. Calculations involved for adjusting the interval of α on every side of the pulse as zero and obtaining the desired output voltage are presented below. Firstly, the root mean square (RMS) voltage value is obtained by using (1), where *n* stands for the harmonic number.

$$V_{rms} = \sqrt{\left\{\frac{1}{\pi}\int_{\alpha}^{\pi-\alpha} V_{DC}^2 d(\omega t)\right\}} = V_{DC}\sqrt{1-\frac{2\alpha}{\pi}} \quad (1)$$

Also, the instantaneous output voltage in the Fourier series can be computed by using (2).

$$v_o(t) = \sum_{n,odd} V_n \sin n\omega t \quad (2)$$

Then, the amplitude of half-wave symmetry can be calculated as in (3).

$$V_n = \frac{2}{\pi}\int_{\alpha}^{\pi-\alpha} V_{DC} sin(n\omega t) d(\omega t) = \left(\frac{4V_{DC}}{n\pi}\right)\cos(n\alpha) \quad (3)$$

The amplitude of the fundamental frequency is controllable by adjusting the angle of α, as in (4).

$$V_1 = \left(\frac{4V_{DC}}{\pi}\right)\cos(\alpha) \quad (4)$$

The *n*th harmonic may be eliminated by determining the suitable displacement angle α if $\cos n\alpha = 0$, or else by using (5).

$$\alpha = \frac{90^\circ}{n} \quad (5)$$

For instance, the 3rd-harmonic, called the "triplens" harmonics effect for the *n*th harmonic, may be eliminated using α=90°/3. Therefore, in the proposed system, the phase angle of the inverter was adjusted digitally through HDL coding, where the phase angle was adjusted by 30° to eliminate the 3rd-harmonic.

2.6. LC filter design

A low-pass filter based to the combination of inductor (L) and capacitor (C) was necessary to reduce the THD, the impacts of which can cause ripple current waveforms and unsmooth current flow in the proposed system. The passive component values were first calculated based on the required output voltage of the inverter. All calculated parameters were then model-designed using MATLAB/Simulink software and validated through simulations. For the inductance computation, the equation used was the formula to calculate the maximum inductance current, ΔI_{Lmax} as depicted in (6).

$$\Delta I_{L_{max}} = \frac{V_{dc}}{4 \times L \times F_{sw}} \tag{6}$$

Then, the equation is simplified to obtain the inductance value, *L*, as in (7).

$$L = \frac{V_{dc}}{4 \times \Delta I_{L_{max}} \times F_{sw}} \tag{7}$$

For the capacitance value, *C*, the equation used is the formula to calculate the cut-off frequency, F_c, as represented in (8).

$$F_c = \frac{1}{2 \times \pi \times \sqrt{L \times C}} \tag{8}$$

The cut-off frequency, F_c, should be smaller than the switching frequency, F_{sw}, as represented in (9).

$$F_c <= \frac{F_{sw}}{10} \tag{9}$$

To obtain the suitable capacitance value *C*, the (8) is then simplified to (10).

$$C = \left(\frac{10}{2 \times \pi \times F_{sw}}\right)^2 \times \frac{1}{L} \tag{10}$$

3. RESULTS AND DISCUSSION

In this section, the results of the simulations and the experimental analysis performed in the research are presented for developing the proposed system with enhanced switching control for a fast-response grid-tied single-phase inverter using the FPGA. Thus, the analysis and discussion are presented based on the results gathered from simulations using MATLAB/Simulink and Quartus II. In the following subsections, the model developed using MATLAB/Simulink, the model developed using Quartus II and the results obtained are presented. All measurements for the experimental analysis were captured using four channel digital phosphor oscilloscope (TDS 3024B). The results obtained from the developed 300-watt full-bridge experimental prototype were also recorded. Thus, this section comprises the analysis of various signal waveforms, which were the switching signals, the grid signal, the ZCD signal, the square waveform of the single-phase full-bridge inverter and the resulting output signal of the proposed system after filter circuit implementation.

3.1. Switching signals

The single-phase full-bridge inverter consisted of four switching devices to ensure a bidirectional power flow for high-quality power conversion. Hence, Figure 6 and Figure 7 illustrate the switching signals acquired from the software simulation and experimental analysis, respectively, for the single-phase full-bridge inverter utilized in this research. The switching signals (S_1, S_2, S_3 and S_4) were measured from each MOSFET gate signal output in the inverter circuitry. The square wave signal was obtained from the overall inverter configuration. The developed program was then uploaded to the DE 2-70 FPGA board to segregate the switching signal of the square wave inverter into four individual switching signals S_1, S_2, S_3 and S_4, as depicted in Figure 7. Analyzing the results obtained from the oscilloscope, it was observed that S_1 and S2 were both in the positive cycle, generating a voltage of $+V_{dc}$, while S_3 and S_4 were both in the negative cycle, producing a voltage of $-V_{dc}$.

3.2. Grid and ZCD waveforms

The experimental analysis results concerning the integration of a ZCD with a PLL are presented in Figure 8. During the positive cycle of the grid voltage, the ZCD produced a high signal (+3.3 V_{dc}). Conversely, when the grid voltage entered the negative cycle, the ZCD detected this transition and produced a low signal (0 V). These observations demonstrate that the ZCD is effectively incorporated into the proposed system to identify the zero-crossing point of the grid voltage signal, where the voltage switches from positive to negative or vice versa. The digital PLL utilizes this signal to synchronize the inverter switching with the grid voltage, leading to rapid response times, and enhanced overall system efficiency.

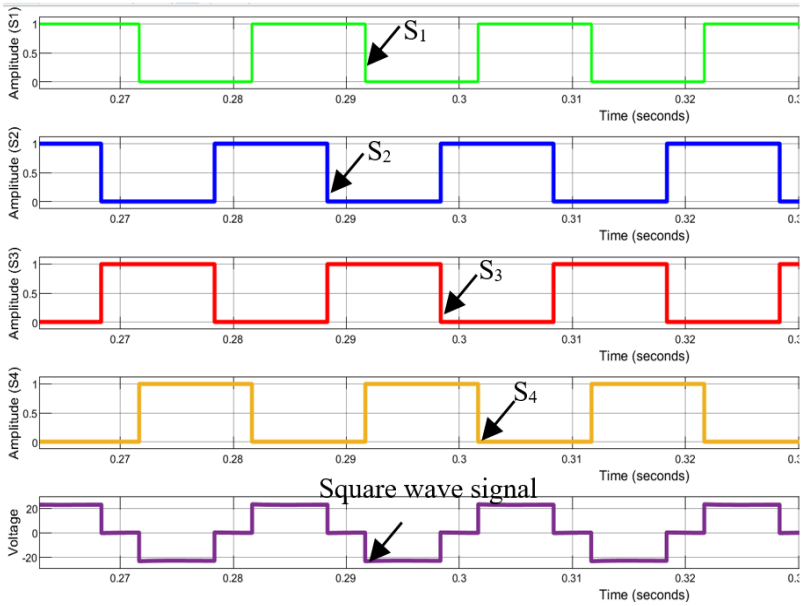

Figure 6. Switching signals (software simulation)

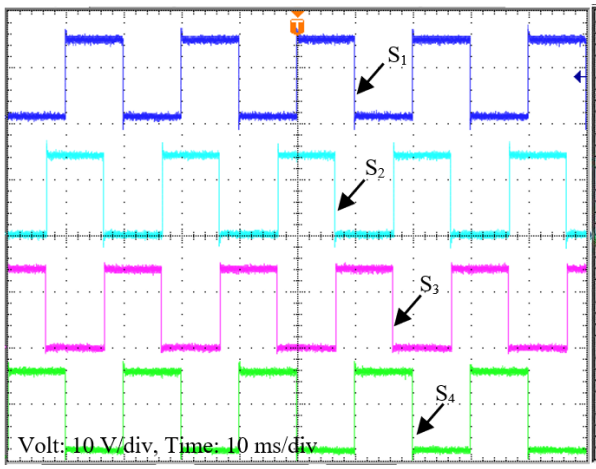

Figure 7. Switching signals (experimental analysis)

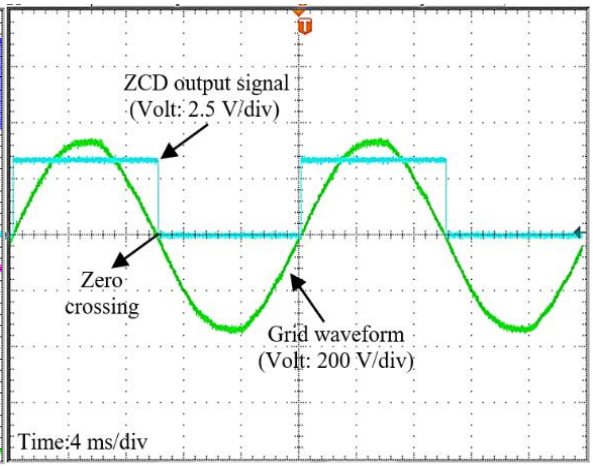

Figure 8. ZCD and grid waveform

3.3. Grid synchronization

In this subsection, the stages of grid synchronization are explained in detail. Firstly, grid synchronization was determined when the grid voltage and the signal delivered from the inverter are in-phase in order to obtain a fast synchronized system. Figures 9 and 10 depict the output obtained for the unfiltered output signal. Under this condition, the unfiltered inverter output was in phase with the grid voltage that

indicates both the signals are operating at same frequency as well as the peaks and the zero-crossings of the signals. This is a crucial step in this research to ensure proper operation and prevent power quality issues.

The single-phase full-bridge inverter was then connected to the LC filter circuit to obtain a smooth sinusoidal waveform, as depicted in Figure 11. The appropriate values of inductance and capacitance resulted in an equivalent output signal to the grid waveform. Figure 12 shows the filtered and grid waveform signals, which were phase-aligned to measure the phase delay between the grid signal and the resulting signal.

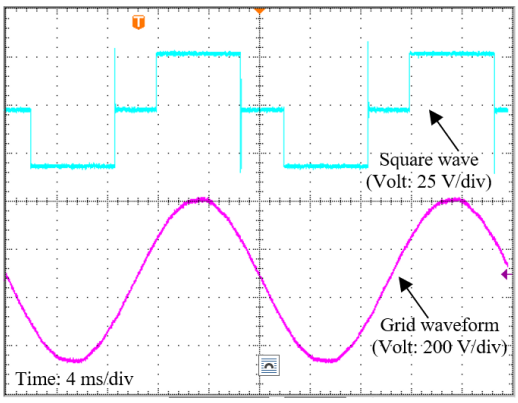

Figure 9. Unfiltered output (square wave) and grid waveform

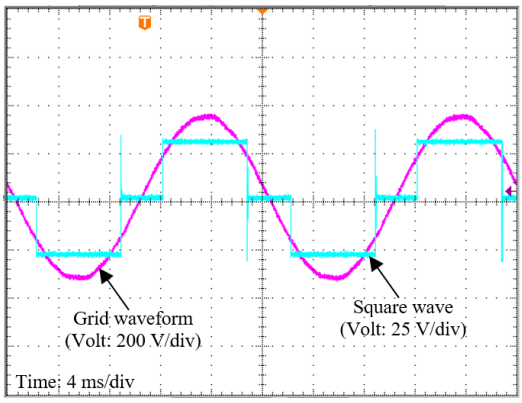

Figure 10. Unfiltered output (square wave) and grid waveform (in phase)

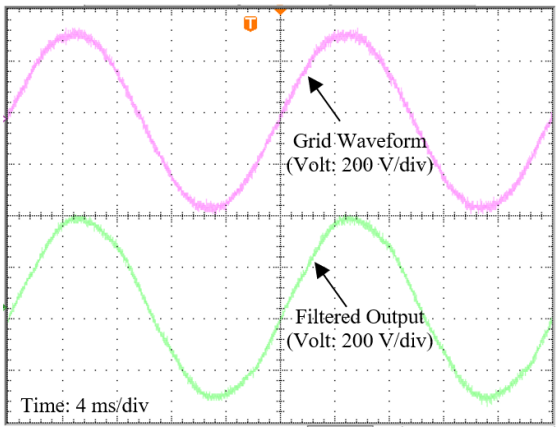

Figure 11. Filtered output (sinusoidal waveform) and grid waveform

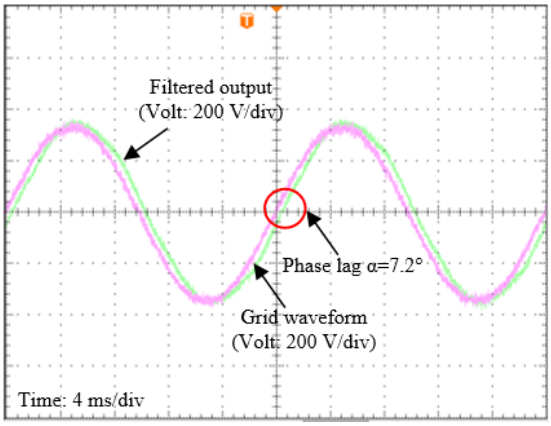

Figure 12. Filtered output (sinusoidal waveform) and grid waveform (out of phase)

As shown in Figure 12, the LC filter introduced a phase lag in the output waveform of the system. This phase lag was primarily caused by the reactive components, mainly the inductor and the capacitor in the filter. The inductor caused a lagging phase shift between voltage and current, while the capacitor caused a leading phase shift. In this case, the combined consequent phase shifts resulted in an overall phase lag in the generated output waveform, where the phase shift was quantified by the angle α. In this case, the measured lag was α=7.2°, meaning that the resulting signal was 7.2° out of phase with the grid signal, which can also be described as the resulting signal lagging behind the grid signal by 7.2°. The generated voltage may still be supplied to the load but there can be consequences and potential issues, such as distortion in the voltage supplied, increased energy losses in the system, effects on the performance and lifespan of the connected load and issues in voltage regulation. Hence, a control strategy was associated in the digital PLL to mitigate the phase lag and uphold precise phase correlation between the grid and generated output waveform. In this scenario, digital PLL was essential for promptly identifying disturbances and modifying the converter's output in order to compensate for them when the grid voltage undergoes phase jumps, frequency jumps, or voltage sags. This compensation guarantees that the grid-connected system remains functional despite the grid's fluctuating behaviors and aids in maintaining the stability of the system. Figure 13 shows the generated

waveform and the grid waveform after adjusting the phase angle in the digital PLL. It is clearly shown that the generated voltage was now in phase with the grid voltage. This synchronization was achieved by adjusting α, which in this case was set to 7.2° in the digital PLL. Thus, the resulting signal was synchronized in-phase with the grid signal at a voltage amplitude of 360 V at 50 Hz and responded for the next half cycle at 10 ms.

A Fast Fourier transform (FFT) analysis was performed for THD_v and THD_i. In this research, the LC filter was used to reduce the THD for voltage and current. As a result, for THD_v, the harmonic value was 30.63% before the filtering component while the harmonic value was reduced to 3.28%, after the implementation of filtering component in the circuitry due to the lower 3rd-harmonic. Subsequently, for THD_i, the harmonic value was 14.94% in the absence of the filtering component while the harmonic value was then decreased to 3.28% after implementation of the filtering component to the circuitry, due to the lower 3rd-harmonic. Specifically, the THD for voltage was reduced by 89.29% and the THD for current was reduced by 78.05%. Subsequently, this method allowed for a fast response using the ZCD signal and the digital PLL. Table 2 presents the THD analysis of the system developed using MATLAB/Simulink software.

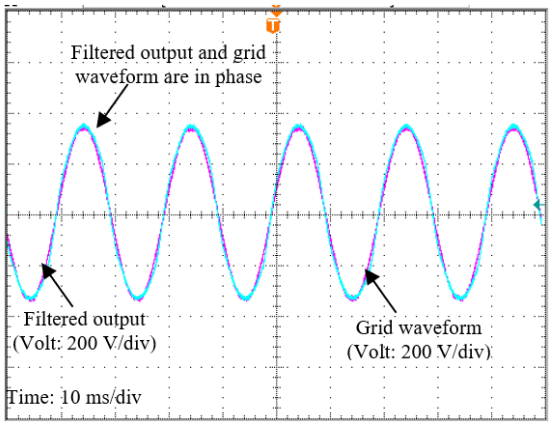

Figure 13. Filtered output (sinusoidal waveform) and grid waveform (in-phase)

Table 2. THD analysis using FFT analysis

THD	Before filter	After filter
THD_v	30.63%	3.28%
THD_i	14.94%	3.28%

4. CONCLUSION

In conclusion, the paper focused on designing a fast synchronized with enhanced switching control for a fast-response grid-tied single-phase inverter using FPGA. The inverter was successfully simulated using MATLAB/Simulink and a digital PLL was implemented using Quartus II software. The synchronization was achieved by adjusting the phase lag of the generated signal using the digital PLL and ensured the signals synchronized in terms of voltage amplitude, frequency, and phase angle from the next half cycle. Subsequently, the THD analysis for voltage and current showed that both the harmonics significantly decreased after implementing the filtering component. Apparently, the THD_v was 30.63% before filtering and 3.28% after filtering, whereas the THD_i was 14.94% before filtering and 3.28% after filtering. Hence, it can be said that the decrease in harmonics was mainly contributed by the 3rd-harmonic elimination. In order to broaden the scope of this research, integration with green technology and renewable energy sources like solar and wind energy will be implemented.

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